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SMEMA Council APEX®
Designers Summit 04

Optimal PCB Test Trace Design for Improved Quality Control

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Abstract
A common industry practice is to confirm the characteristic impedance of critical PCB traces meet specified performance tolerances before any components are attached. A popular technique is to use a time domain reflectometery (TDR) to derive the characteristic impedance from reflections of a pulse injected into the designated "test" trace. One problem with the TDR method is that interconnect anomalies located closer to the TDR launch location can impact the "apparent" impedance of interconnect geometries following the anomaly. For example, through and stub via effects, trombone delay lines, and skin depth losses can easily cause the computed TDR impedance to falsely indicate an out-of-tolerance condition, when in fact the PCB is properly constructed. This paper describes what measures can be taken during the PCB layout to ensure that subsequent TDR measurements of critical impedance-controlled traces will accurately represent the true characteristic impedance.

Introduction
In many instances test traces are deployed either on a test coupon or on the printed circuit board (PCB) itself to assure the quality of manufacturabilty of the PCB. Most often these specifications are either impedance control or propagation delay, where the test traces (or coupons) are being used in conjunction with a digital sweep scope, in a procedure called time domain reflectometry (TDR). In using TDR analysis, a small signal is introduced into the trace (of a known voltage) of which the rise time (RT) of the voltage step is on the order of 40– 80ps. The output of the reflected voltage is sampled and information ascertained about the test coupon impedance given the relationship between the reflected and incident voltage. Propagation delay information is also gathered based upon the time the signal was injected into the test trace and the time took to travel back to the scope (sometimes referred to as round trip delay). Figure 1 shows a typical TDR setup with a typical test coupon.

TDR measurements are commonly used to test both the viability and quality of manufactured PCB's. Since the measurements made from these test traces may go on to either pass or fail expensive PCB's, it is imperative that good design practices are employed to minimize erroneous test results during the quality control (QC) process. The problem is, that test trace design is usually only thought about secondarily, or not at all relative to actual PCB trace layout. As an example, in Figure 2, several problems prevalent with the test traces on the PCB. The first problem is to note the difference in pitch between two different test traces and the ground (GND) pad. Note also that at several places, the traces move back and forth, adjacent to one another in what is known as a trombone or serpentine trace layout. Another real issue is the proximity of vias and other physical structures that are placed close to the test traces themselves (note the large BGA package in the center of the board and the corresponding test trace).

The real issue is that many of these effects cause problems in what we attribute to be problems with the traces in the PCB itself, which may or may not be the case. We would like to therefore minimize the issues that can cause erroneous results and offer a few guidelines for producing test traces.

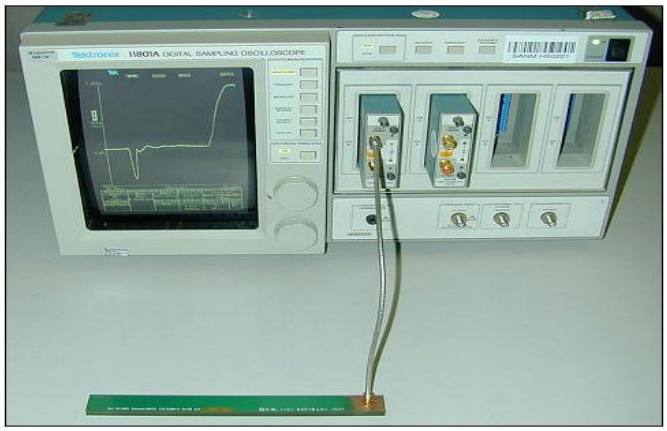

Figure 1 - Typical TDR Setup with a 6" Test Coupon

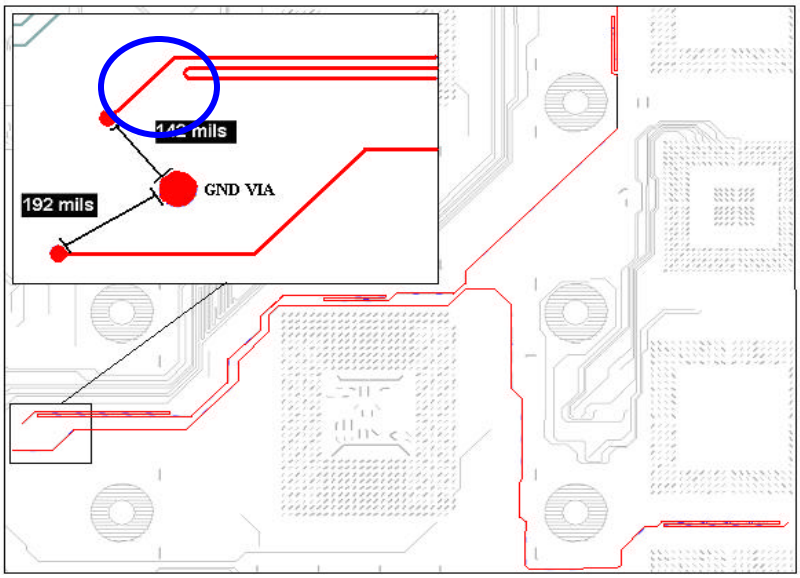

Figure 2 - PCB Outline with Test Traces in Blue, Showing Different Signal / Gnd Pitch, Folded "Trombone" Traces and Close Proximity to Other Packages

Minimizing the Inductance

Inductance can be a significant issue with TDR testing. One should focus on minimizing the inductance that is inherent between the signal (via or launch pad) and return path to the reference plane. When thinking about inductance, realize it is the manifestation of the return current path from the signal source. The longer this path is, the larger the inductance usually is. In Figure 3, three different homemade probes have been made to probe between a signal and gnd via in a test coupon, pictured above the probes. In probes A and B, the ground return happens to be through the small pin attached to the metal cladding on the outside of the cable. While this feature allows for easy modification to any via pitch on a PCB, by bending the ground pin on the probe, it lends itself to a greater amount of inductance and hence, measurement discontinuities. Figure 4 shows the result of having a low inductance path versus a higher inductance path of these two probes. The effect here is that the inductance shows up clearly as a discontinuity in the TDR, it also slows the rise RT of the signal down and may occlude certain features of the via, as depicted in Figure 4. If we are to further remove the inductance, by removing the ground pin all together, and use the cladding as the return path as in cable probe C, we see even a further reduction in the perceived inductance. In Figure 6, when we compare the straight coax to a commercial probe, as depicted in Figure5, the improvement in measurements made from the straight coax are obvious, in fact, we see no lead inductance at all. Of course, the usefulness of a single coax is only beneficial if a ground return path is readily available adjacent to the cable cladding. Most often a standard probe will be used. It is important to be aware then of inductance that is perceived at the head of the launch as perturbations that may be of the probe and not of the launch via or trace.

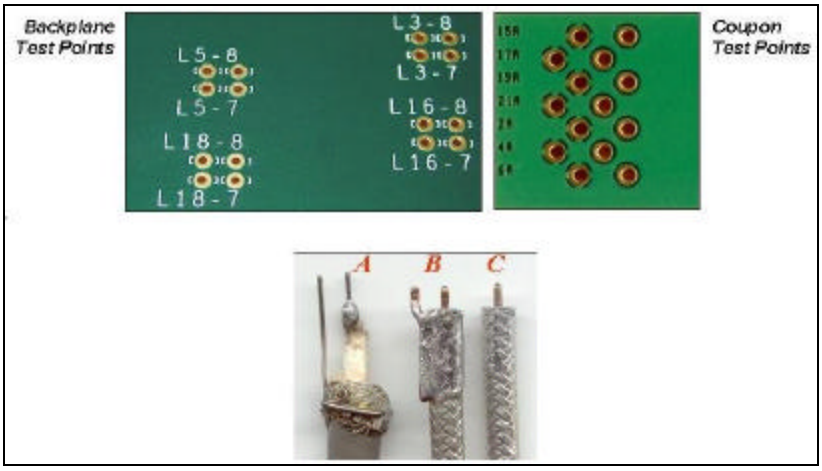

Figure 3 - Test Coupon and Backplane Test Points with Homemade Probes used to Test Traces. Probe A Carries More Inductance Than Probe C, and Therefore is Not as a Favorable for Impedance and Propagation Measurements

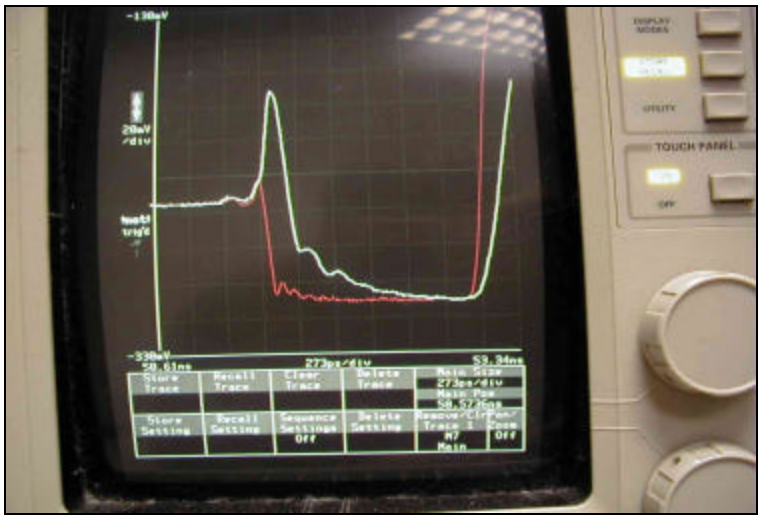

Figure 4 - TDR Using Probe Type A (white) as Compared to Probe Type B (red) Note the Inductive Effects of the Ground (Return Current) Pin have of the TDR

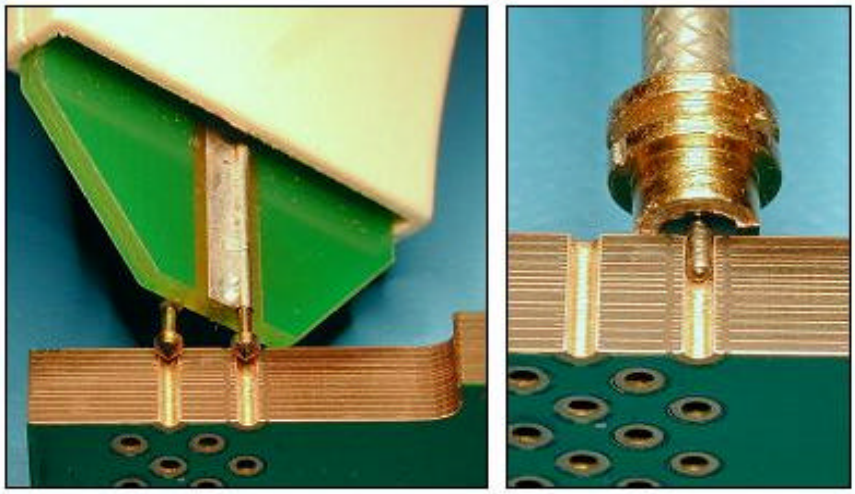

Figure 5 - Test Probes in Coupon (left) – Polar Probe, Useful at about 50ps RT. Single Coaxial Cable (right). Removing the Top Layer of Solder Mast Allows the Use of the Top Plane (Ground Layer) as a Return Signal Path thus Reducing Overall Inductance

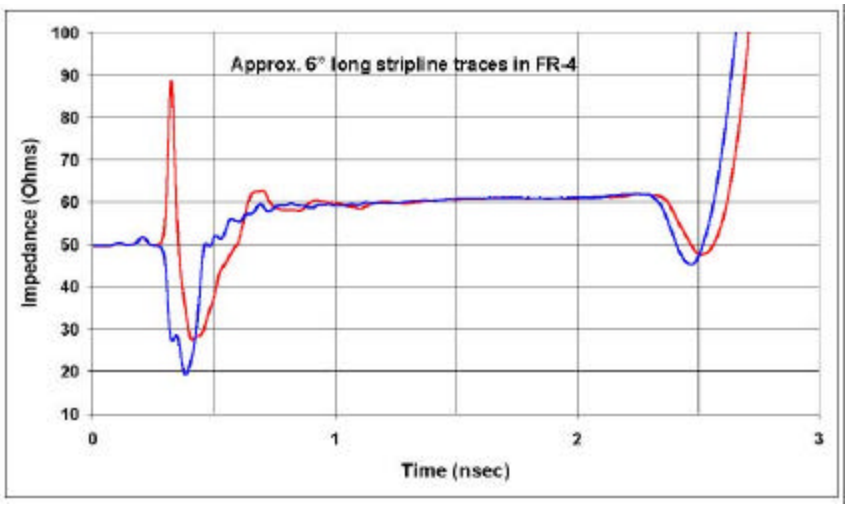

Figure 6 - TDR Response from a Polar Probe (in red) and Single Coaxial Cable (blue). Removing the Top Layer of Solder Mast Allows the Use of the Top Plane (GND) as a Return Signal Path thus Reducing overall Inductance

Inductance associated with the signal /gnd pitch is not the only concern. The mutual inductance and capacitive coupling created by traces running adjacent to one another is another issue. Figure 7 shows a test trace laid out in a trombone fashion over several inches. This structure can lead to a significant amount of crosstalk, which manifests itself as impedance discontinuities. Figure 8 shows the effects of trombone traces on trace impedance. Generally, having traces that run closely adjacent to one another increases the crosstalk of one trace upon another and can give rise to the higher perceived impedance. This is in part a product of the mutual inductance seen between the two adjacent traces relative to the self-inductance of the trace itself.

We can approximate the crosstalk Xm (and hence, some idea concerning the mutual inductance), between two of the adjacent trombone traces as a percentage of the current that is translated from one trace to another, such that $Xm= K*(1/1+ (s/h)^2)$ [1] where s is the separation distance between two traces, h is the height of the trace from the reference plane, and K depends on the rise time and the length of the interfering trace. Separation distance plays a large role as well as the height the trace is from the reference plane, in coupling energy to the adjacent trace. The equation for determining mutual inductance is very similar for determining cross talk of the two adjacent lines, that is, the energy coupled from the aggressor to the victim line is a function of the separation distance, the height of the traces from their respective reference planes, as well as the trace length. The impedance discontinuities are caused by energy that is coupled to the adjacent trace (or traces) from the aggressor. Once the energy reaches the bend of the trombone trace, current that is present in both the aggressor and victim interfere with one another resulting in an impedance discontinuity, thus causing a perturbation in the signal which is reflected back onto the trace itself. This is evident as spikes in the impedance within the TDR waveform. Obviously, a way around this problem is to space the overlapping traces far enough from one another such that the separation distance relative to their height above the reference plane is <1. Another solution would be just not to use serpentine traces for TDR measurements. Obviously the wider the traces and the closer they are positioned to one another the more inaccurate impedance measurements are going to be, relative to the rest of the traces in the PCB.

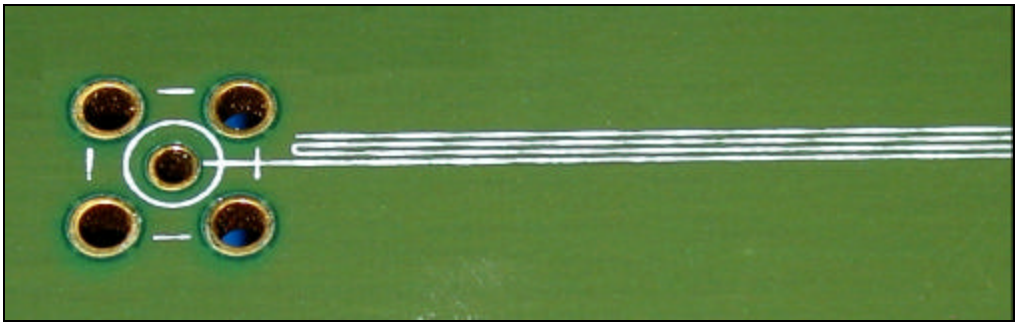

Figure 7 - SMA Launch with 5mil Wide Trombone Traces and a 9mil Pitch

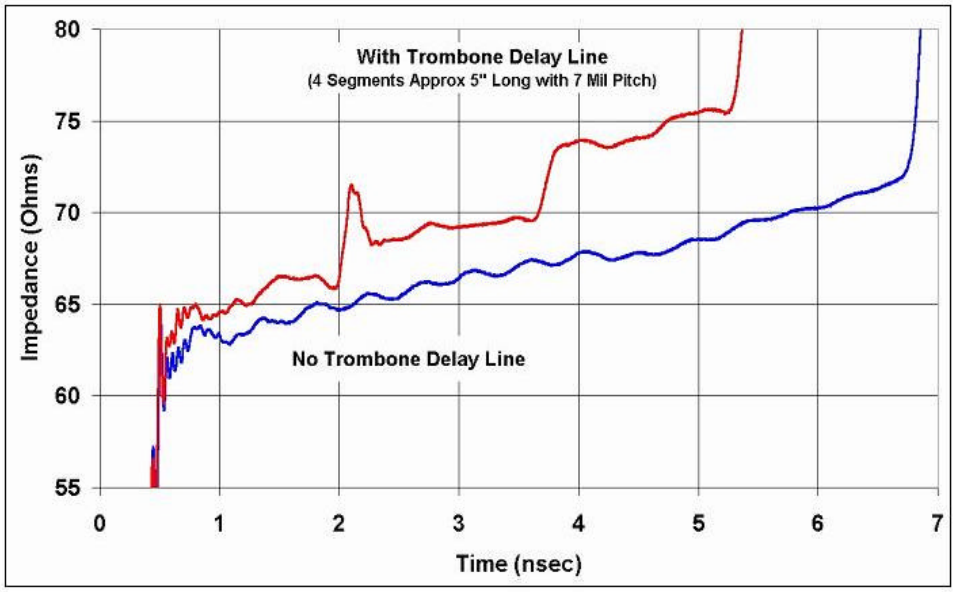

Figure 8 - TDR Measurements Made Across Traces with Overlapping Segments (trombone type layout) Versus no Overlap (straight) Test Trace. Both Absolute and Periodic Impedance is Higher with the Trombone Designed Traces

Optimize Trace Length

One should also be mindful of the trace lengths of the test traces. Realize that DC resistance loss (R_{DC}) and to some extent skin effect losses (R_{AC}), can contribute to significant changes in perceived trace impedance as a function of trace length. A good example of this is seen is Figure 9. Here, the only difference was the trace width. In general, the perceived resistance (really the internal impedance) of the trace is a combination of both R_{DC} and R_{AC} such that the internal impedance, $Zi = R_f + jwL$ [2] where we note that $R_f = R_{DC} + R_{AC}\sqrt{f}\,(1+j)$. Skin effect losses are manifested in $R_{AC.}$ With most trace dimensions in use today, a 40 – 50ps TDR pulse will be fast enough such that skin effect losses will be evident immediately. Note that in Figure 10, as the skin effect component is given greater weight, the slope of the curve follows a form that is a function $\sqrt{f}$. As the length of the trace seen by the TDR step function increases, the resistance is seen to increase. Unfortunately the operation of skin effect loss is immediate in TDR measurements, that is, there is an immediate increase in impedance seen as a function of the pulse response. The only way to effectively minimize contributions of the skin effect component is to launch a step pulse that is below the skin effect cutoff frequency. This frequency can be found by calculating the skin depth of the trace, which is dependent of the trace thickness. Of course, this is typically not done for the simple reason that most measurements will want to be made at a RT that is representative of the signal that will be operational on the board. Be aware that this effect is most dramatic on very narrow traces, such as 3 to 5mils.

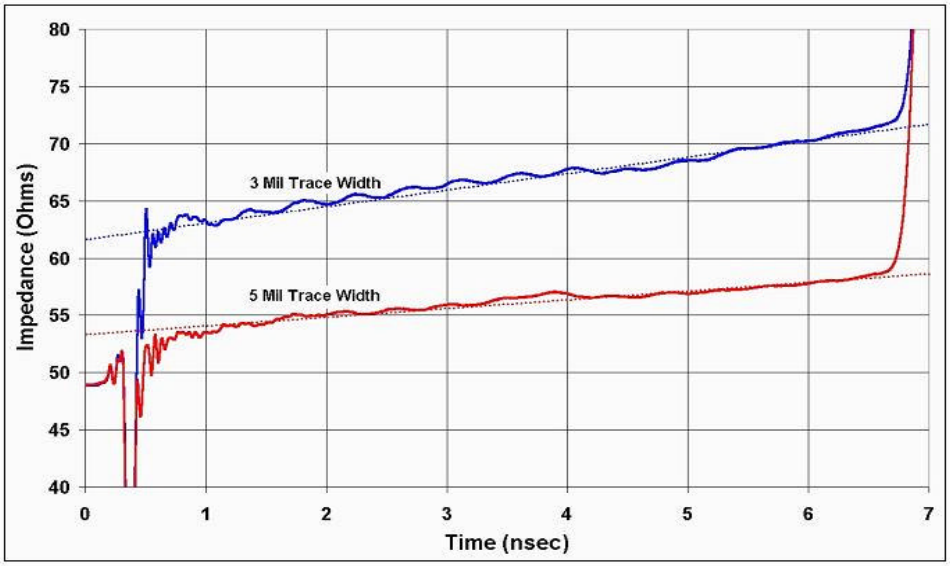

Figure 9 - TDR Measurements Made Comparing 3 and 5mil Trace Widths. Note the Higher Initial Impedance Due to Skin Effect Loss. The 3mil Trace Width also has a Higher Rate of Impedance Change

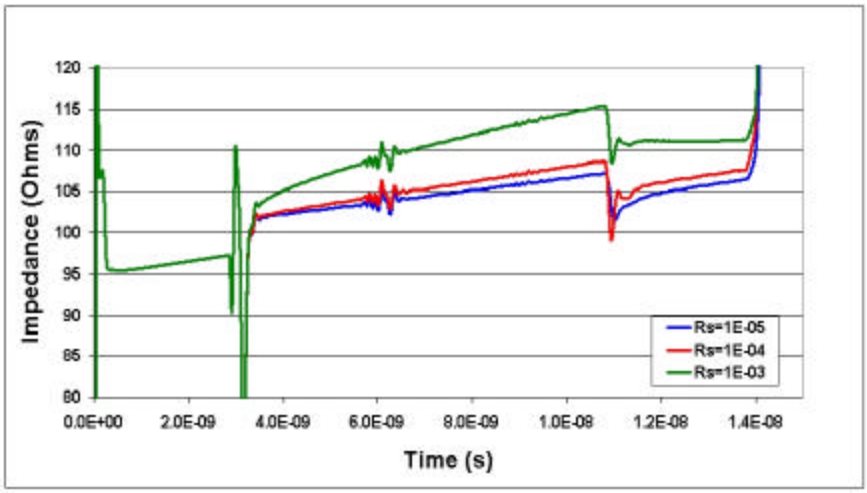

Figure 10 - Three Different Levels of Skin Effect Loss Showing the Contribution to Impedance Changes. Rs Measured in Units of $\Omega/m^*\sqrt{Hz}$

The other important component is the DC resistance, which with longer traces can have a dramatic effect on the trace impedance. Since the DC resistance increases the length increases, the effects are not immediately seen. Referring again to Figure 10, in the case where the skin effect impedance has not been given that much weight, the impedance rise is almost solely a function of the DC resistance. In reality a trace has both skin effect and DC resistance (as well as dielectric loss). Note also that the slope of the impedance trace is larger for the 3mil trace vs. the 5mil trace showing that for every incremental increase in length corresponds to greater increase in impedance. A good check to see how much the impedance will rise is to calculate the DC resistance either manually, or with a 2-D field solver, accounting for the length of the trace, and adjust the output impedance accordingly. This is just a general rule. A more definitive result in achieved through the use of a parametric model, like a W element used in one of the available SPICE type solvers. The reality is that both AC and DC resistance loss will be a factor in contributing to overall impedance increases. Being mindful of the DC losses will go a long way in correctly representing the impedance.

One other note about trace lengths is to be mindful of the length of the cable used to probe the test trace. Any impedance discontinuities between the TDR sampling head and the probe cable can show up anywhere along trace if the cable length is less than the trace length being measured. As an example, in Figures 10 and 11 the launching impedance at the probe head has been made such that there is a discontinuity between the sampling head and cable. This can be a problem if the cable is bad, or the connector is dirty or faulty. As such, there is a visible perturbation that looks to be from the trace but in fact is an artifact of the launch structure. Note two things about the discontinuity: 1) It is an aberration caused by the impedance discontinuity of the via, energy that bouncing back and forth between the via and probe head, and 2) its contribution looks worst as the RT of the TDR is shortened. The fact that you do not see the discontinuity with slower RT shows the veracity of the problem, and how it can be masked. It is easy to remedy this problem by using good cables with quality SMA or 3.5mm fittings and cables that are longer than the traces being measured

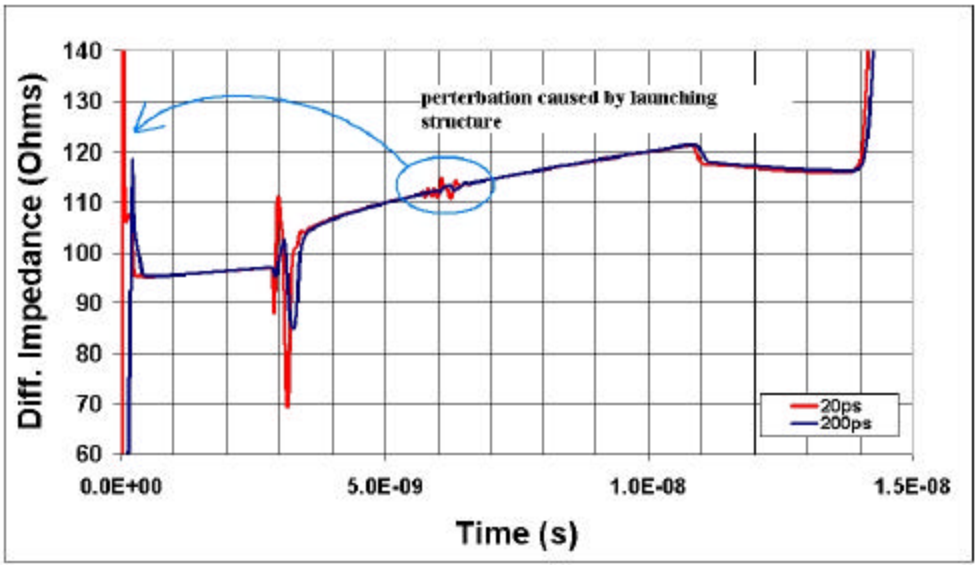

Figure 11 - Two TDR Responses from a 20 and 200ps RT Step Signal. Note the Differences in the Features of the Launch Via and the Discontinuity is the Middle of the Trace Caused by Back Reflections Between the Launch Via and the Connector. For the RT of 200ps, the Anomaly is not Present

Minimize via Transitions

Vias are quite abundant on most PCB's and their incorporation as a launching point to traces within the board is usually imperative. This being said, further transitions through multiple vias should be avoided unless the designer is trying to characterize the vias effects on the propagation or impedance through the board. Aberrant results such as those noted on Figure 12 are quite common with ANY trace moving through via structure, irrelevant of the trace width or its thickness. It is interesting to note that not only will the impedance change through each via transition, but the propagation delay increases as well, and not just because of the length of the via, but because of the inherent per unit length capacitance (C), and inductance (L) of the via itself. At a sufficiently high frequency, the total delay (Td) through the via can be approximated as Td = $\sqrt{LC}$. The effect of this in the figure, is that the pulse slows as it transitions though each via, which leads to a spreading, or smearing effect of the TDR pulse and it decreases the ability of the instrument to resolve finer features of impedance variations along the trace. This is evident as the impedance discontinuity due to the vias are present in the beginning of the waveform and are almost completely absent toward the end. The slowing down of the pulse and the distortions created by moving through the via structure is dependent upon the geometric structure of the via. It better to launch off of a via which

has been tuned to the characteristic impedance of the trace (usually 50 to 60 ohms) or simply use a pad if the trace is a microstrip structure. Ultimately, it is difficult to arrive at any via structure that has the same characteristic impedance of the trace being measured, therefore, expect some discontinuity between the via and the trace.

The location of the test trace within the PCB stackup is another important factor in designing test traces. Positioning test traces near the top of a via, effectively not using a large portion of the via can lend itself to more perturbations due to via "stub effects". These effects are prominent, as seen in Figure 13, where the via discontinuity causes initially, a decrease in the measured impedance due to the via, and then further discontinuities down the trace. The discontinuity is a manifestation of current which has traveled down the via barrel, reflects off of the end of the barrel, and is subsequently injected back into the system and is seen as a pulse of energy somewhere toward the end of the trace measurement. Utilizing the full length of the via can minimize the stub effects if they are a concem, especially if one suspects that they could be contributing or covering up other problems within the trace geometry. If traces must be placed on layer very near the top of the board, a simple way to utilize the full length of the via may be just to turn the board over and measure the from the backside, assuming the launching signal and ground are through vias. Another alternative may be to use two through vias in sequence, where one via goes through the board and then is attached to the adjacent via through a small trace, then the second via moves up to the position the test trace. Still another method would be to drill down only to the trace of interest. While this third option gives the best results, it is also the most expensive from a manufacturing standpoint.

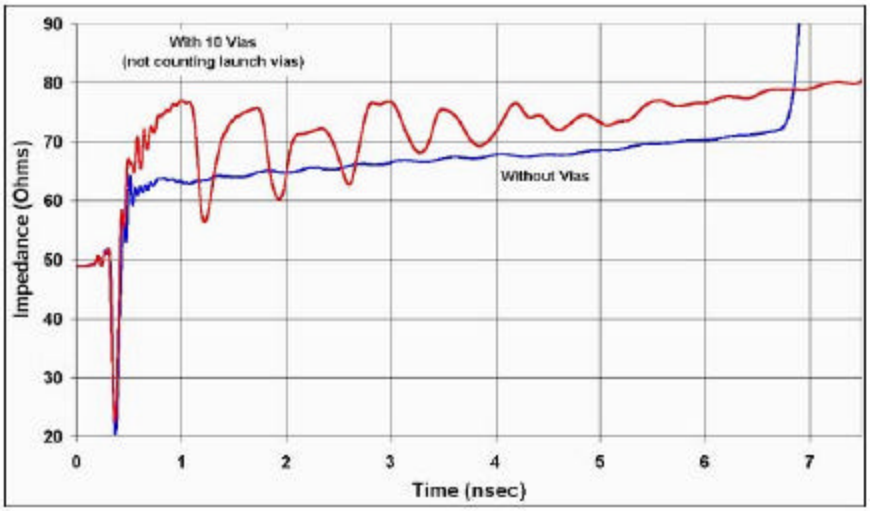

Figure 12 - TDR Measurements Made Comparing Test Traces with 10 Vias in the Signal Path Versus no Vias in the Signal Path. An Obvious Improvement in Trace Impedance Characterization is Seen with no the Removal of Vias in the Signal Path

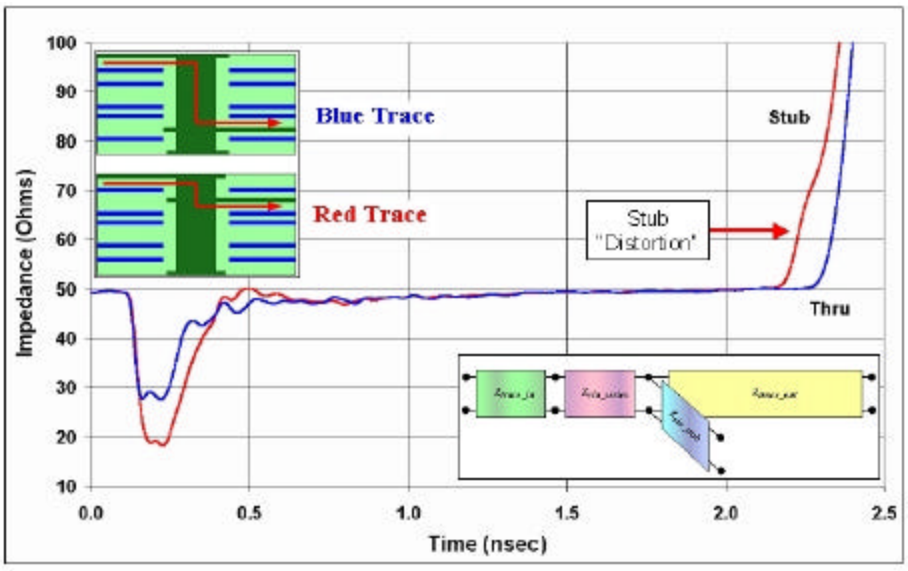

Figure 13 - Two TDR Responses from a 6-inch Long 50-ohm Stripline on Layers 2, and 18 in a 21 Layer Test Coupon, Made Using FR-4 Material

Conclusion

What can be said is that specific trace design needs to follow function. If concerns over vias and or other mechanical structures are an issue within the PCB, it may be warranted to design a test trace incorporating these features, but these features should be eliminated or otherwise minimized if direct impedance measurements of the trace itself are desired. Be aware of the test trace dimensions, as a function of the TDR's RT and the DC resistance as they may to various degree, be a contributing factor in perceived impedance.

Summary

Please keep the following items when designing or measuring impedance test traces or coupons:

1. Provide a short return current path between the test signal and gnd via (or pad). A nominal distance is about 80 –100mils.
2. Place all traces as a single strip. Do not fold traces over adjacent to one another unless you are specifically looking to understand how this geometry affects signal impedance and delay. Along the same lines, avoid placing vias or other structures not directly related to the test trace close to the trace itself, such that it will effect the return current path and thus the impedance.
3. Be aware that the impedance tends to rise on TDR waveforms as a function of trace length. How fast the impedance changes is a function of trace width and thickness. For narrower traces, use shorter trace lengths, possibly on the order of three to five inches.
4. Through vias, which are used as launching structures, should be fully utilized. Avoid via "stub structures" where possible.
5. Use quality test cables and connectors. Ensure that test cables are at least as long as or longer than the trace segments being tested.

References

1. Johnson H, Graham M. High–Speed Digital Design. Prentice Hall: Upper Saddle River, NJ; 1993.
2. Ulaby, Fawaz T. Fundamentals of Applied Electromagnetics. Prentice-Hall: Upper Saddle River, NJ; 1999.

SANMINA-SCI

Optimal PCB Trace Design for Improved Quality Control

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Agenda

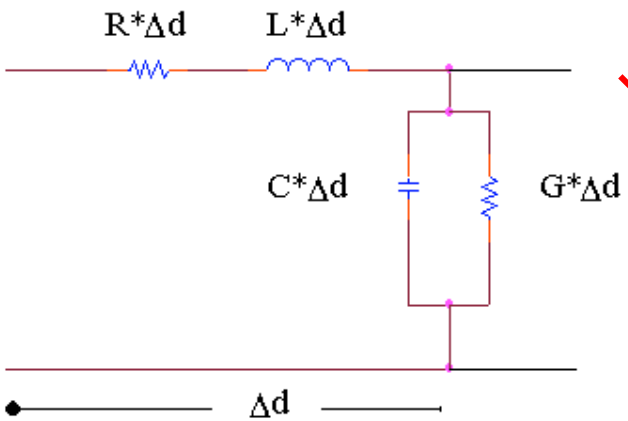
- Introduction
  - Function of test traces
  - TDR signal approach
  - Typical test coupons
- Issues with TDR probes
  - Probe lead inductance
  - Signal / Gnd pitch
  - Bandwidth limitations
- Examples of Bad Test Trace Design
  - Trombones
  - Via placement
  - Via stubs
- Other Issues
  - Skin Effect
  - Cable length
- Summary

Some Purpose of Test Traces

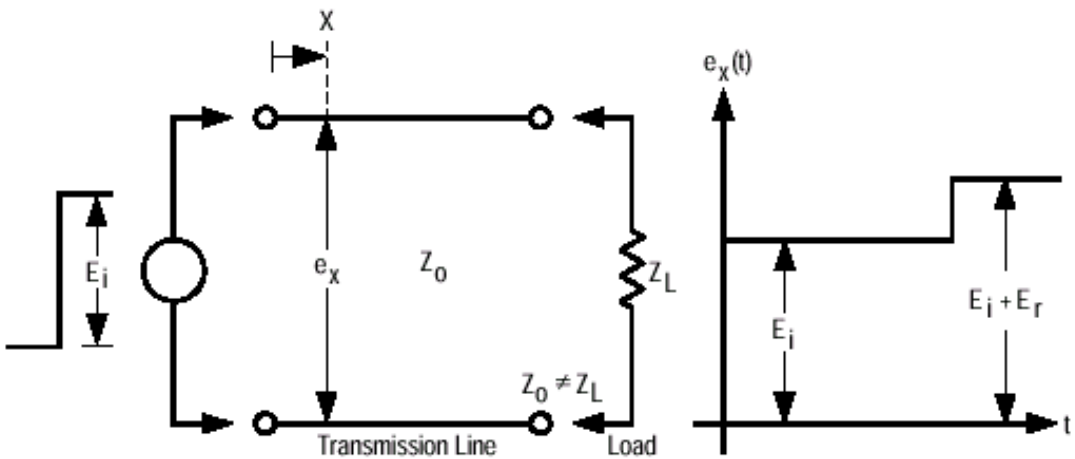
- Check of Trace Impedance constraint
- Check of trace lengths
- Verification of overall manufacturability
- Verification of dielectric quality
  - Know length, can verify ε_r given prop delay**

***well, sort of*

TDR Operation: Reflection Coefficient from an Input Step



$$Z_O(\omega) = \sqrt{\frac{(R + j\omega L)}{(G + j\omega C)}}$$

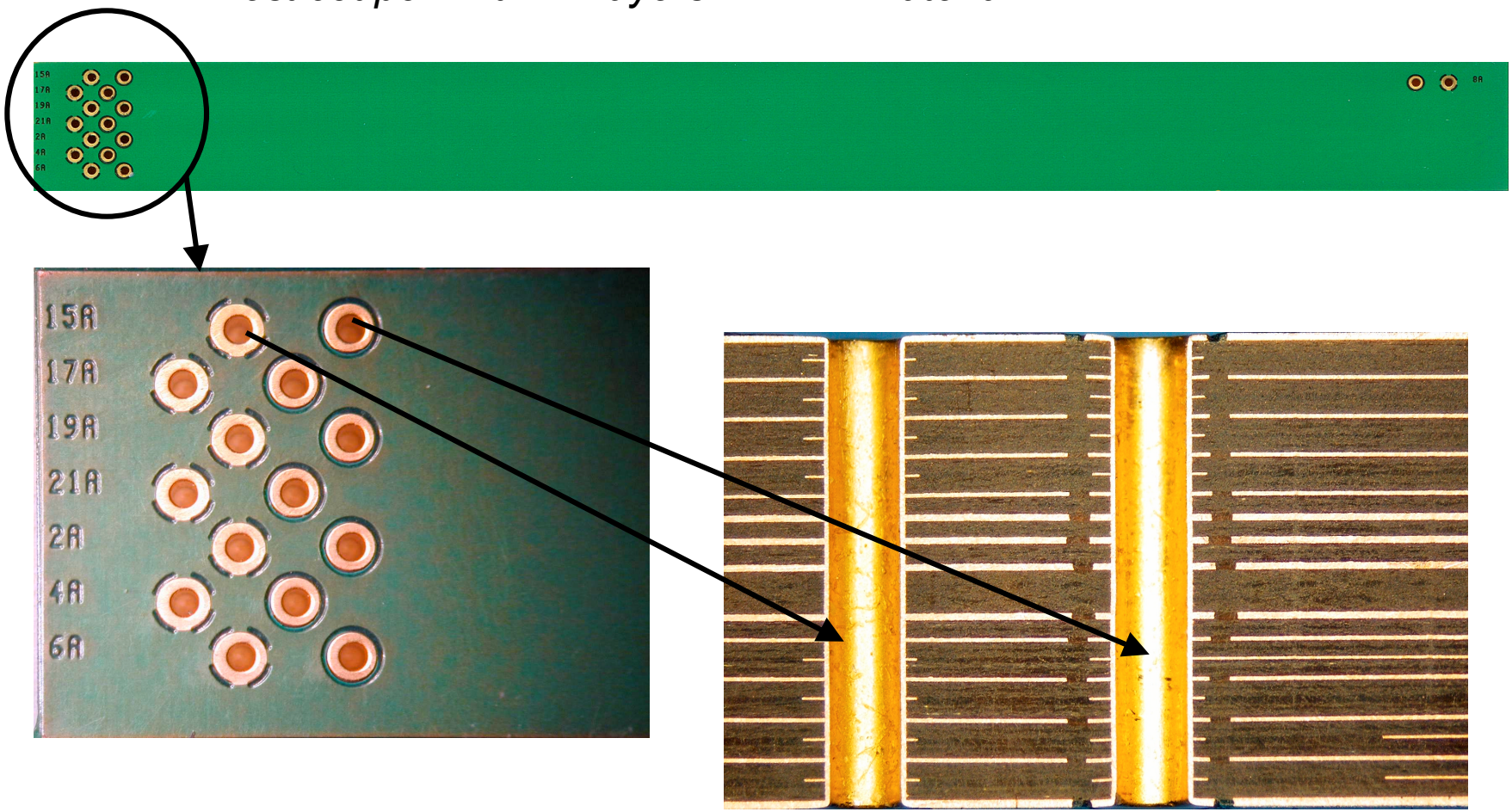


$$\Gamma_L = \frac{E_i}{E_r} = \frac{V^-}{V^+} = \frac{Z_L - Z_O}{Z_L + Z_O}$$

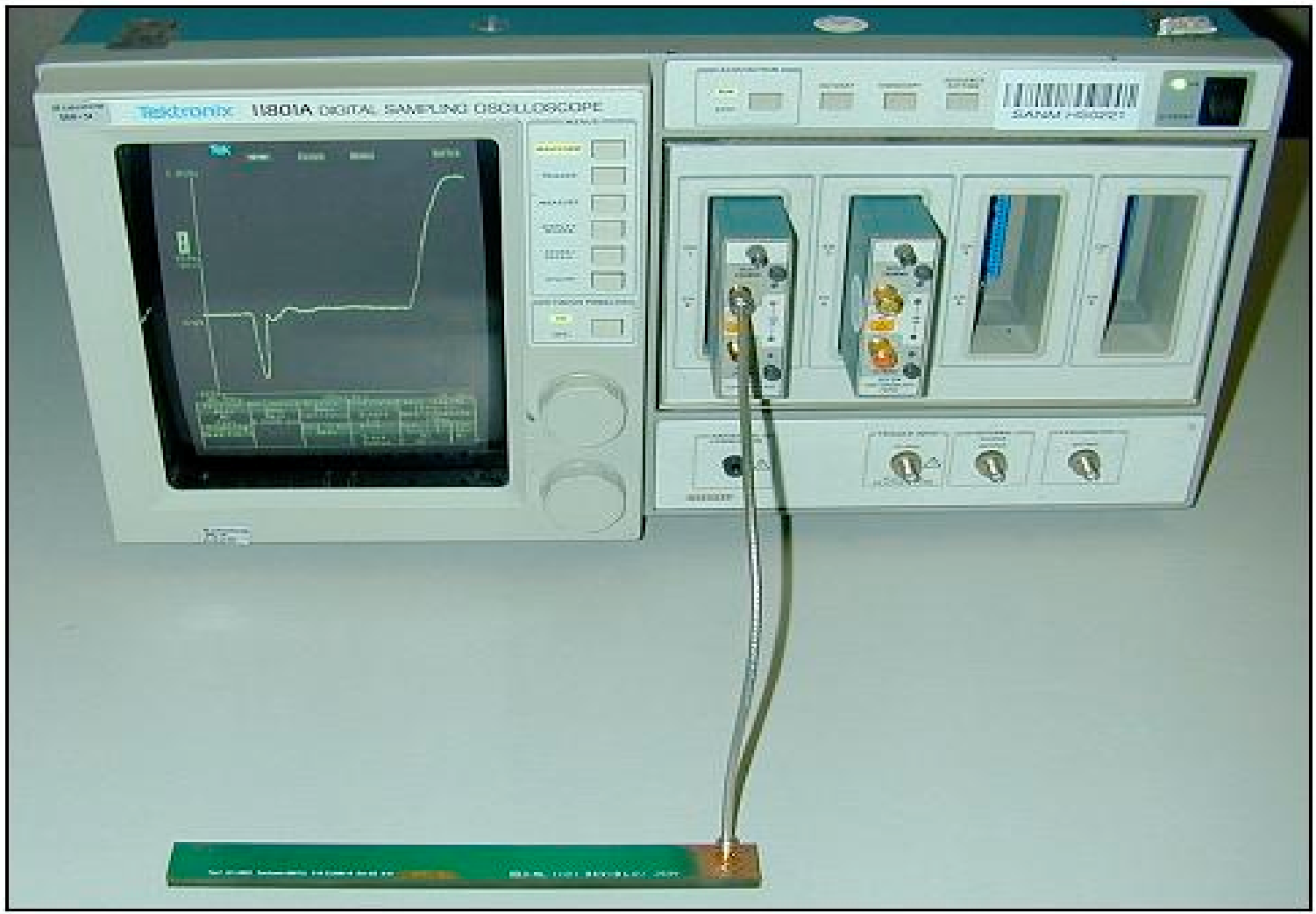
$$Z_L = Z_O \frac{1+\Gamma}{1-\Gamma}$$

Test coupon and Via structures

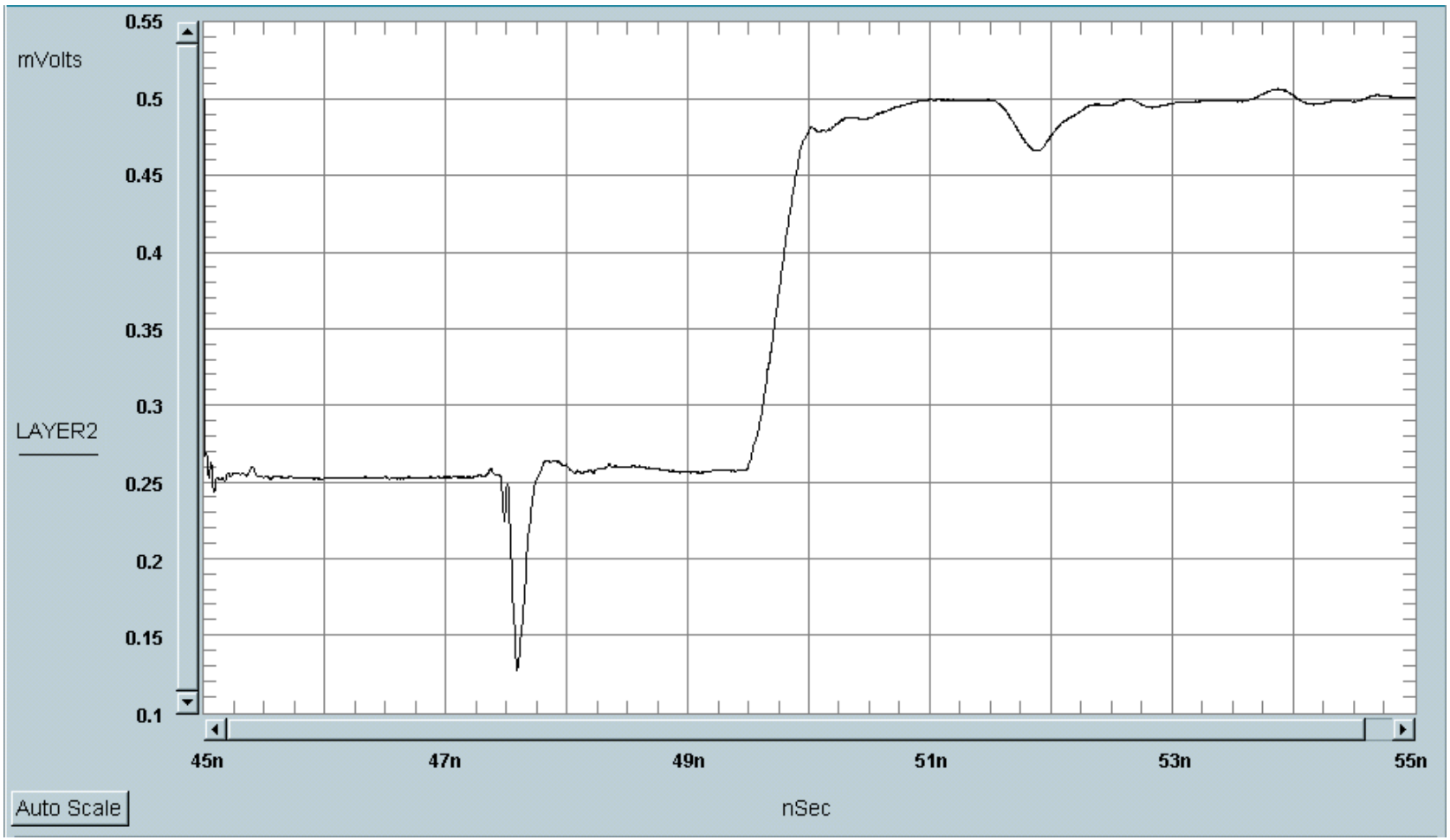
Test coupon with 22 layers in FR-4 material



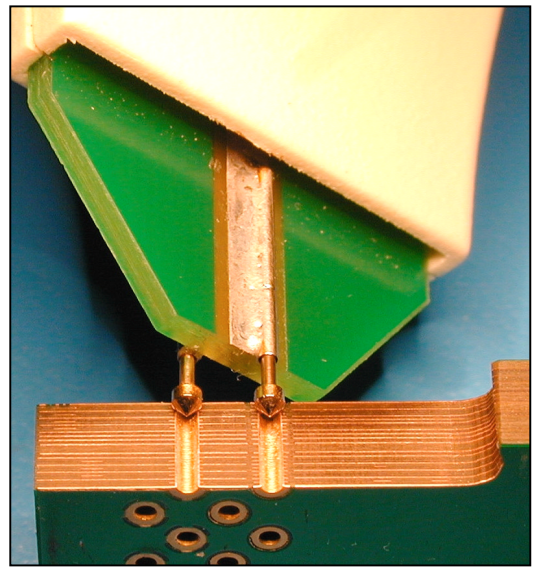
Typical TDR setup



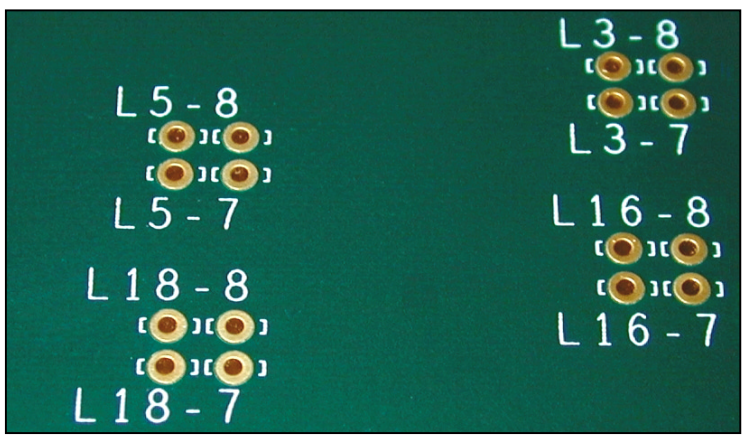
Sample TDR Measurement

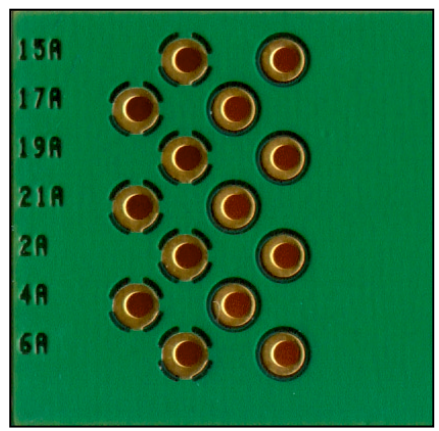


Standard Test Probes and Points



Backplane Test Points

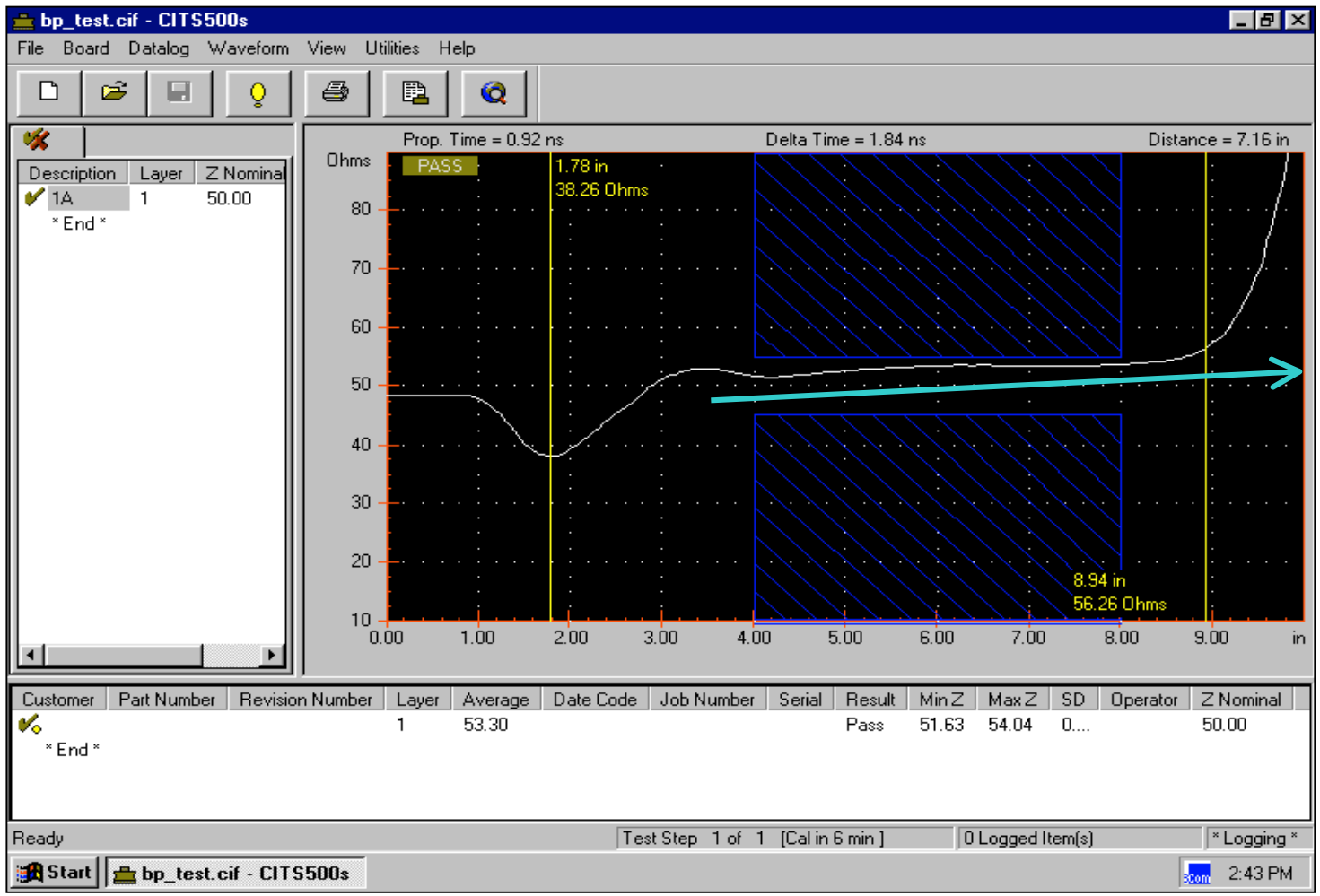




Coupon Test Points

Sample TDR Measurements

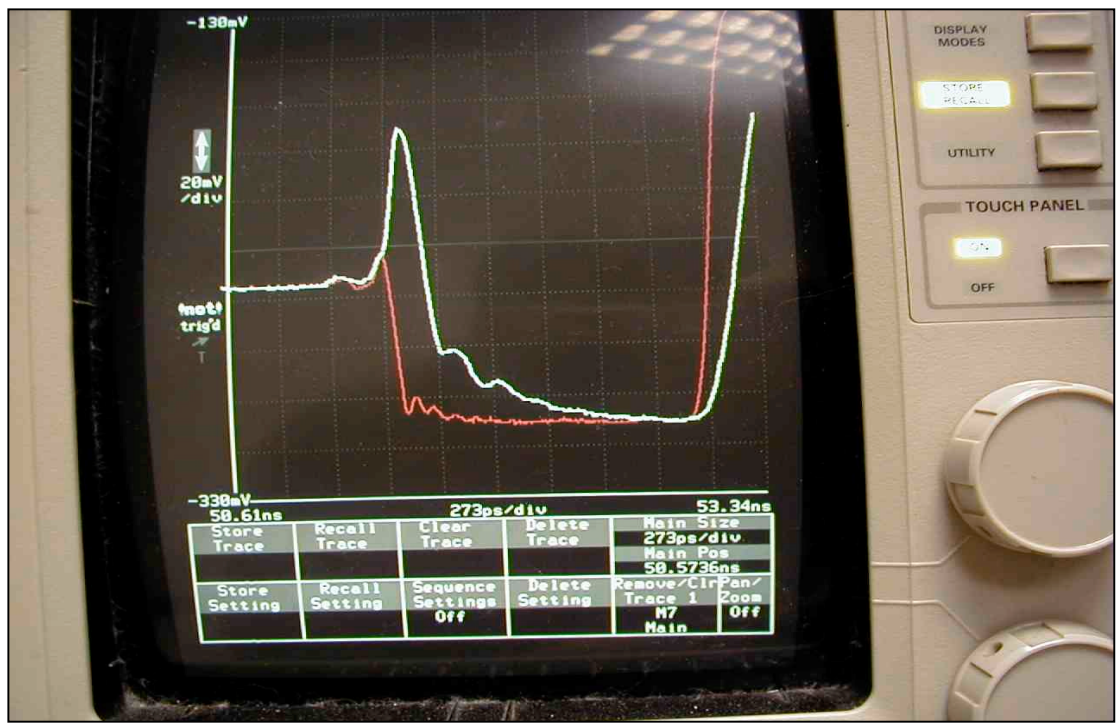
- *Test board response - note slight elevation in impedance, inductive "bump"*



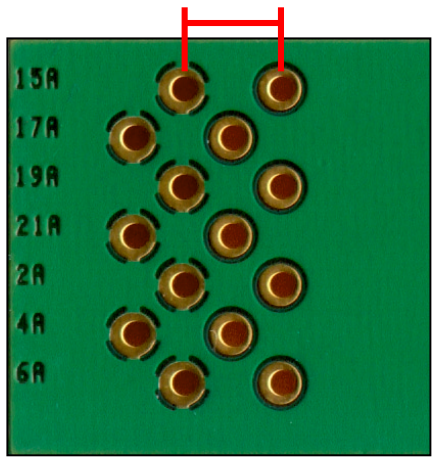
Comparison of TDR probes: Lead Inductance - part I

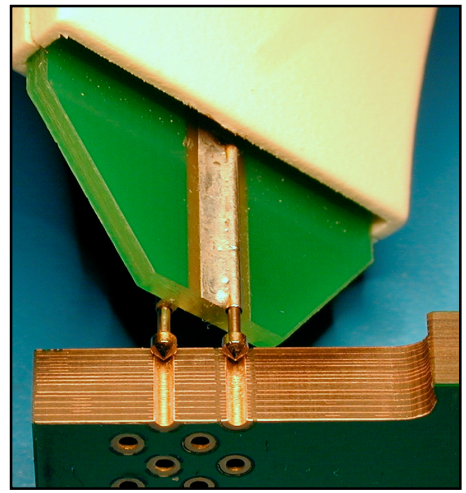
This :
(White Trace)

Versus This:
(Red Trace)

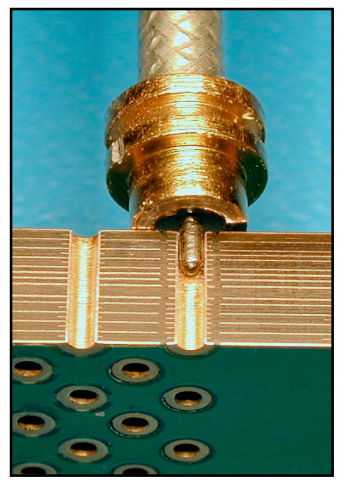


Comparison of TDR probes: Lead Inductance - part II

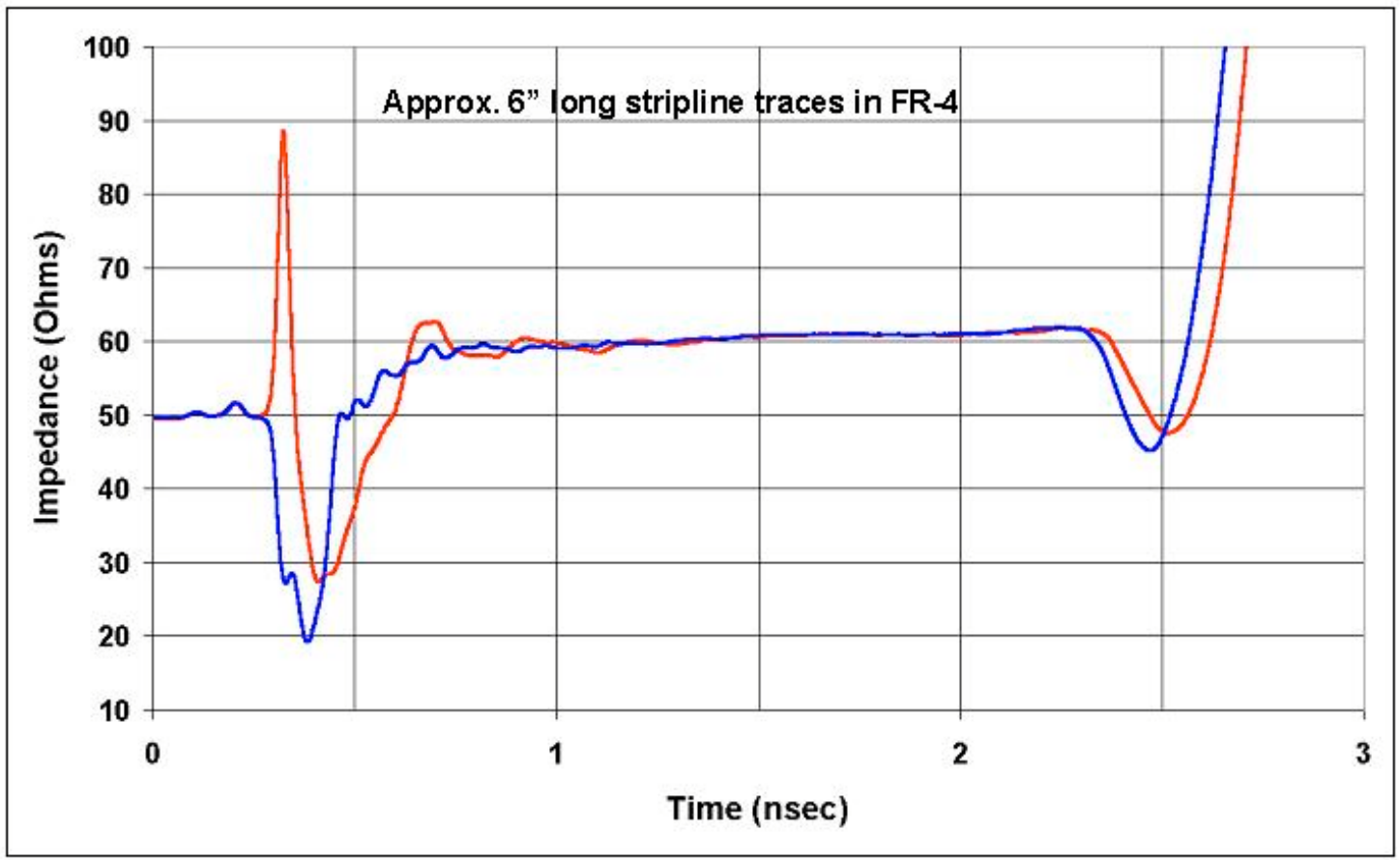




Much less here

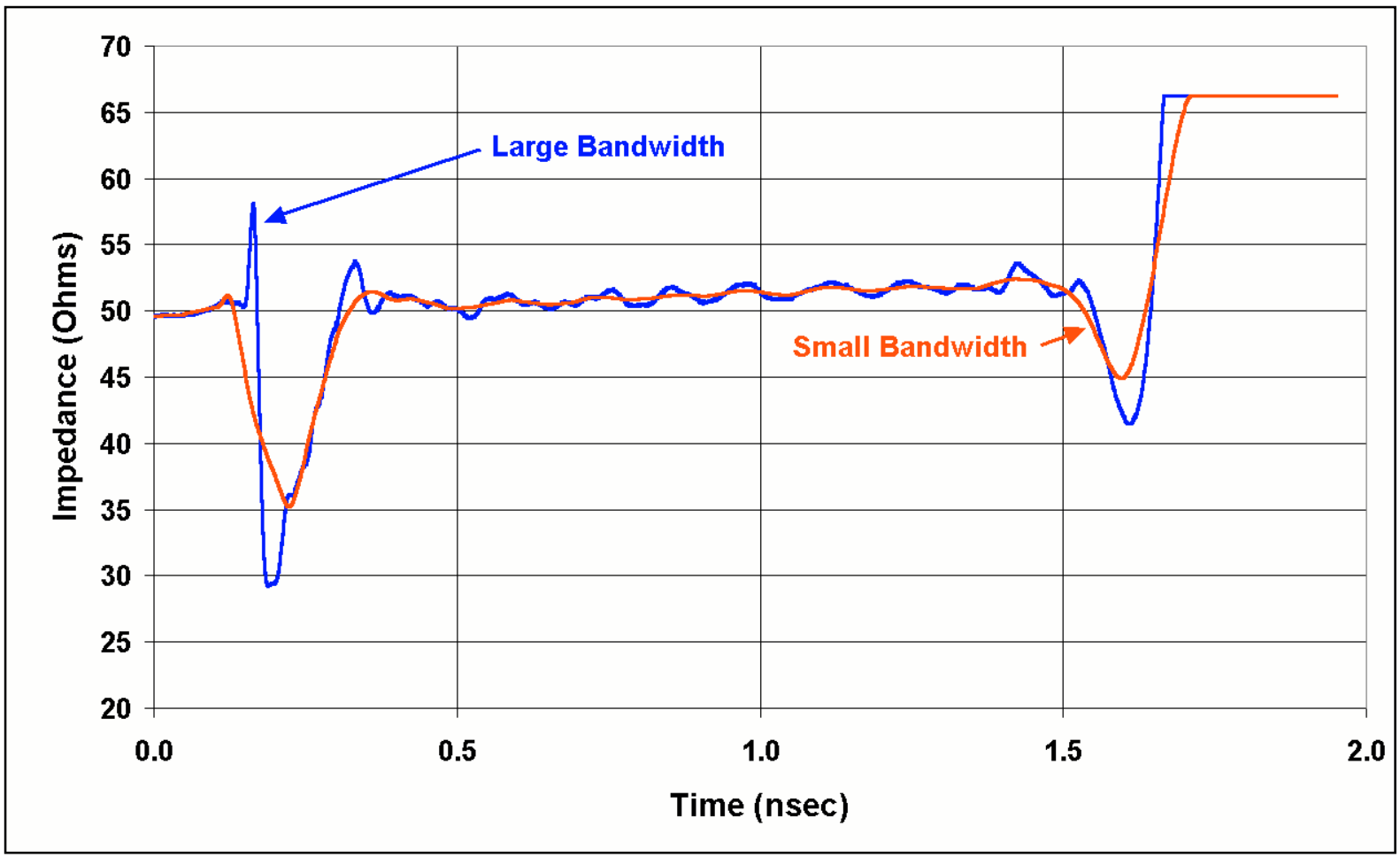


Comparison of TDR probes: Lead Inductance - part II



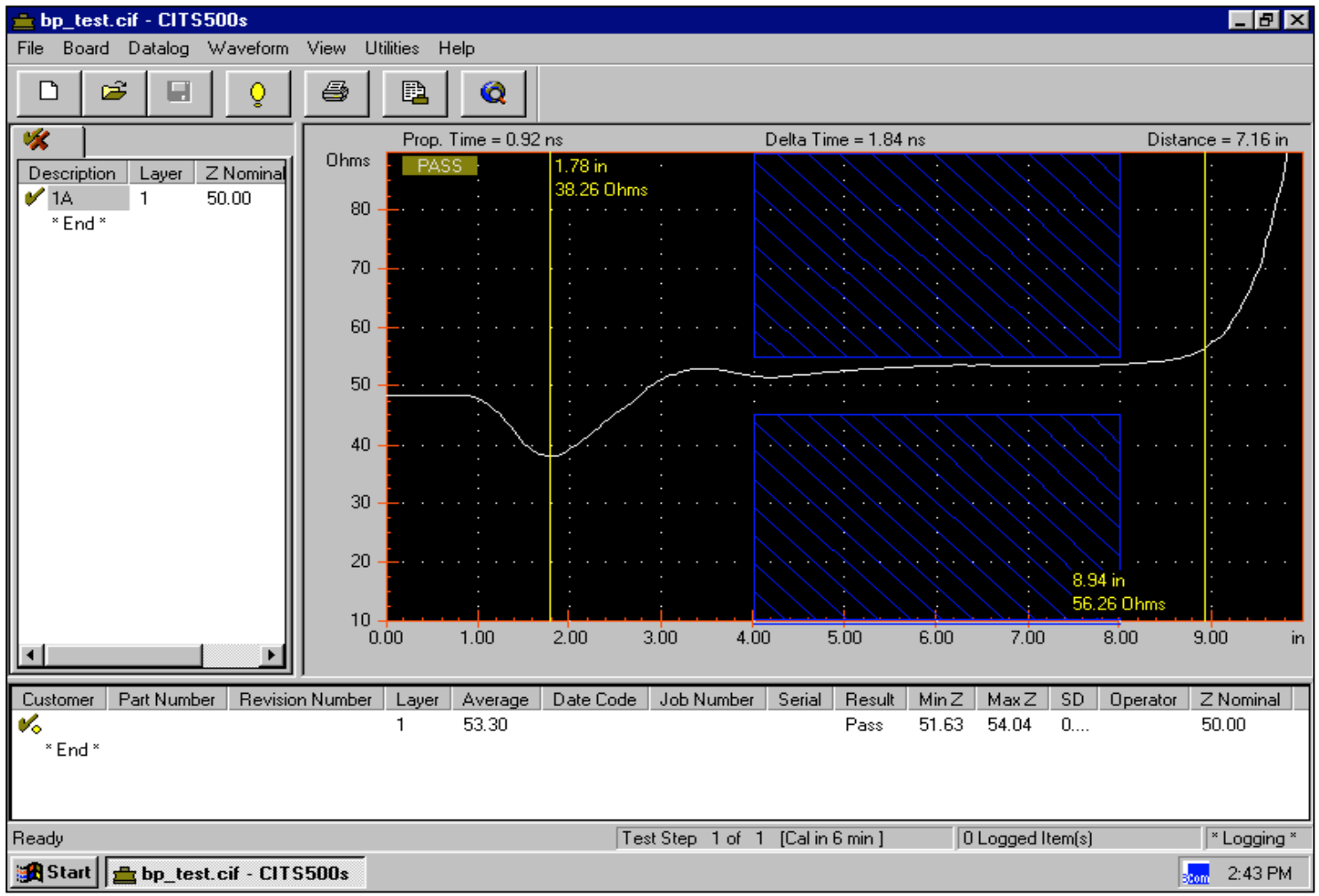
Comparison of TDR probes: Large vs. Small bandwidth

Be aware of the settling time and artifacts that may arise ∝ RT



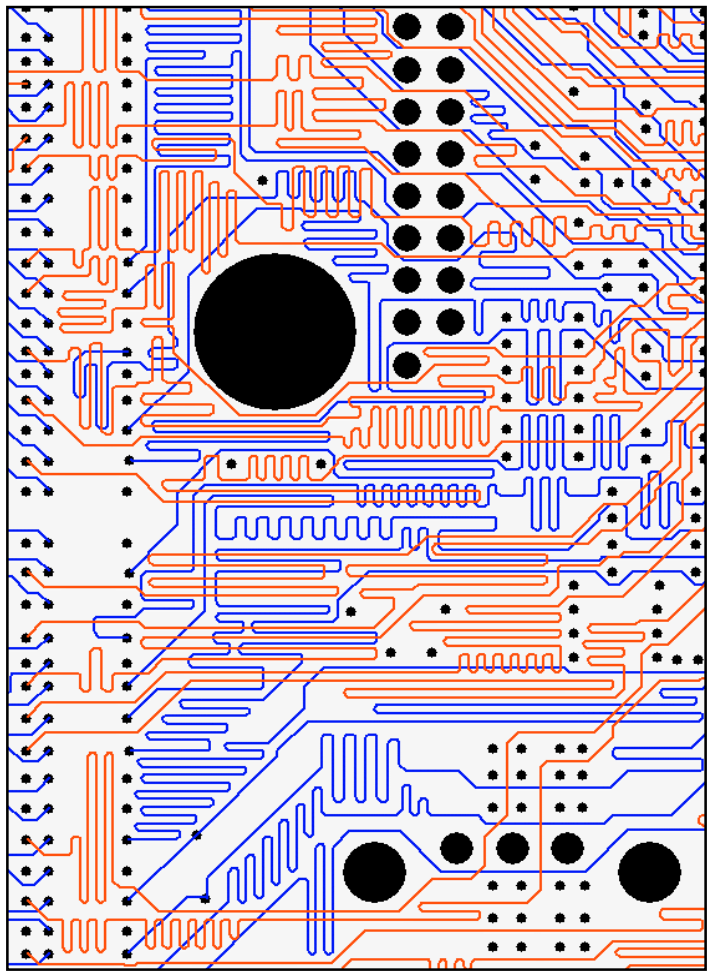
Sample TDR Measurements

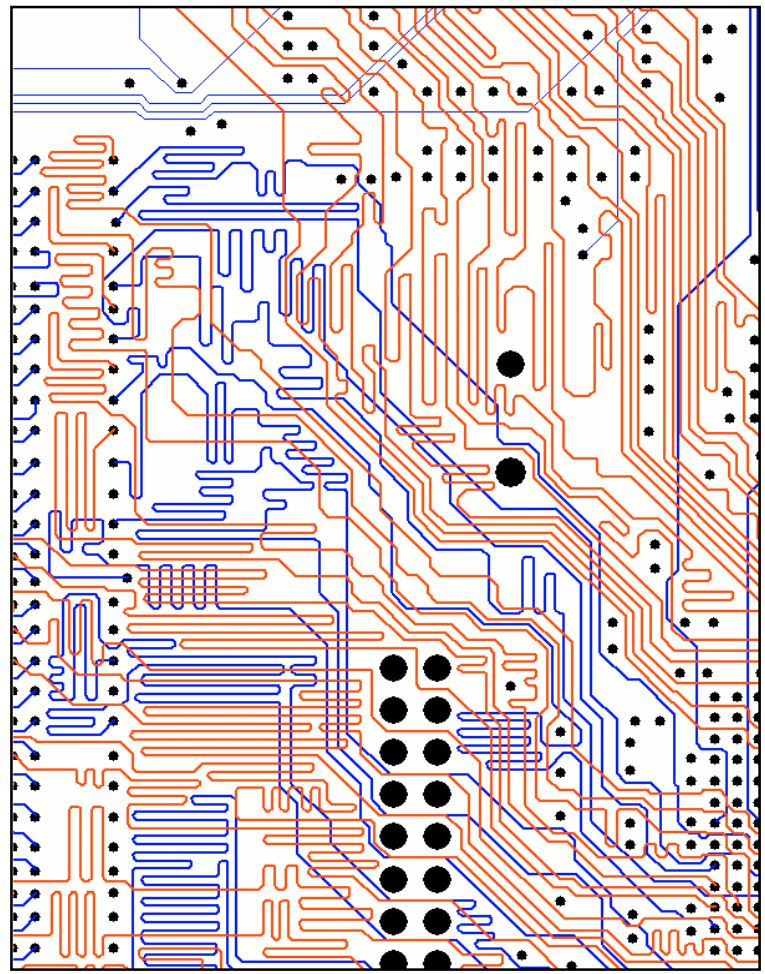
- *Fairly slow rise time - on the order of 300ps*



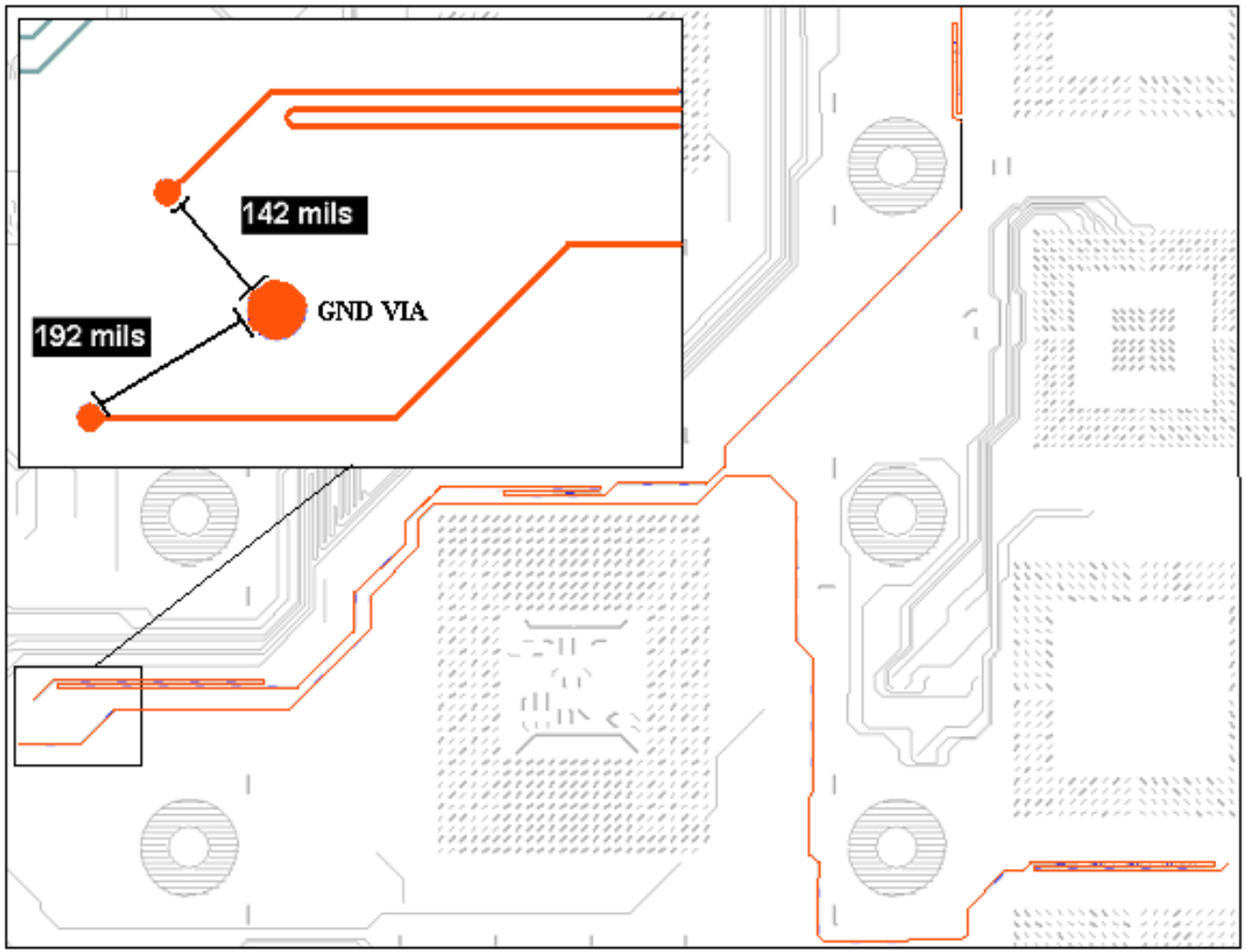
Examples of Trombone and Accordion Delay Lines

Realize the limitations of placing test traces within a given stackup



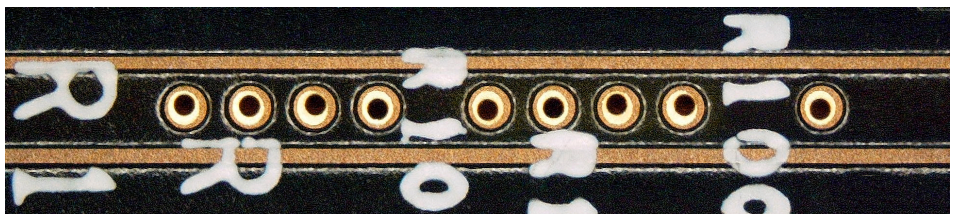


Non-Uniform Test Point Contact Dimensions

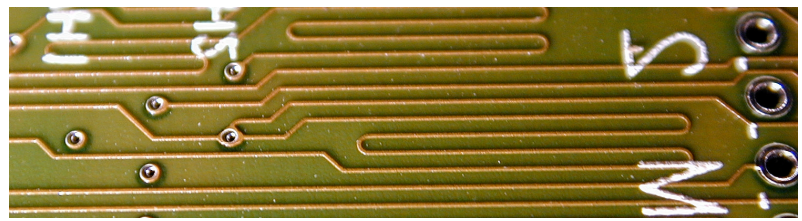


Typical Don’ts in Designing Test Traces

Vias



Trombone

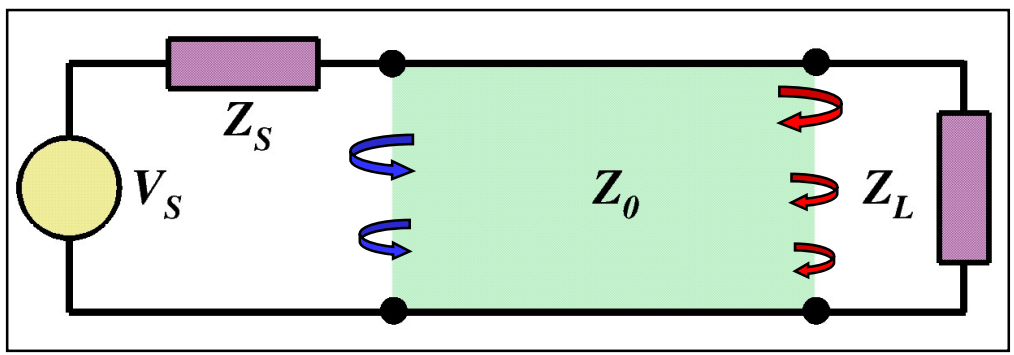


$$\Gamma_{\text{Source}} = \frac{Z_S - Z_0}{Z_S + Z_0}$$

$$\Gamma_{open} = +1$$

$$\Gamma_{short} = -1$$

$$\Gamma_{matched} = 0$$



$$\Gamma_{Load} = \frac{Z_L - Z_0}{Z_L + Z_0}$$

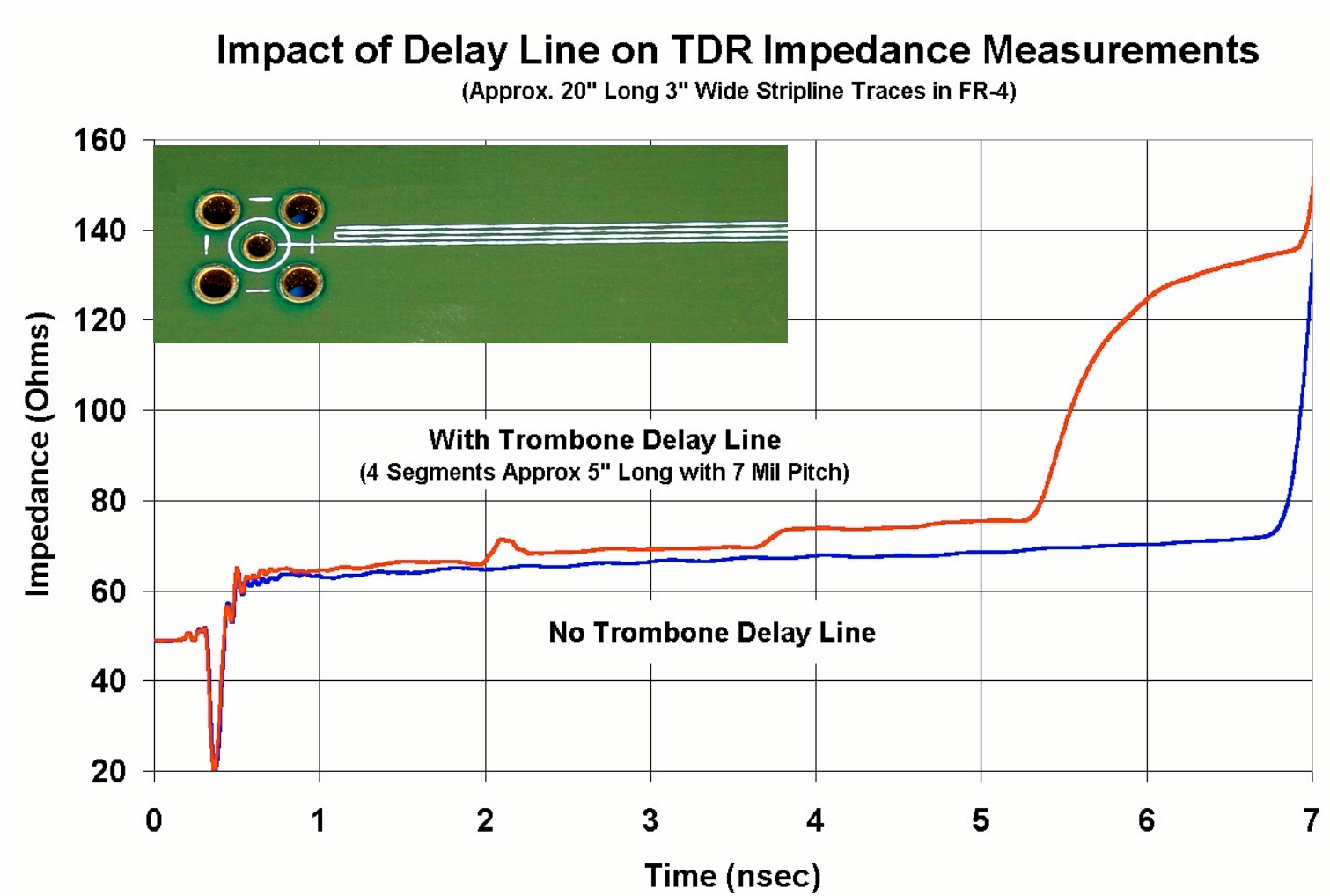
$$\Gamma_{open} = +1$$

$$\Gamma_{short} = -1$$

$$\Gamma_{matched} = 0$$

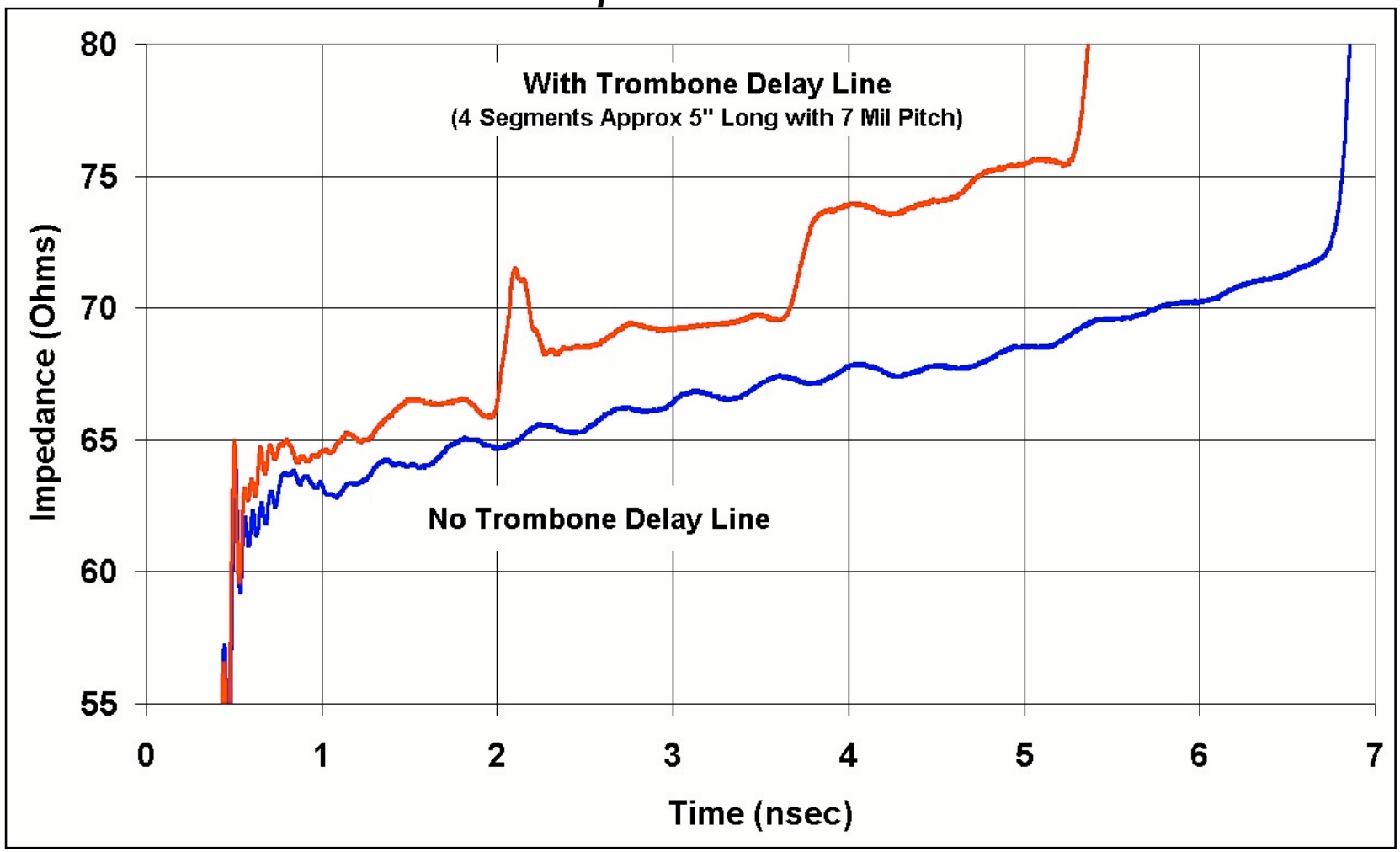
- **If $Z_S \neq Z_0 \neq Z_L$ then energy gets trapped between the impedance mismatch points.**

Impact of Trombone Delay Line on TDR Measurements



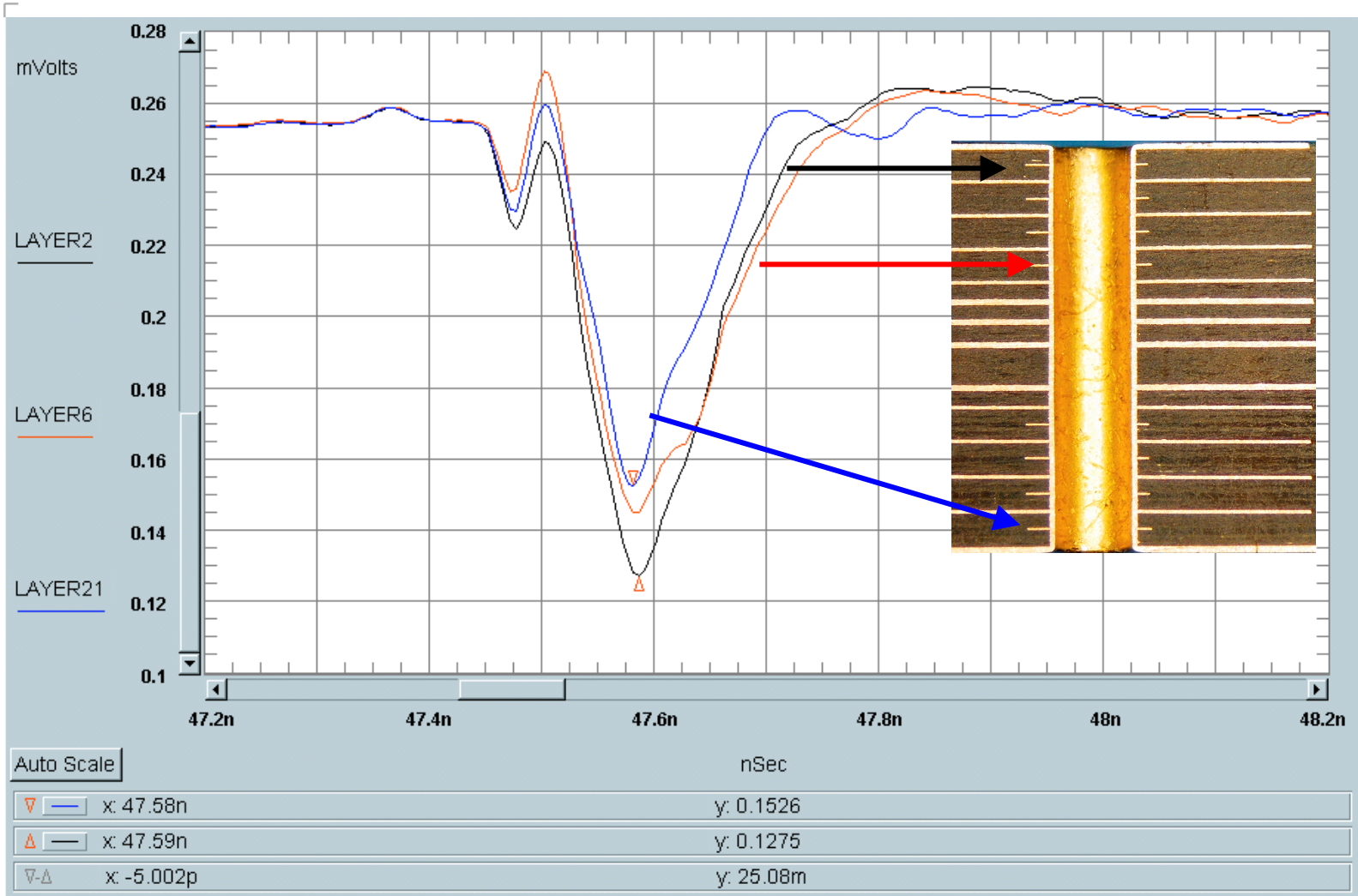
Impact of Trombone Delay Line on TDR Measurements (Detail)

3 mil wide stripline trace in FR-4



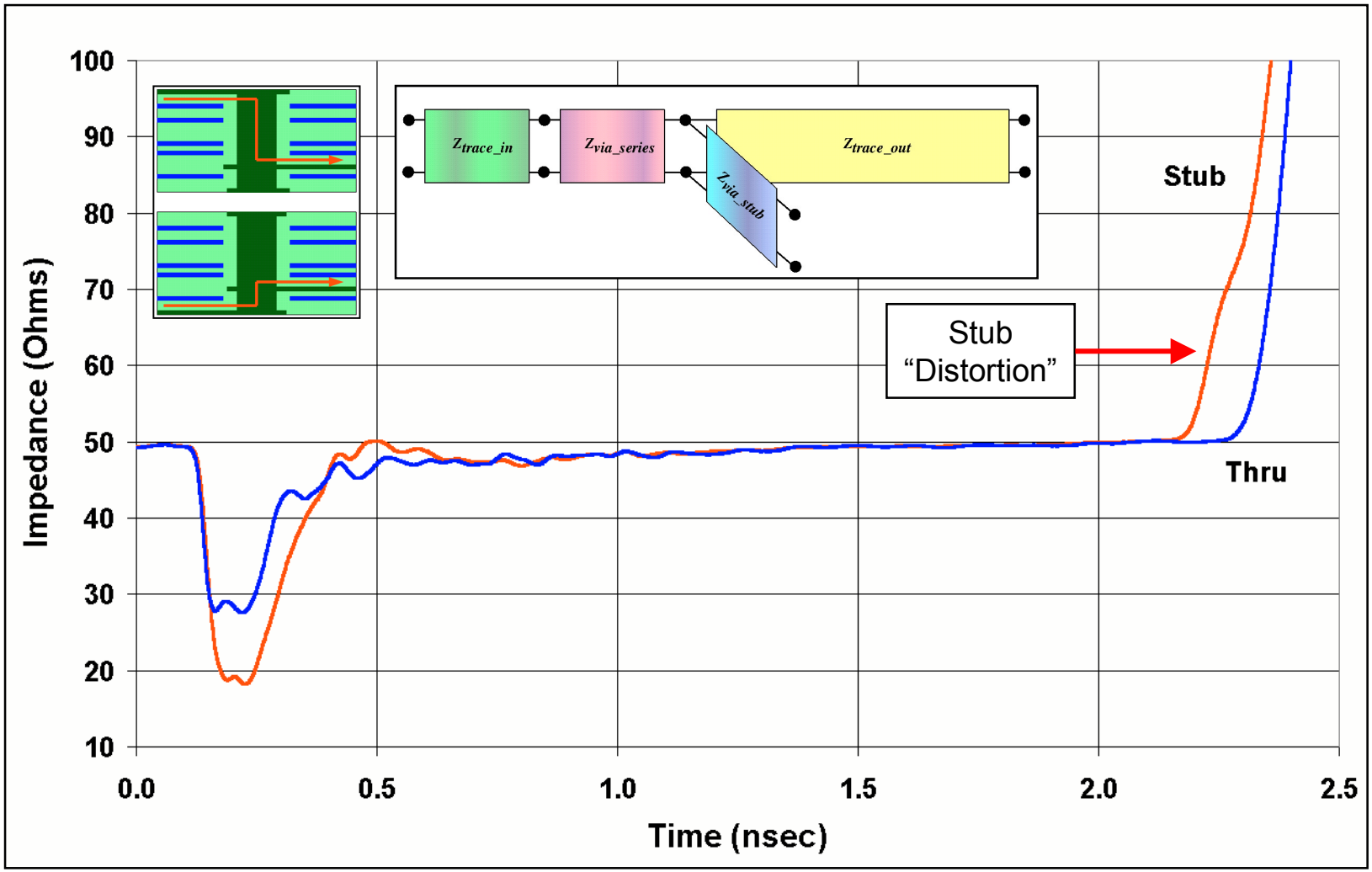
Via Stub Effects (Time Domain)

At high frequencies vias behave like series/shunt transmission line stubs

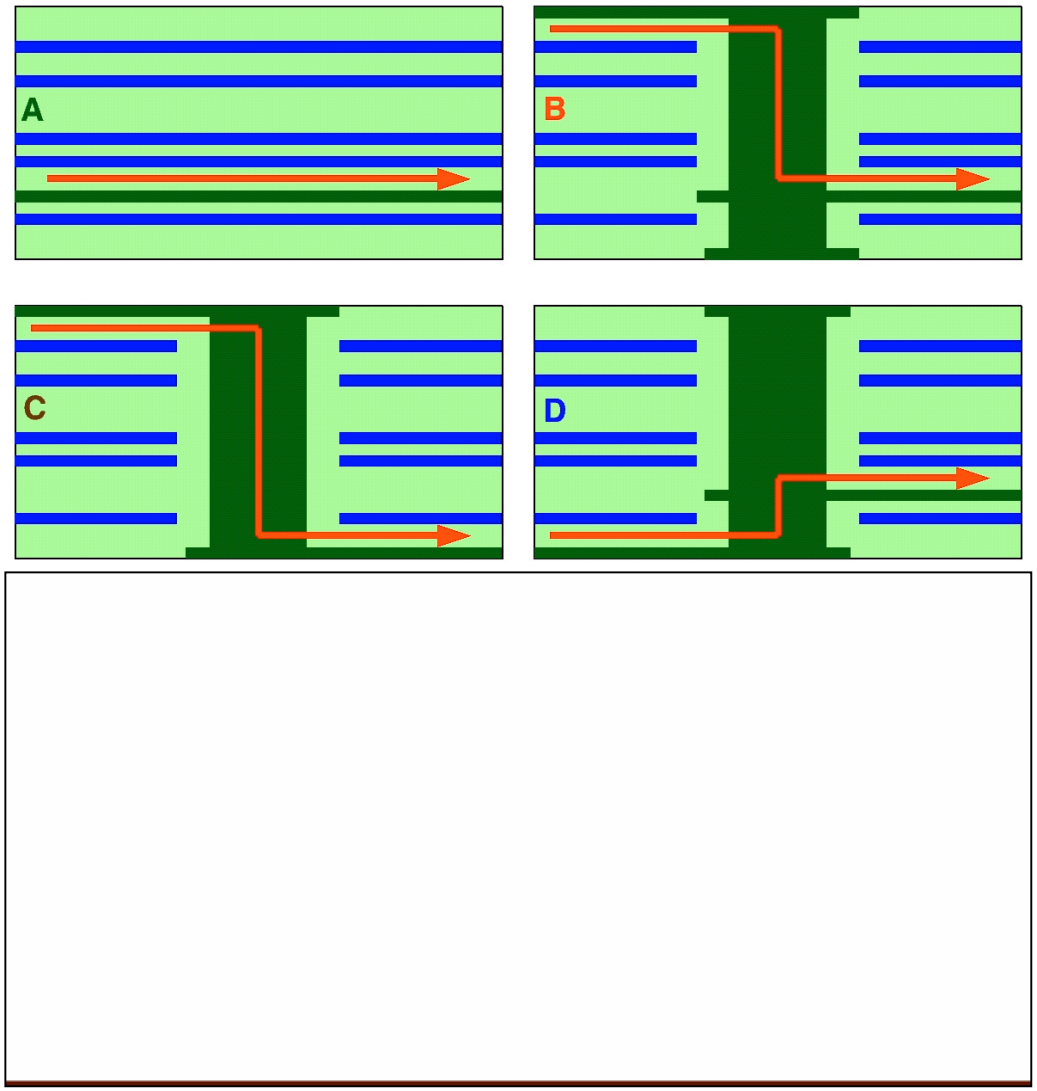


Via Stub Effects (Time Domain)

At high frequencies vias behave like series/shunt transmission line stubs

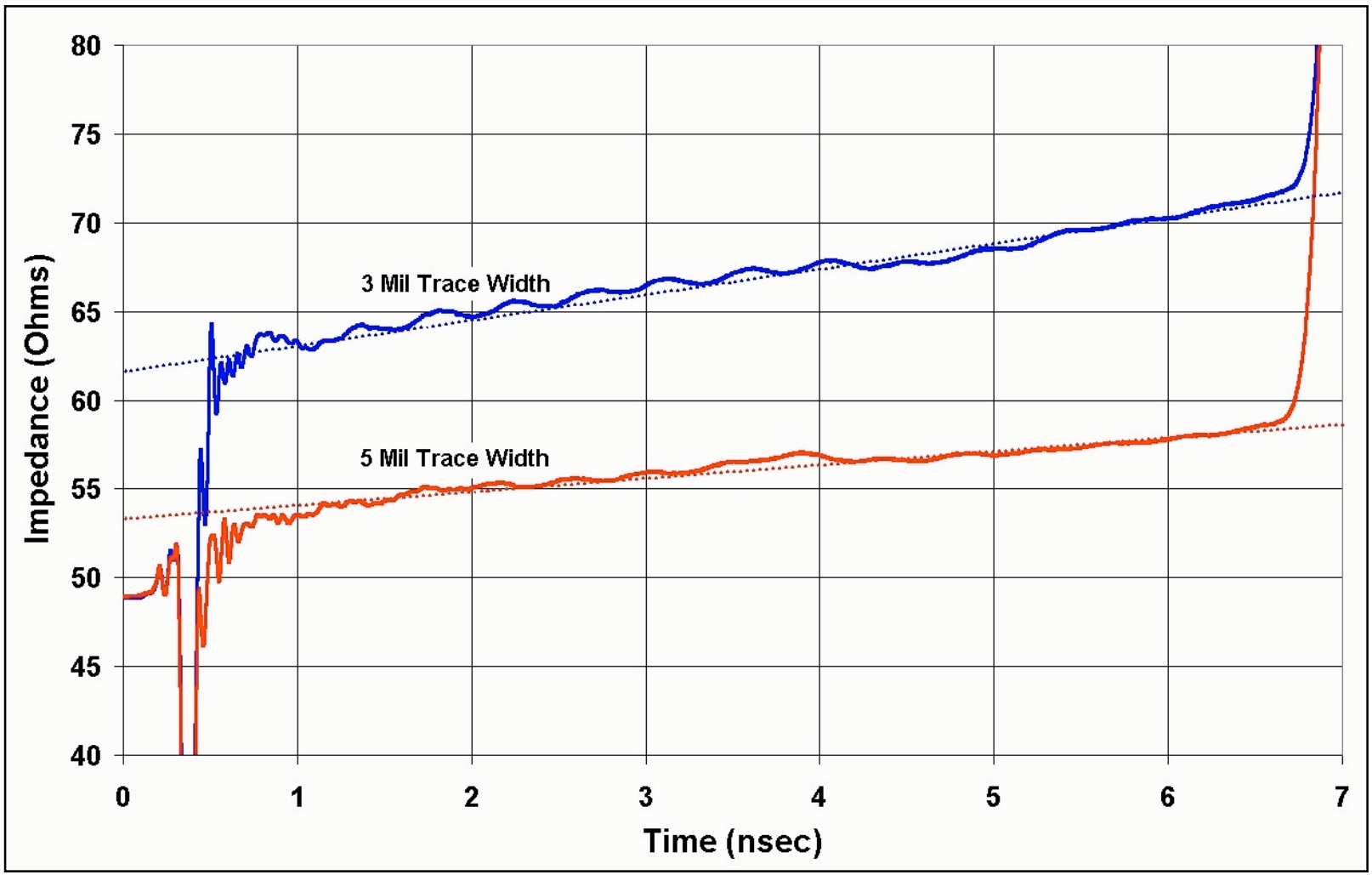


Via Signal Integrity



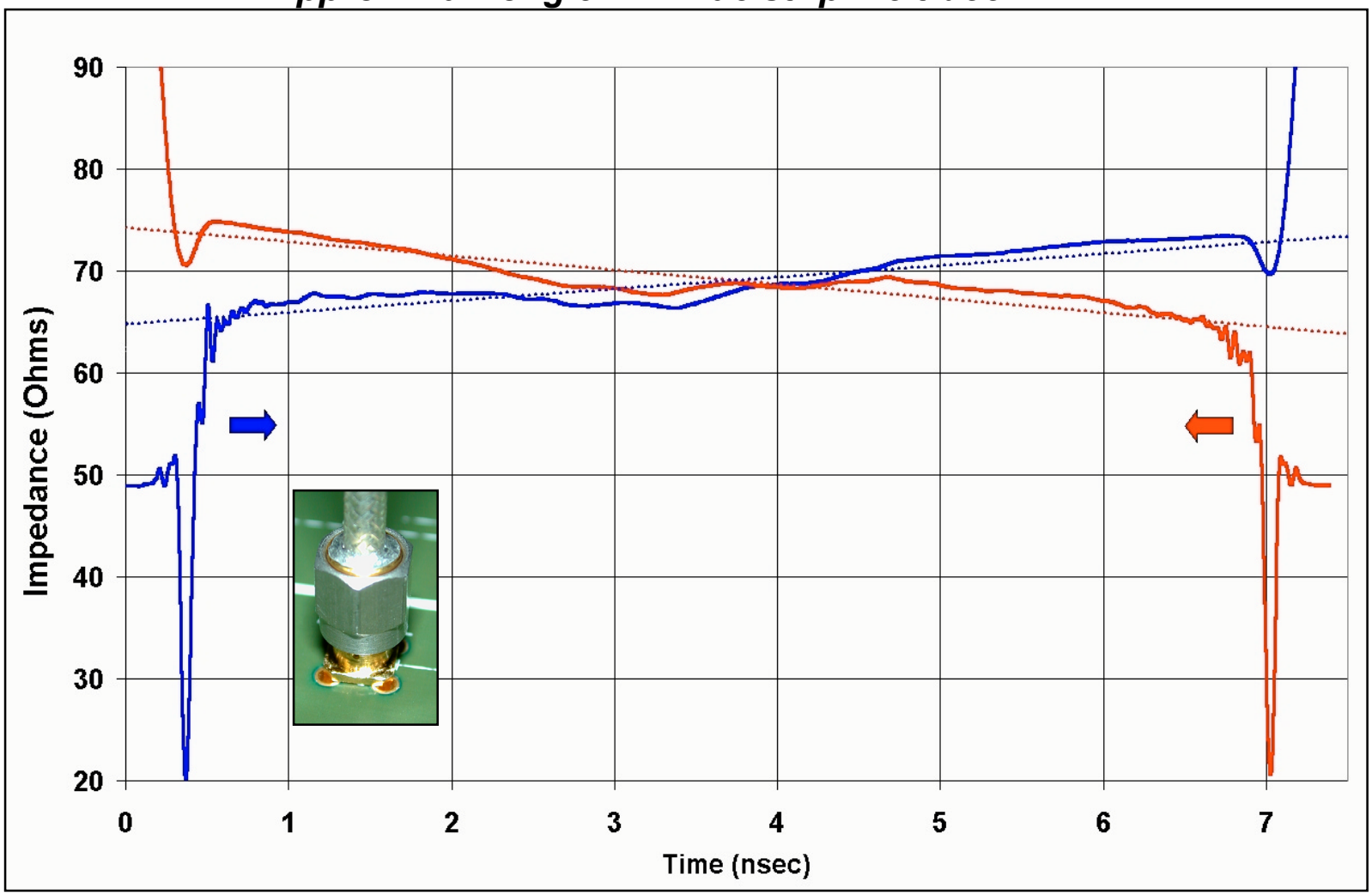
Lossy Line "Ramp Effect" on TDR Measurements

Approx. 20" long stripline traces in FR-4 Higher losses = steeper slope

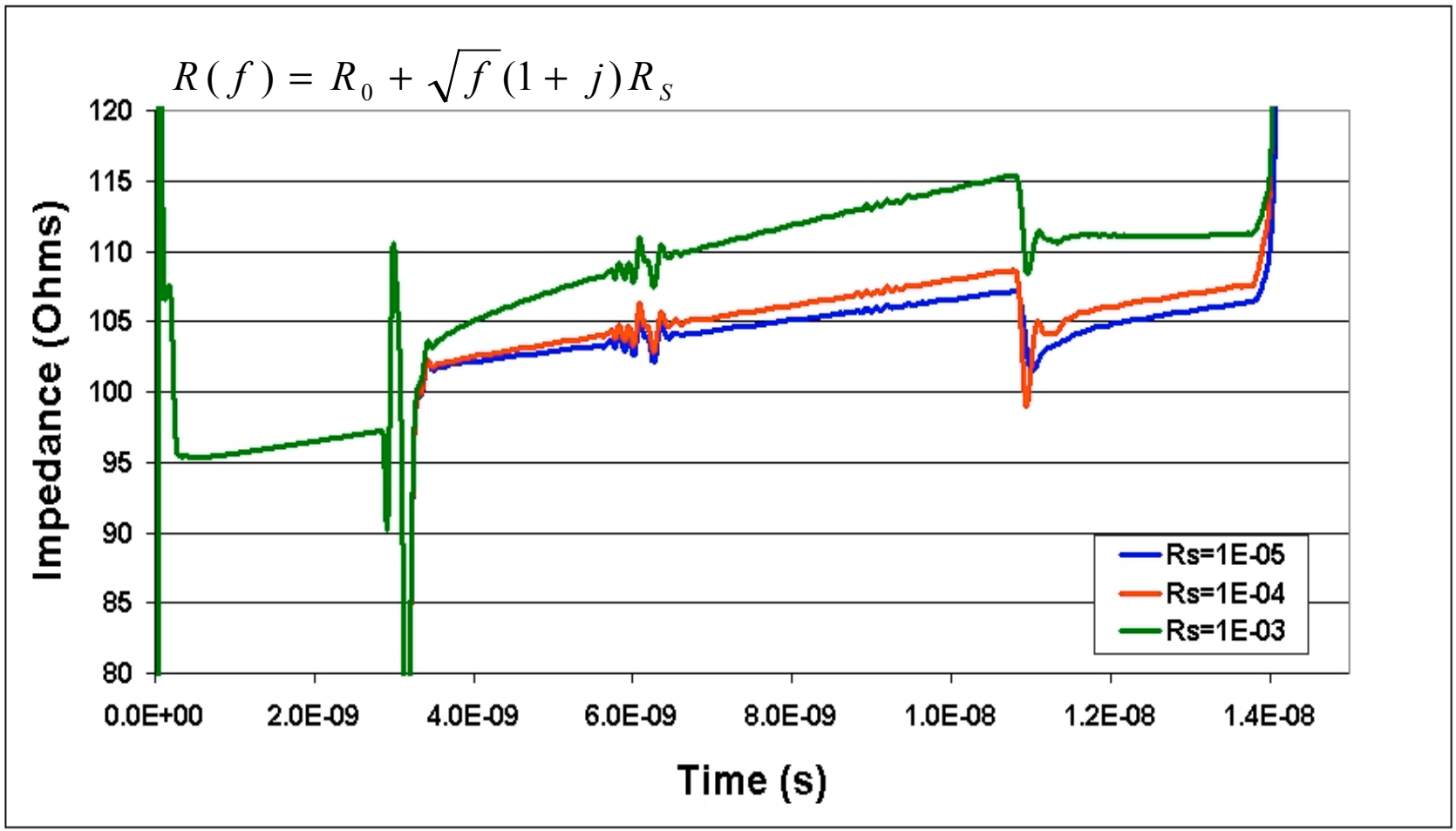


Loss of Structure Detail With TDR Measurement

Approx. 20” long 3 mil wide stripline trace in FR-4

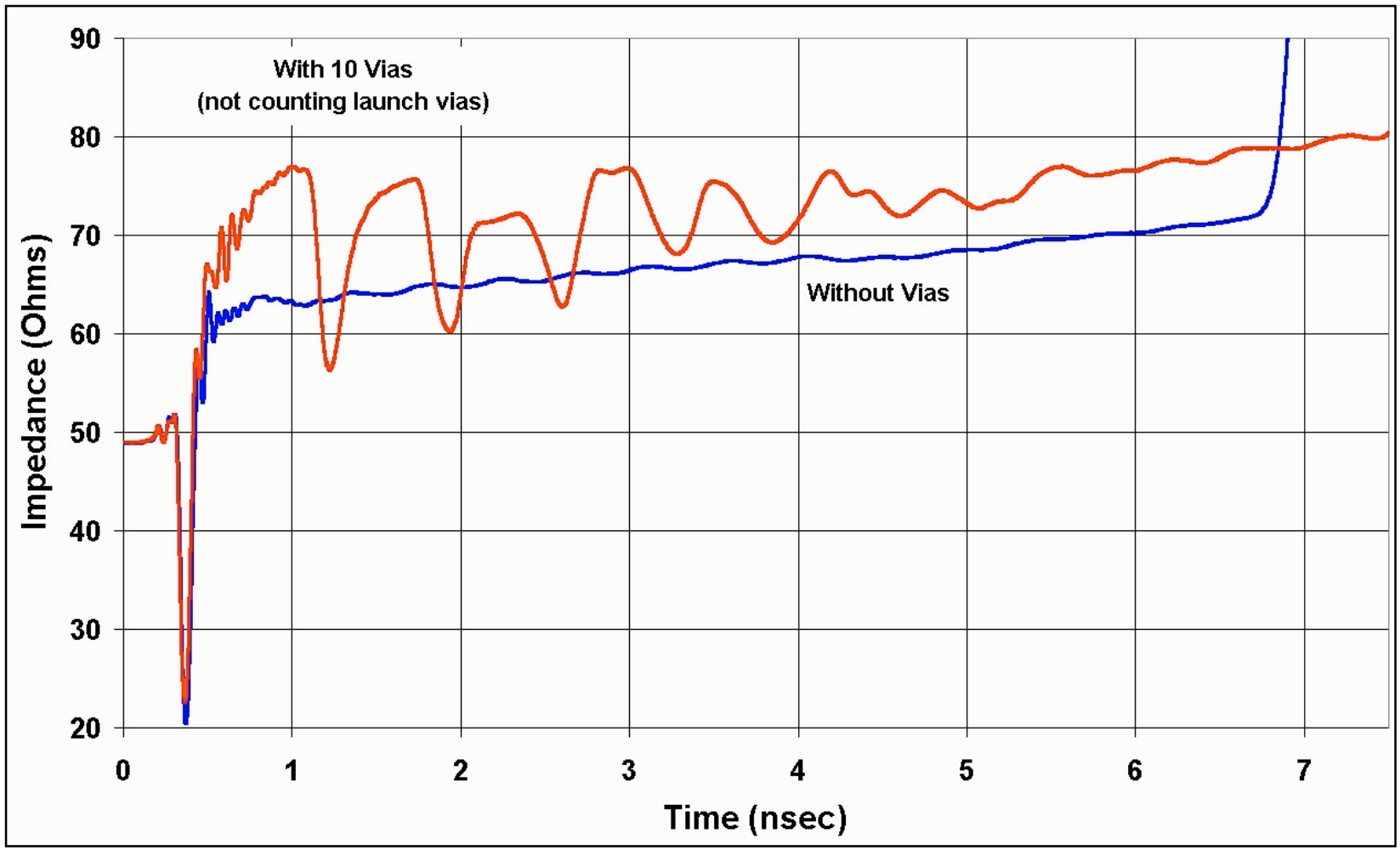


Skin Effect - Impact on Impedance



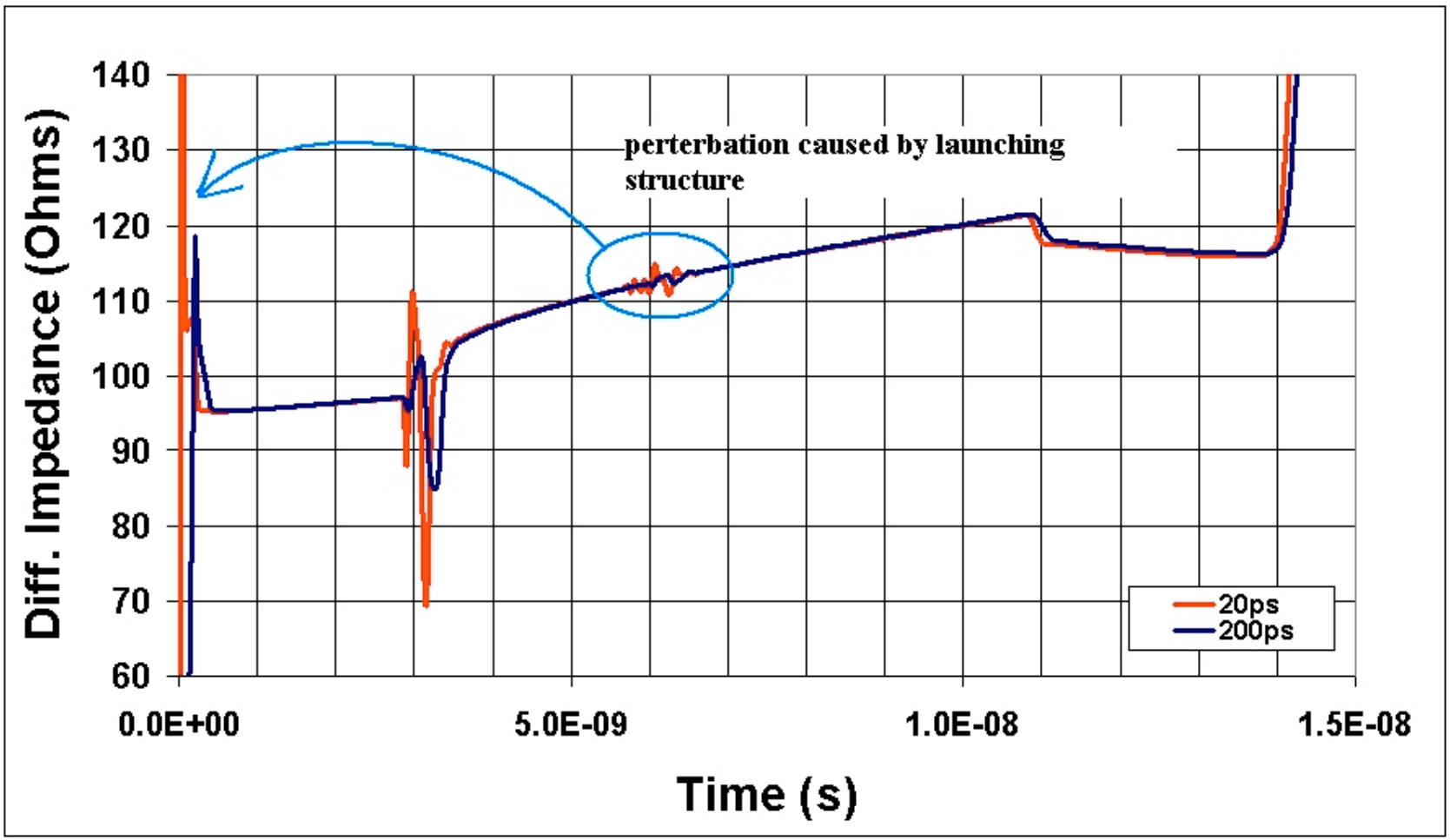
Impact of Vias on TDR Measurements

Approx. 20" long 3 mil wide stripline trace in FR-4



TDR Disconnects

Ensure test cables are longer than the traces being sampled



Summary

- Provide a short return current path between the test signal and gnd via (or pad). A nominal distance is about 80 –100mils.
- Place all traces as a single strip. Do not fold traces over adjacent to one another unless you are specifically looking to understand how this geometry affects signal impedance and delay. Along the same lines, avoid placing vias or other structures not directly related to the test trace close to the trace itself, such that it will effect the return current path and thus the impedance.
- Be aware that the impedance tends to rise on TDR waveforms as a function of trace length. How fast the impedance changes is a function of trace width and thickness. For narrower traces, use shorter trace lengths, possibly on the order of three to five inches.
- Through vias, which are used as launching structures, should be fully utilized. Avoid via “stub structures” where possible.
- Use quality test cables and connectors. Ensure that test cables are at least as long, or longer than the trace segments being tested.