Presented at IPC Printed Circuits Expo®
SMEMA Council APEX®
Designers Summit 04

Introduction to Microvia Design

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Abstract
Microvias are the fastest growing new technology for printed circuits. This talk will highlight the procedures, standards and conditions that designers needs to consider to introduce microvias to their printed circuit board designs. The basis for these procedures is the IPC-2226, IPC-4104 and IPC-6016 HDI standards. The talk will cover: Microvia Platform Types and Examples, General Requirements, Material Considerations, Mechanical/Physical properties, features sizes and constructions, Electrical Properties and Thermal Management.

The Drivers for HDI Standards

The electronics arena is increasing the capability of integration of transistors into the semiconductor die. This reality leads to more functions in the same amount of silicon real estate and thus increases the number of I/Os needed. In addition, as the size of the transistor shrinks, so does the size of the over all die. "Die shrink" is the way the semiconductor industry can offer "more" for "less". The benefit for this capability is higher speeds in circuit switching; the penalty is that the increased number of I/Os must now be positioned in different patterns in order to maintain the performance capability of the chip with its' new and greater functionality.

So driving the new trend is more I/Os, shorter lead length, smaller packages and different positioning of the I/Os to make contact to the outside world. Today's solution to the component-packaging problem is not leads on two sides versus four sides, nor is it gull-wing, versus "J" lead as the I/O of choice. The array package has come into its own, and a sphere or ball has become the lead configuration of choice. The need for information in the form of standards, specification or guidelines is paramount.[1]

HDI Structures

In order to efficiently interconnect array packages with high I/Os a new methodology needed to be developed. Although terms such as sequential multilayer or Build-up Multilayer (BUM) have surfaced in the last few years the real benefit of HDI is in the small holes identified as "Microvias". These holes are very small. The HDI Design Committee of the IPC has identified microvias as any hole equal to or less than 150 microns; that's six thousandths of an inch. In fact the language of the new package technology is becoming more and more slanted toward microns with both conductors and holes being described in terms of microns (micrometers) or millimeters.

Component ball location of the various array packages is being standardized on various millimeter pitches; 1.5, 1.25, 1.00 mm are the standards for BGA; 0.8, 0.75, 0.65, 0.5 mm are some of the pitch standards being discussed for the mini-BGAs. The use of microvias makes it possible to achieve the "escapes" from component ball patterns that are at the center of the component. Having a uniform grid approach among the various package types permits the combination of different array components on the same mounting structure; providing efficient interconnection.

The use of microvias accomplishes several things. First the via connection can be placed directly in the attachment land; the other is that mounting real estate is now made available in order to provide extra room for conductor routing and interconnecting the electronic high I/O array components. The microvias require smaller lands for both the capture of the hole (where the hole starts) and the target land (where the microvia ends). This combination of the two lands helps to make HDI structures such a useful development for interconnecting array component packages. The fact that there are several methods to create microvias provides a variety of choices, however, each manufacturer must decide which method best fits their customer base or their manufacturing core competence.

Three Platforms OF HDI

The classification of HDI products into HDI platforms is very much driven by the needs and the recent progress in developing HDI products. The mobile communication companies and their PCB suppliers have been pioneers in this area and have set many standards. In parallel, the product needs pushed the limits of the technology for high volume manufacturing and competitive pricing. The consumer industry in Japan had been far ahead in terms of volume manufacturing of HDI products. The computer and networking industry had not seen the high pressure in the past to go with HDI technologies but they will

be forced in the future to set up the technology, because of the increasing component densities. The advantage of using HDI substrates in flip chip packages is pretty obvious because of the small pitch and increasing I/O counts.

The HDI technologies can be segmented in several technology platforms. The main drivers for HDI products are today the mobile communication products, high-end computers and packaging substrates. The technical needs for these products are completely different, so that there is not one HDI technology but several platforms. Three platforms have been identified as:[2]

- HDI for miniaturization (hand-held)
- HDI for very dense substrates and segmented functionality
- HDI for high layer count and local density

HDI for Miniaturization

The original aspect of HDI for miniaturization is the overall reduction of size and weight for the final product. This is achieved with the dense design itself and with the compatibility with new dense components like µBGAs. An increase in functionality is in most cases possible while pricing is stable or even decreasing. The construction in this platform is mainly six or eight layers using internal connections (buried board) from layer 2 to (n-1). Other characteristics are 10 mil via pad, 3-5 mil via holes, mainly 4-mil lines/spacing and a board thickness around 40 mil. The material is FR4 or FR4 with a higher Tg (160°C). Figure 1a describes the basic construction and the main design rules are in Table 1.

HDI for Very Dense Substrates

HDI boards for very dense substrates are mainly four or six layer constructions with buried via connections and two layers of microvias. The focus is to match the I/O density of the flip chips. This technology will very soon merge with the HDI for miniaturization. Figure 1b shows a section of a typical substrate and Table 1 the common design rules.

HDI for High Layer Count

HDI boards for high layer count are conventional multilayers with laser-drilled holes from layers 1 to 2 and 1 to 3. Sequential combinations are possible. The microvias are drilled in the glass-reinforced dielectric. The focus is to escape out of component areas and to maintain the required impedance levels. Figure 1c shows a typical multilayer. The current industry's capability is shown in Table 1.

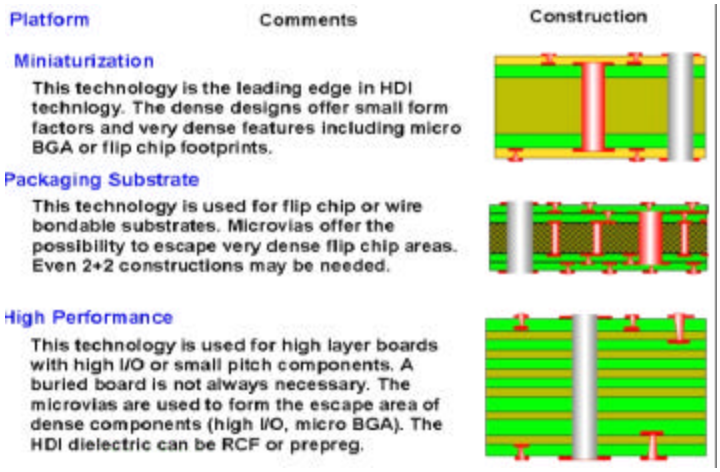


Figure 1 - The Three Platforms for HDI-microvias: A. Miniaturization of Consumer Products, B. Dense IC Substrates for Packaging, C. High Layer Count for High-performance Products

Table 1 - Comparison of Current Industry Capabilities

Feature	Conventional PCB	Conventional HDI	PBGA & MCML HDI	Adv. Type for High I/O FC
Min. Lines-mils	4.0	4.0 (3.0)	3.0	1.6
Min. Spaces-mils	4.0	4.0 (3-5)	3.0	2.0
Min. Pad Pitch-mm	Array 0.8	Array 0.4	Array 0.25	Array 0.12
Min. Pad Diameter-mils	20.0	10.0 – 16.0 18.0 – 22.0 (TH)	0.8-12.0	Infeed 5.0 Outfeed 4.0
Via Generation	Drill	Photo / laser	Photo/laser/plasma	Multi-beam laser
Min. Via Diameter w/o Plating-mils	10.0	Infeed 4.0 Outfeed 3.0	Infeed 3.5 Outfeed 2.5	Infeed 3.0 Outfeed 2.0
Pad Surface	All	Lead-free	**Ni/pure Au.,Im Ag**	Microbumps

Example of Build-Up Technology (HDI) Application

HDI-microvias boards have been in production since 1985, when they debute'd in the miniturized Hewlett-Packard 32- bit desktop computer, the FOCUS. Today, all cellular phones are microvia construction, as well as many portable or hand-held devices. One of the densest boards is seen in Figure 2. This is an industrial PDA with Wi-Fi, laser scanner, VGA -touch screen, high-speed computer and data encryption. There are nearly 307.8 connections per square inch on both sides with 0.4mm, 0.5mm, 0.65mm and 0.8mm BGA packages. This is 4,682 leads on a 15.2 square inch board!

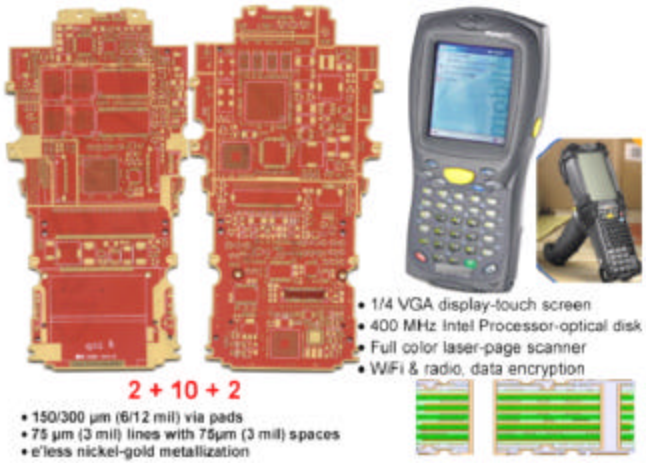
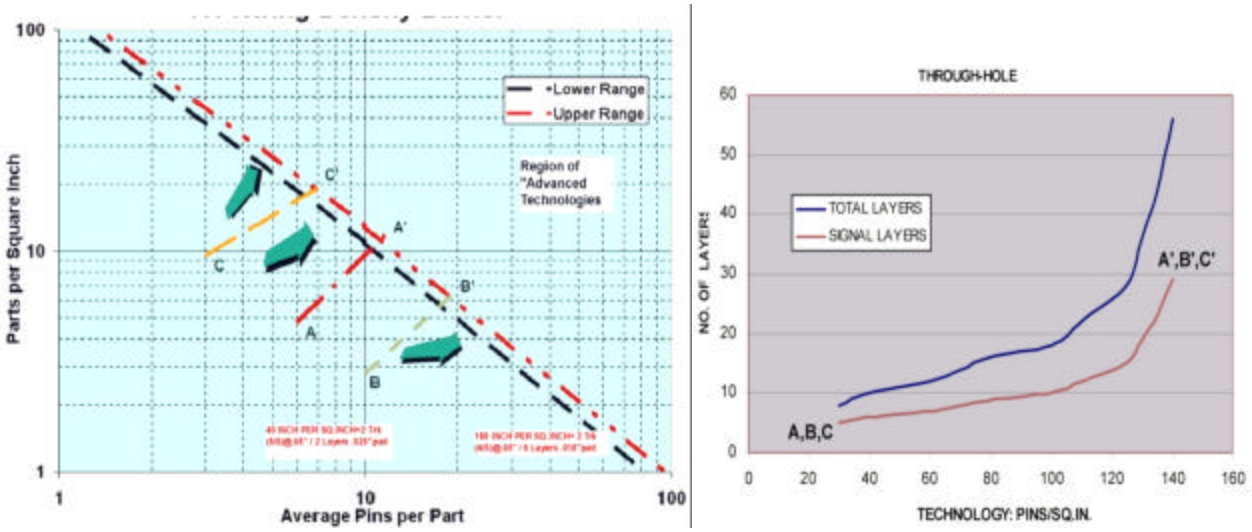


Figure 2 - N.A. Industrial PDA with Wi-Fi, Laser Scanner, VGA-touch Screen, High-speed Computer and Data Encryption

Design Basics[3]

As discrete components continue to get smaller, with the increasing use of 0402s and 0201s, and IC packages are more and more BGAs, the total of connections on both sides of a board increases. When the average connections per square inch begin to exceed 100 pins (connections) per square inch (p/si), there is less room to wire up these devices. The space occupied by the SMT land pattern, the through-hole via and the traces that connect them begin to exceed what you can put in a single square inch. This is the approach to the *"Through-Hole Barrier"* as seen in Figure 3a**.** Beyond around 120 connections per square inch, design rules have to be severely cut and additional layers added to complete the interconnect as shown in Figure 3b**.** The layer count begins to go up exponentially.



(a) (b)

Figure 3 – (a) A Density Barrier Exists for Through-hole Boards in the 120 to 140 Connections per Square Inch due to a Lack of Space for the SMT Pad and its Via. This Density Chart Allows an Assembly to be Benchmarked for its Component Packaging Density (ave pins per part), its Assembly Density (parts per square inch) and its Wiring Density (inches per square inch). C-C', A-A' and B-B' are Assemblies and as More Parts are Added to them and the Parts have More Pins, they Move to the Right and Upward. The Diagonal-dashed Lines are the "TH Wiring Density Barrier". (b) - As the Pins Per Square Inch Goes Above 130, the Total Layers Grow Exponentially

Materials

New HDI Materials

Material characteristics are the number one factor in high-performance multilayers. The most important step in HDI design is still the selection of materials. This will determine performance and fabrication technology. When designing HDI, there is an increasing array of new materials available that are not available for conventional multilayers. These materials come in four varieties:

- Copper clad resins (RCF, polyimide film, etc)
- Laminates (reinforced epoxy, Cyanate Ester, etc)
- Liquids (epoxies, photosensitive, BCBs, etc)
- Films (un-reinforced epoxy, liquid crystal polymers, etc)

From a mechanical standpoint, materials may be grouped as reinforced and non-reinforced laminates and prepregs as in Figure 4. Reinforced materials are generally better in dimensional stability, lower in coefficient of thermal expansion (CTE) and less sensitive to thermal cracking, while the non-reinforced materials often have a lower dielectric constant (Dk), are thinner and may be photoimageable.

A number of different reinforced and non-reinforced materials are enabling further miniaturization in the high-reliability market segment, as well as in consumer electronics. Glass reinforced laminates and resin-coated copper foils (RCF) are the most popular HDI materials.[3,4] Additional details can be found in the HDI Material Standard, IPC-4104.

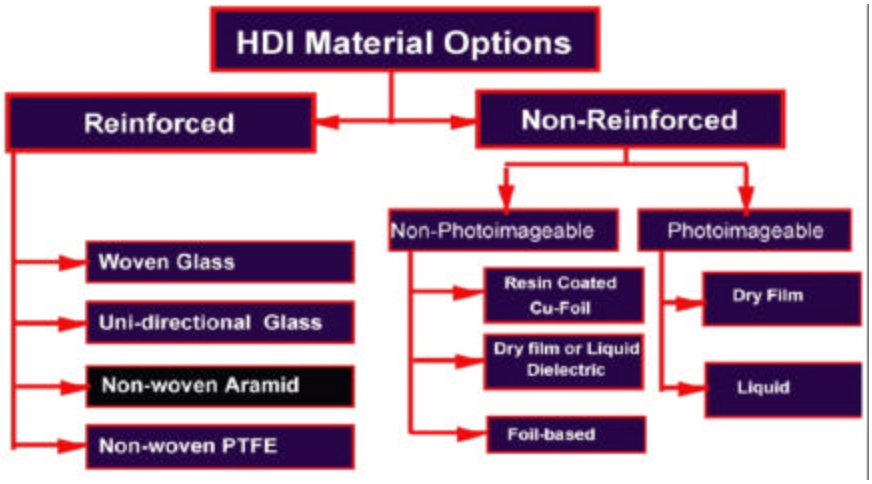


Figure 4 - HDI Material Options Broken into Reinforced and Non-reinforced Dielectrics. [4-source; The Board Authority June 2000]

Mechanical / Physical Properties

Feature Sizes

The microvia is the dominant feature in HDI designs. Figure 5 shows the typical minimum design for a large-panel. The minimum microvia diameter (A) is 4-mils with a 3 or 4-mil Outfeed dia. (B). The Capture land (C) is 10-mils, but as the figures show, a higher yield is obtained with a 12-mil land. The Target land (D) is usually 10 or 12-mils. The pitch (Z) is minimally, 16-mils. These capabilities are determined by CAT Benchmarking Panels (IPC-2151) with the coupon seen in Figure 5.

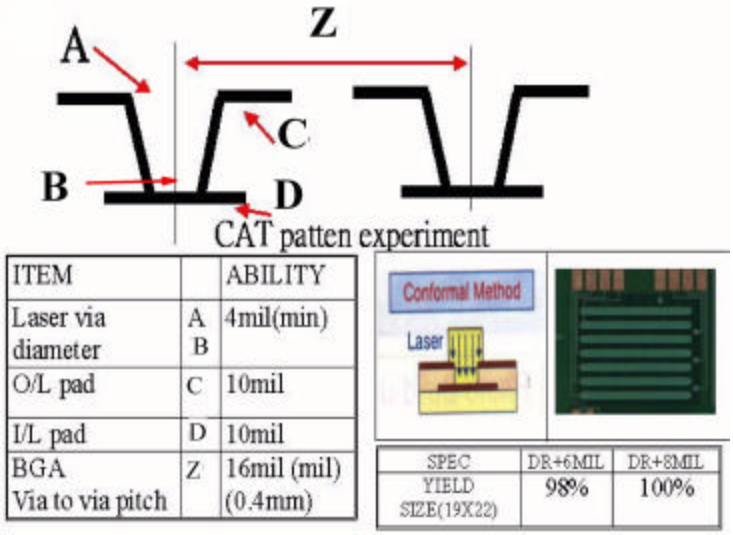


Figure 5 - Minimum Blind Via Sizes as Determined by CAT Performance Panels (IPC-9151) and Yield Results of O/L Capture Pad Size. [The Board Authority June 2000]

Construction Types

The structure of the high-density interconnection is by type. They are seen in Figure 6: Type I, Type II Type III, Type IV, Type V and Type VI characteristics. However, it is important to identify that there might be a different type of constructions on which the added microvia material would be identified. Thus, the following definition applies to all HDI's:

- TYPE I 1 [C] 0 or 1 [C] 1, with through vias from surface to surface
- TYPE II 1 [C] 0 or 1 [C] 1, with through vias buried in the core and from surface to surface
- TYPE III ≥ 2 [C] ≥ 0, two or more HDI layers added to through via in the core or from the surface to surface
- TYPE IV ≥2[P] ≥ 0 where P is a passive "substrate with no electrical connecting functions".
- TYPE V Coreless construction using layer-pairs.
- TYPE VI alternate construction using solid-vias in layer-pairs.

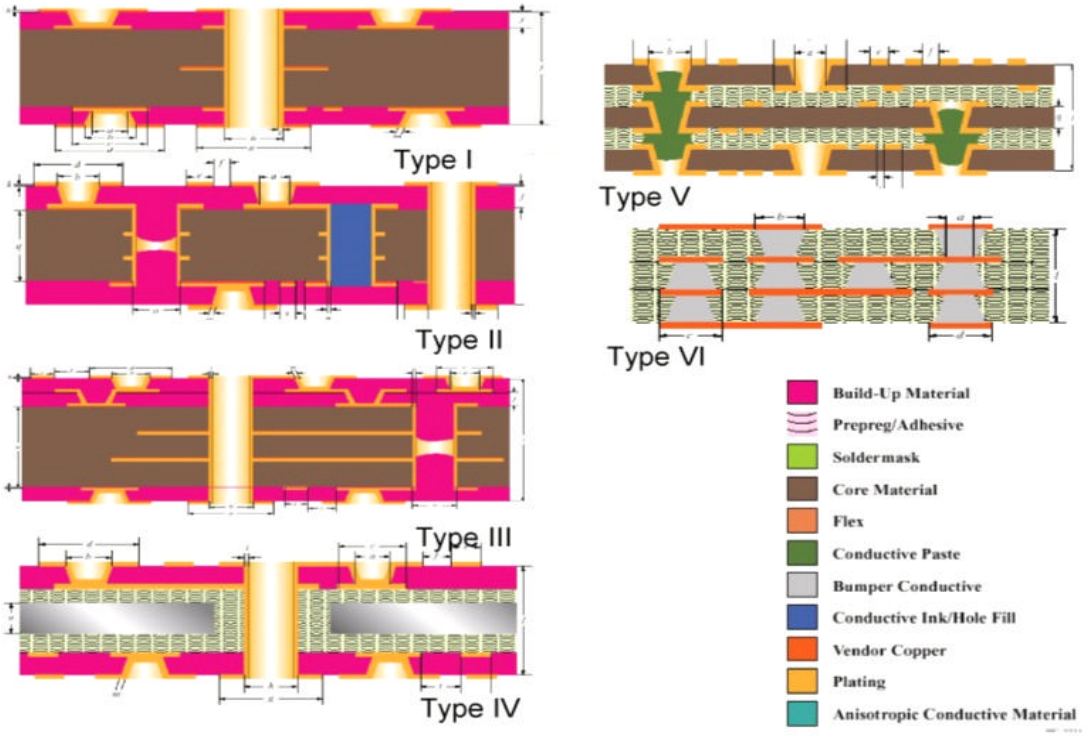


Figure 6 - HDI Construction Types from Type I to Type VI with Materials of Construction. [Source; IPC-2315, IPC-2226]

The core could now also be identified as an A, B, or C type core. Thus, [CA] is a core with internal vias only; redistribution makes contact to the surface. [CB] is core with internal and external (through microvia structures). High-density interconnecting structures make contact into the innerlayers of the core. [CC] is passive core, no interconnections.

Type I Constructions: 1[C] 0 or 1[C]1
This construction describes a High Density Interconnect substrate in which there is both plated microvias and plated through holes used for interconnection. Type 1 constructions describe the fabrication of a single microvia layer on either one 1[C]0 or both sides 1[C]1 of an underlined PWB substrate core. The PWB core substrate is typically manufactured using conventional PWB techniques. This substrate may be a rigid or a flexible substrate. The substrate can have as few as 1-circuit layers or be as complex as many prefabricated multilayer innerlayers. A single layer of dielectric material is then placed on top of the core substrate. Microvias are formed in the dielectric connecting layer 1 to layer 2 and layer n to layer n-1. Through holes are then drilled connecting layer 1 to layer n. The microvias and through holes are then metallized or filled with conductive material. Layer 1 and layer n are circutized and fabrication is completed. Typical design rules are shown in Table 2.

Type II Constructions: 1[C] 0 or 1[C]1
Type II has the same HDI layers as Type 1. The difference is the *core*, [C]. Type 2 allows the through vias to be placed in the core before the HDI layers are applied. The processes are the same except for the cores through vias being filled before the HDI layers are applied. Typical design rules are shown in Table 2.

Type III Constructions: ³2[C] ³0
This construction describes a High Density Interconnect in which there are both plated microvias and plated through holes used for interconnection. Type III constructions describe the fabrication of two microvia layers on either one 2[C]0 or both sides 2[C]2 of a PWB substrate core. The PWB core substrate is typically manufactured using conventional PWB techniques. This substrate may be a rigid or a flexible substrate. The substrate can have as few as 1-circuit layers or be as complex as a prefabricated multilayer PWB with buried vias. A single layer of dielectric material is then placed on top of the core substrate. Microvias are formed in the dielectric connecting layer 2 to layer 3 and layer n-1 to layer n-2. This first microvia layer is either metallized or filled with conductive material and then circuitized. A second layer of dielectric material is then placed on top of this circuitized layer and microvias are formed connecting layers 1 to layer 2 and layers n to layer n-1. Through holes are then drilled connecting layer 1 to layer n. The microvias and through holes are then metallized or filled with conductive material. Layer 1 and layer n are circutized and fabrication is completed. Typical design rules are shown in Table 2.

Type IV Constructions: 1 [P] 0 or 1 [P] 1 or >2 [P] > 0
This construction describes a High Density Interconnect in which the microvia layers are used as redistribution layers over an existing drilled and plated passive substrate. The PWB or metal core substrate is typically manufactured using conventional PWB techniques. This substrate may be a rigid or a flexible substrate.

Type V Constructions
This construction describes a High Density Interconnect in which the microvia layers are used as 2-sided layer-pairs. These are laminated and connected by conductive pastes or posts after the layer-pairs are tested. The layer-pairs can be manufactured by conventional PWB techniques. This substrate may be a rigid or a flexible substrate.

Type VI Constructions
This construction describes a High Density Interconnect in which the microvia layers are used as 2-sided layer-pairs with solid-vias. These are laminated and connected by conductive pastes or posts after the layer-pairs are tested. The layer-pairs can be manufactured by conventional PWB techniques. This substrate may be a rigid or a flexible substrate.

Table 2 - Recommended Design Rules for all Types of HDI Structures [IPC-2226]

Symbol	Feature	Level A	Level B	Level C
a	Microvia diameter at target land (as formed, no plating)	102 µm [4 mil]	76 µm [3 mil]	51 µm [2 mil]
b	Microvia diameter at capture land (as formed, no plating)	152 µm [6 mil]	127 µm [5 mil]	76 µm [3 mil]
c	Microvia target land size = [(a + 2x annular ring) + FA (1)]	406 µm [16 mil]	330 µm [13 mil]	229 µm [9 mil]
	FA for c =	203 µm [8 mil]	152 µm [6 mil]	102 µm [4 mil]
d	Microvia capture land size = [(b + 2x annular ring) + FA (1)]	406 µm [16 mil]	330 µm [13 mil]	229 µm [9 mil]
	FA for d =	203 µm [8 mil]	152 µm [6 mil]	102 µm [4mil]
s	Internal conductor trace width	127 µm [5 mil]	75 µm [3 mil]	50 µm [2 mil]
t	Internal conductor spacing	127 µm [5 mil]	100 µm [4 mil]	50 µm [2 mil]
e	External conductor trace width	127 µm [5 mil]	75 µm [3 mil]	45 µm [1.77 mil]
f	External conductor spacing	127 µm [5 mil]	100 µm [4 mil]	45 µm [1.77 mil]
g	Through via land size = [(h + 2x annular ring width) + FA (1)]	See 9.1.1 of IPC-2221	See 9.1.1 of IPC-2221	See 9.1.1 of IPC-2221
h	Through via diameter (as formed, no plating)	See Table 5-2	See Table 5-2	See Table 5-2
i	Minimum through via hole wall plating thickness	See IPC-2221, Table 4-3	See IPC-2221, Table 4-3	See IPC-2221, Table 4-3
j	Dielectric thickness (HDI blind microvia layer) (2)	64	64 µm [2.5 mil]	<50 µm [2 mil]
k	External Cu foil thickness (if Cu foil utilized)	1/2 oz (See IPC-2221, Table 10-2)	3/8 oz (See IPC-2221, Table 10-2)	1/4 oz (See IPC-2221, Table 10-2)
m	Minimum blind microvia hole plating thickness	10 µm [0.3937 mil]	10 µm [0.3937 mil]	15 µm [0.5906 mil]
m'	Minimum buried microvia hole plating thickness	10 µm [0.3937 mil]	10 µm [0.3937 mil]	15 µm [0.5906 mil]
n	Minimum buried via hole wall plating thickness	See IPC-2221, Table 4-3	See IPC-2221, Table 4-3	See IPC-2221, Table 4-3
o	Buried via diameter (as formed, no plating)	See IPC-2221, Table 9-4	See IPC-2221, Table 9-4	See IPC-2221, Table 9-4
p	Buried via land size = [(o + 2X annular ring) + FA (1)]	See 9.1.1 of IPC-2221	See 9.1.1 of IPC-2221	See 9.1.1 of IPC-2221
q	Buried via core thickness (excluding outermost conductors)	75 µm [3 mil]	63 µm [2.5 mil]	<63 µm [2.5 mil]
r	Buried via Cu foil thickness (outermost layer)	1/2 oz (See IPC-2221, Table 10-2)	3/8 oz (See IPC-2221, Table 10-2)	1/4 oz (See IPC-2221, Table 10-2)
u	Core board thickness (excluding conductors)	75 µm [3 mil]	63 µm [2.5 mil]	<63 µm [2.5 mil]
	Staggered via pitch	(p+c)/2	(p+c)/2	(p+c)/2

1. F.A. = Fabrication Allowance which considers production master tooling and process variations required to fabricate printed boards.
2. Measured from top surface of Layer 2 Cu to bottom surface of Layer 1 Cu.

TYPE I and TYPE II Structures

Design Rules

The designer should be aware that not all fabricators have equal capabilities in the areas of fine pitch imaging, etching, layer-to-layer alignment, via formation and plating. For this reason the HDI design guide categorizes design rules into three Levels, nominally A, B, and C with A being the easiest to produce and C being the most difficult. Selection of more stringent design standards will limit the number of fabricators capable of producing such a board. Circuits produced with design rules in the 'A' category will be easier to produce, have higher yields and therefore can be fabricated at lower cost. To keep costs at a minimum, the design rules most appropriate for the application should be selected.

Level A

This specification allows conventional HDI processes to be used with relaxed tolerances. It should have the highest yield and lowest cost. It is estimated that 95% of HDI fabricators can meet these design rules.

Level B

This is the conventional HDI process. It is estimated that 60% of HDI suppliers can meet these design requirements under production conditions.

Level C
Top-level fabrication shops, representing 20% of the total market, can meet these design rules. Panel sizes are often reduced to increase yield, which increases final cost. Production volumes are presently limited, with special attention required during the production process.

Via Escalation

Most fine-pitch or high-I/O BGAs can be designed with Type I HDI construction. The escalation for increased density is seen in Figure 7. Variable depth microvias are added to Type I before moving to a Type II construction. Then variable depth and stacked microvias are added to Type II before moving to Type III construction. Stacked vias with a Type III construction is the highest density (and the highest cost). These are typically used in fine-pitch flip-chip substrates going down to 0.1mm pitch.

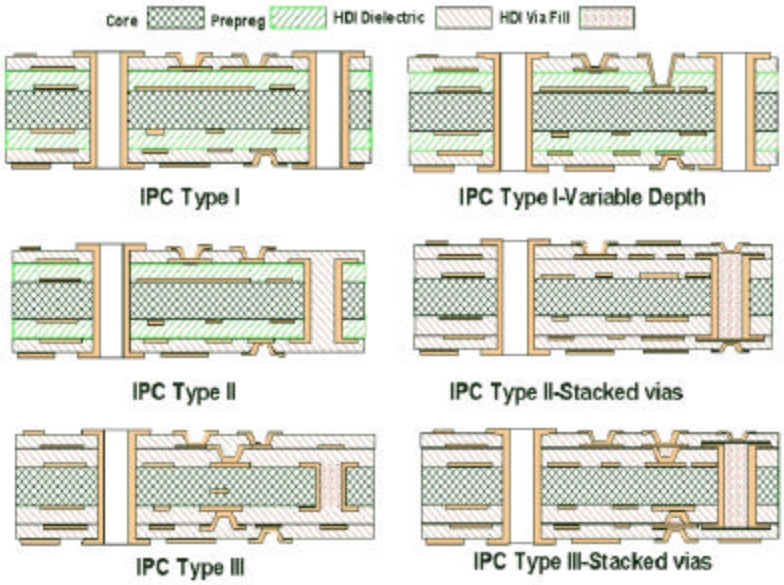
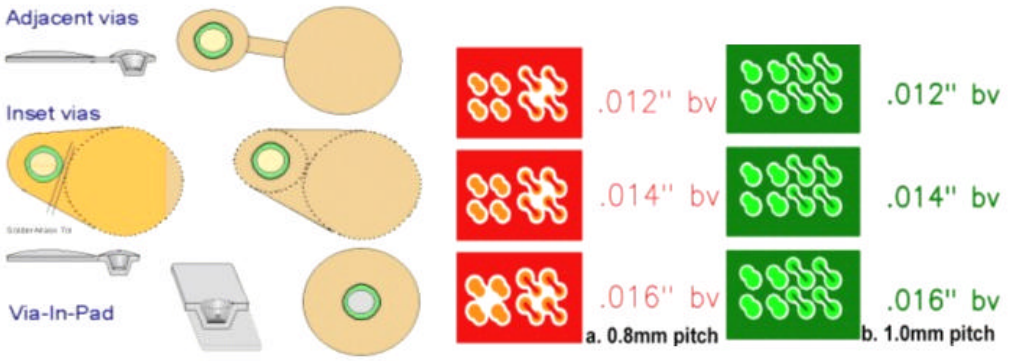


Figure 7 - The IPC HDI Types I to III are the Most Common Microvia Structures Used - from the Simplest (Type I) to the Most Complex (Type III with stacked vias).[Source: 3-The Board Authority]

Via Placement

Microvias being inherently small can be placed closer to SMT lands, all the way to being *'in the SMT land'*. Figure 8a shows the adjacent placement (dogbone), inset and via-in-pad. Figure 8b compares the adjacent to the inset for 1.0 mm and 0.8 mm pitch BGAs with .012" to .016" BGA lands. The inset microvias still provide enough room for a surface ground fill.



(a) (b)

Figure 8 – (a) Three Alternatives for the Connection of a BGA Pad to a Microvia. (b) - Comparison of the Inset Microvia to an Adjacent (dogbone) Microvia. The Inset Vias Allow Enough Room for a Surface Ground Flood.

Electrical Properties

High Frequency Performance[5]

The characteristic impedance of single ended microstrips, striplines, coplanar and differential signals is determined by the material's dielectric constant and the board's thickness stackup and design rules. Signal attenuation is a function of the material's dielectric loss, design rules and trace length. Various types of noise (ground bounce, switching noise, power supply spikes, etc.) including crosstalk is a function of power supply coupling through the boards stackup, ground layers, design rules and material characteristics.

One of the major goals in improving the signal integrity of a high-speed board is the reduction of inductance. The SMT mounting pads with the lowest inductance are the ones with no traces and use a microvia-in-pad (VIP). Figure 9 shows that a microvia is 1/10th the inductance and capacitance of a standard through-hole.

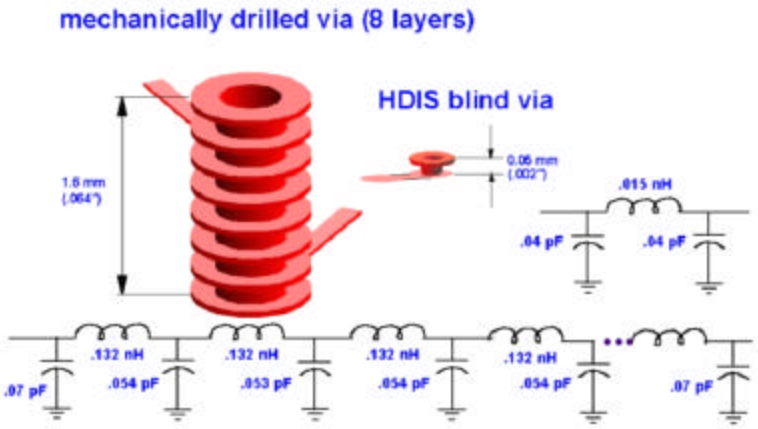


Figure 9 - Comparison of Electrical Performance of a Through-hole to a Microvia.[5]

Thermal Management

Current Carrying Capacity[6]

The thinner dielectrics that go with microvias are an aid to thermal dissipation. The new films and liquid dielectrics also allow better thermal properties than may be found with conventional laminates.

The current work going on with IPC-2152, the Current Carrying Capacity is seen in Figure 10a. The original IPC curves in IPC-2221 were derived from 1954 NIST single-sided phenolic boards. As seen in Figure 10 b and 10c, the IPC information is very conservative and sometimes 4X higher than test measurements have revealed.

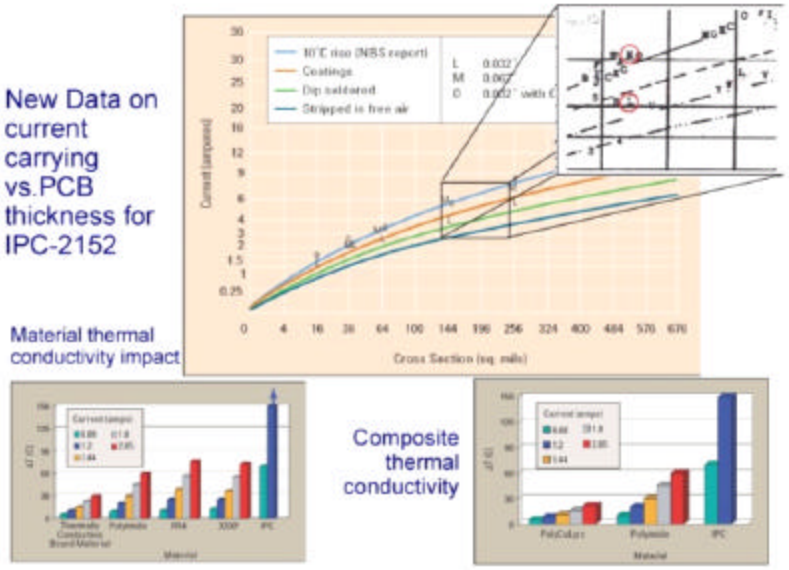


Figure 10 – (a). New Data on Current Carrying Capacity for IPC-2152 (b). Material Thermal Conductivity Impact (c). Composite Thermal Conductivity.[6]

Conclusion

The IPC-2315 has been released for a few years now, so we encourage you to join the IPC-2226 HDI Design Std. Committee. The High Performance HDI Platform is the vehicle for complex components that also have higher I/Os and finer pitches and circuits that run at extremely high frequencies and fast signal rise-times. This requires tighter requirements for signal integrity and consequentially, for the base materials. The selection of via structures, board stackup and design rules are then much more complex.

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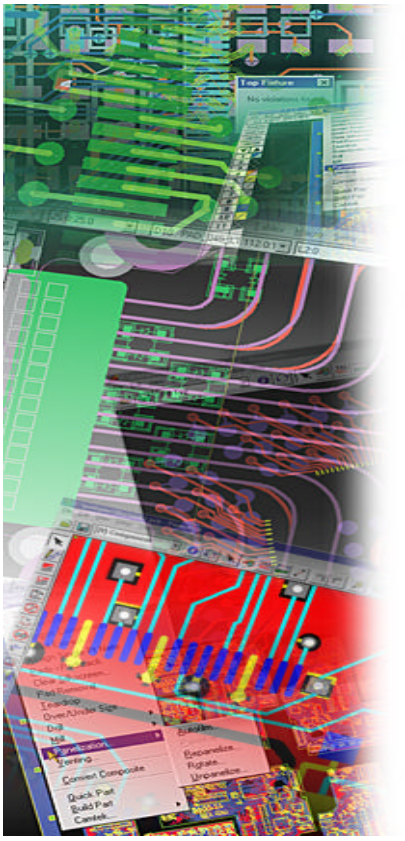

Introduction to Microvia Design

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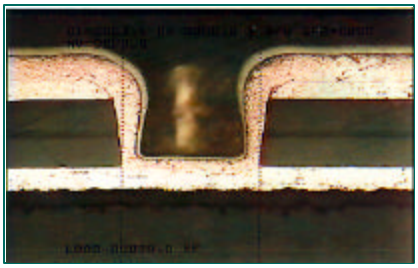
IPC-2226

Sectional Design Standard For High Density Interconnect (HDI) Printed Boards

- Platform Types
- General requirements
  - ►Microvias
  - ►Design basics
- Materials
  - ►New HDI materials
- Mechanical/Physical properties
  - ►Feature sizes
  - ►Construction types
- Electrical properties
  - ►High frequency performance
- Thermal management
  - ►Current carrying capacity

Microvias



drilled through copper/dielectric with UV-YAG

- ITRI Project Sample

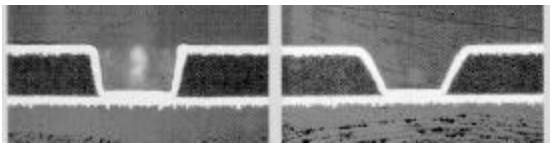
- CO2 lasered cavity

- 3 mil blin
  Polymide

- Plasma via in RCC

- Photodielectric via

- CO2 lasered blind via



IPC Document

A IPC Documents

The Institute For Interconnecting And Packaging Electronic Circuits

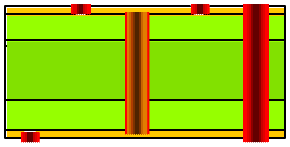
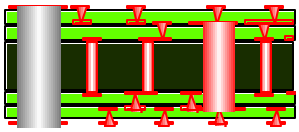
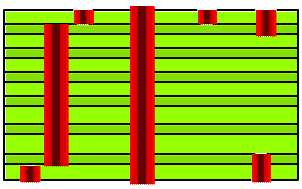
IPC-2315
Design Guide for High Density Interconnect Structures and Microvias

IPC-2226
Design Standard for High Density Interconnect Structures and Microvias

IPC-4104
Materials Standard for High Density Interconnect Structures and Microvias

IPC-6016
Specifications and Requirements for High Density Interconnect Structures and Microvias

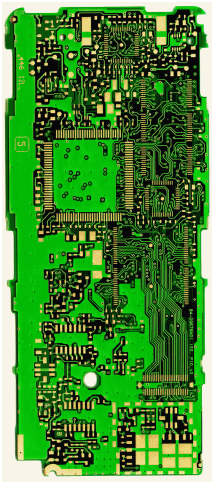
HDI PLATFORMS

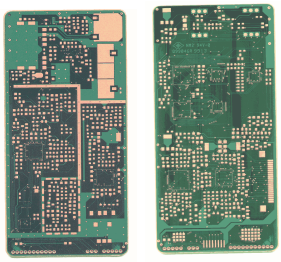
Platform	Comments	Construction
Miniaturization	This technology is the leading edge in HDI technlogy. The dense designs offer small form factors and very dense features including micro BGA or flip chip footprints.	
Packaging Substrate	This technology is used for flip chip or wire bondable substrates. Micro vias offer the possibility to escape very dense flip chip areas. Even 2+2 constructions may be needed.	
High Performance	This technology is used for high layer boards with high I/O or small pitch components. A buried board is not always necessary. The microvias are used to form the escape area of dense components (high I/O, micro BGA). The HDI dielectric can be RCF or prepreg.	

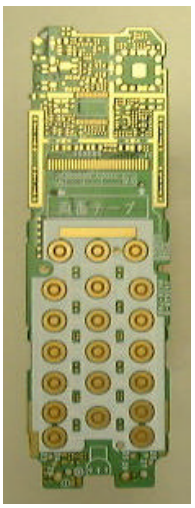
Platform 1: HDI for Miniturization

Rapidly evolving from Seq. Lamination to HDI

3+3, 4+4, 1+2+2+1, now 1+4+4+1



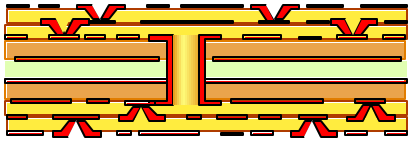


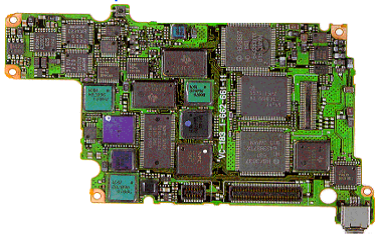


Platform 1: HDI for Miniturization

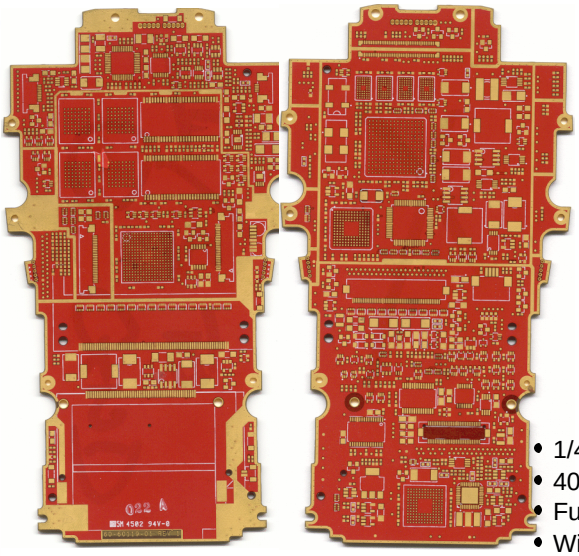
SONY Micro-CamCorder (DCR-PC7),59 x 129 x 118 mm, 500g.

- 20 CSPs, all 0.5 mm pitch
- 62 I/O image memory CSP polyimide tape interposer (TI, 9x13 mm)
- 100 I/O analog com CSP polyimide tape interposer(TI, 10x10 mm)
- 208 I/O Control, CSP polyimide tape interposer (NEC, 10x10 mm)
- 17 other Sony made CSPs
- 8 Layer HDI, 2+4+2
  - 100um lines, 125um spaces
  - 250um via lands
  - 3 mil lines / 3 mil spaces
  - 8496 - 5 mil photovias





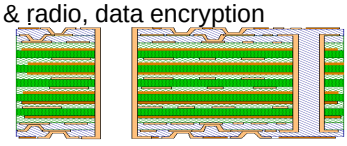
Platform 1:HDI High-Performance PDA



- 1/4 VGA display-touch screen
- 400 MHz Intel Processor-optical disk
- Full color laser-page scanner
- WiFi & radio, data encryption

2 + 10 + 2

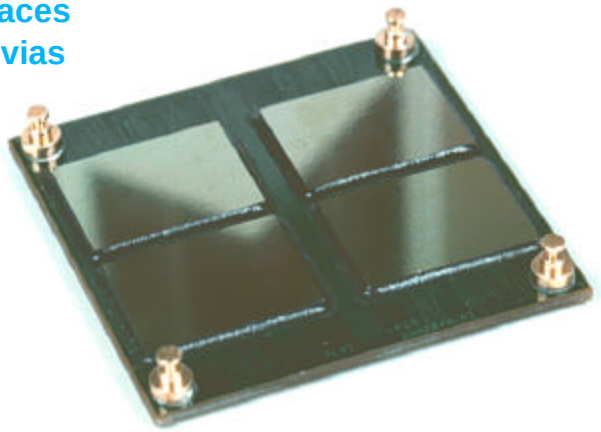
- 150/300 µm (6/12 mil) via pads
- 75 µm (3 mil) lines with 75µm (3 mil) spaces
- e'less nickel-gold metallization



Platform 2: HDI for Packaging Substrates

Flip Chip Multi Chip Module

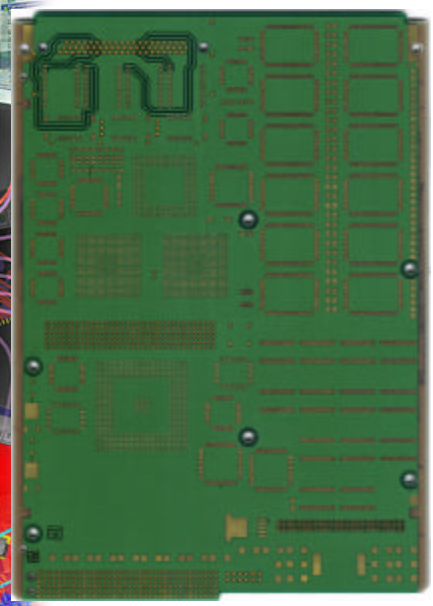
- 37.5 mm, 1.27 mm grid, 765 I/O BGA
- SLC 2S2P (4+4) RFP 38 mils thick
- Filled vias on top surface
- 2 mil lines / 3 mil spaces
- 9,719 - 3.5 mil photovias



Source: IBM

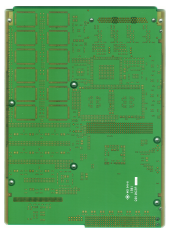
Platform 3:HIGH REL. Avionics Module

- Triple OC-192 (10Mb) Optical Network Controller



build-up multilayer

1+8+1

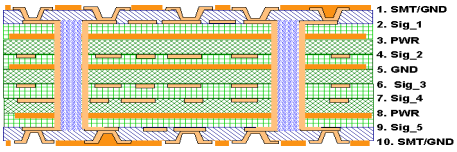


- **Application: Commercial aircraft network controller**
- **Enables high I/O component assembly (230 LPSI)**
- **1 week redesign time**
- **Low EMI/RFI, flooded surface GND plane**
- **Laser vias in SMT pads**
- **Replacement: for 18 L TH**
- **Material: Low loss-High Tg FR408**

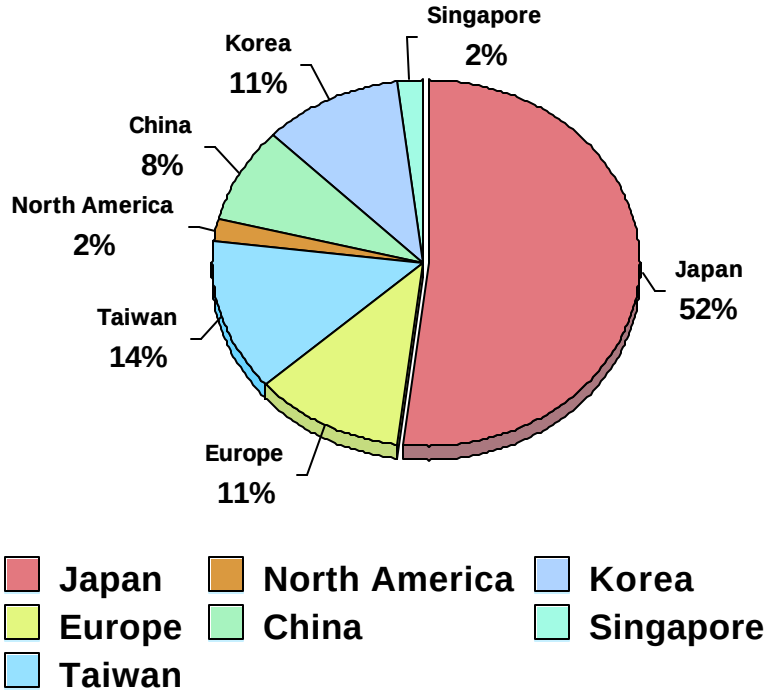
design rules

Thickness: 0.072"	VIA / PAD DIA. (inch)	TRACE / SPACE (inch)
Outerlayers	0.006 / VIP	- / -
Innerlayers	0.010 / 0.020	0.005 / 0.007

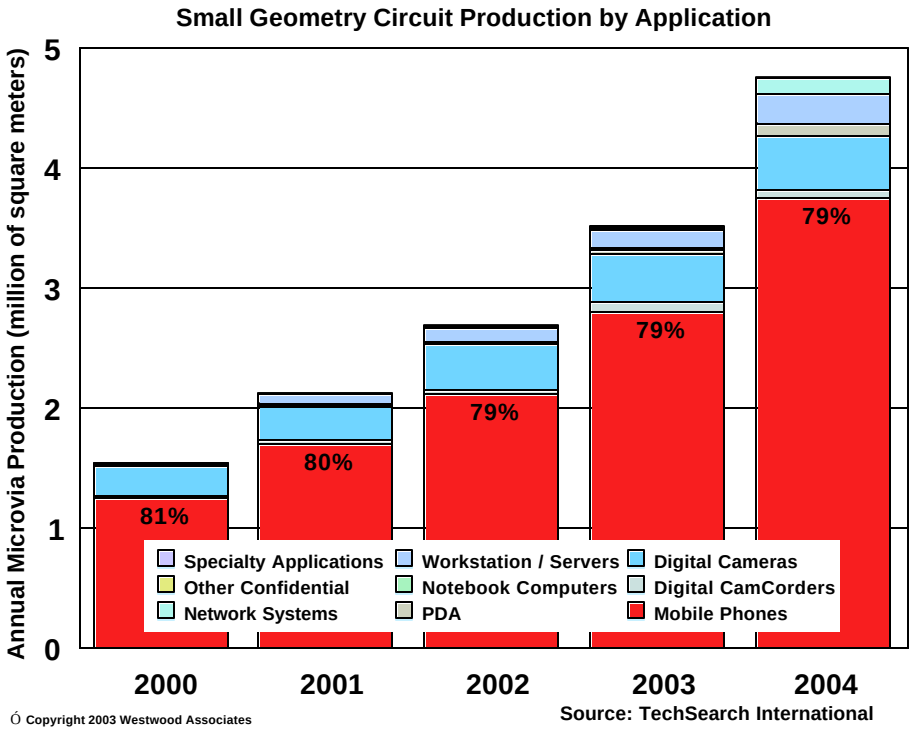
cross section



Small Geometry Circuit Production

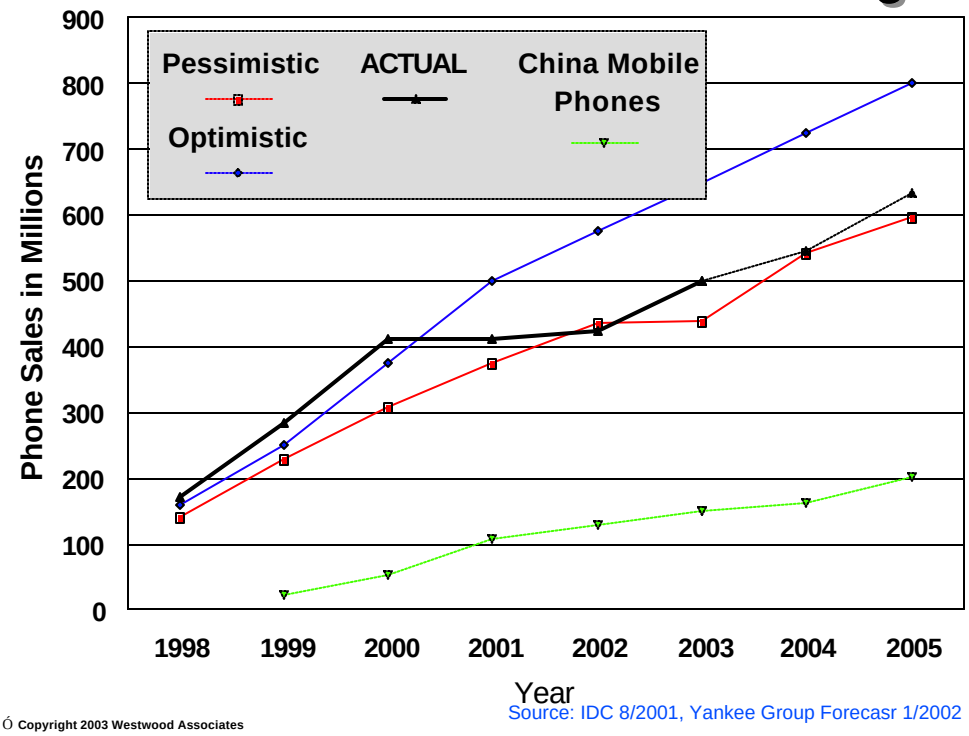


Mobile Phone Share of Microvia Board Market



Source: TechSearch International

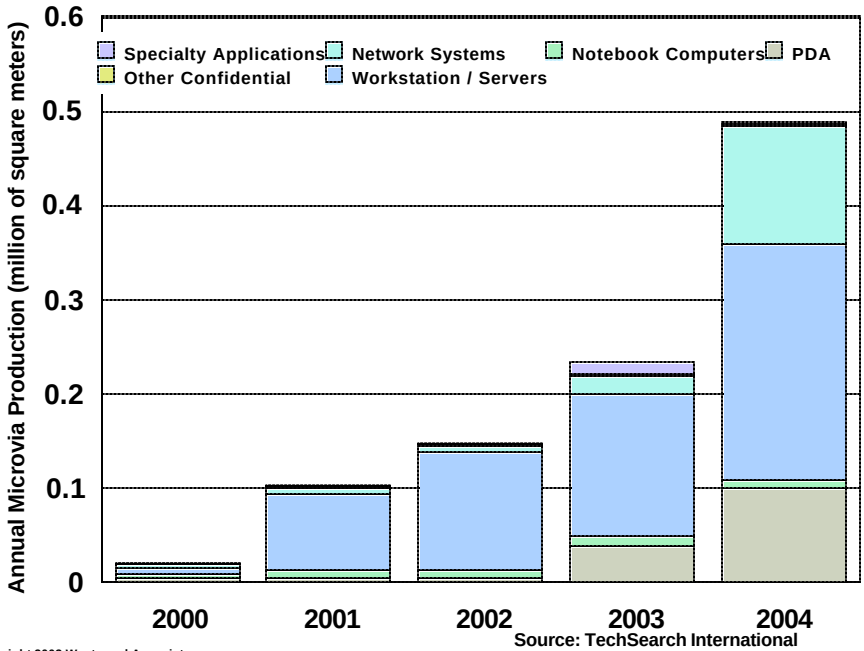
Global Cell Phone Manufacturing



Source: IDC 8/2001, Yankee Group Forecasr 1/2002

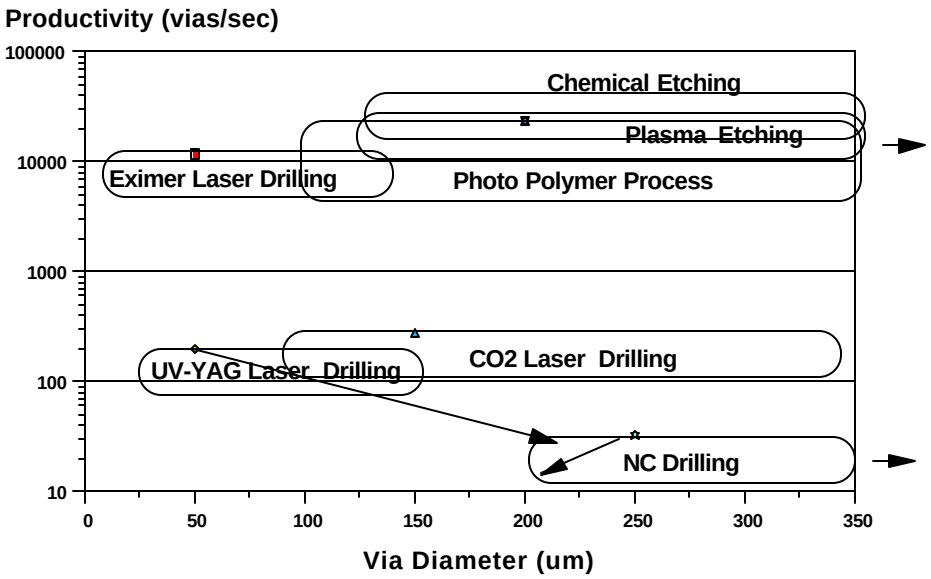
Microvia Board Market

Small Geometry Circuit Production by Application minus consumer (cell phone, camera & camcorders



Source: TechSearch International

Comparison Of Via Formation

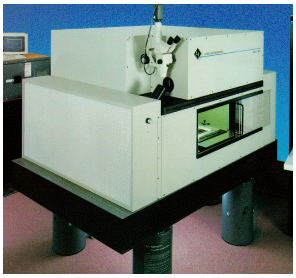


CO_2/UV/YAG Laser Drilling Equipment

New UV YAG lasers require no gases, are very compact and can drill up to 120 vias per second.

Solid State UV YAG
Can drill both blind and through hole vias, structure copper, and drill all laminates and reinforcements

New excimer lasers are the largest and most expensive but still cannot penetrate copper or glass and require some type of mask. Holographic phase masks can drills up to 12,000 vias per minute.

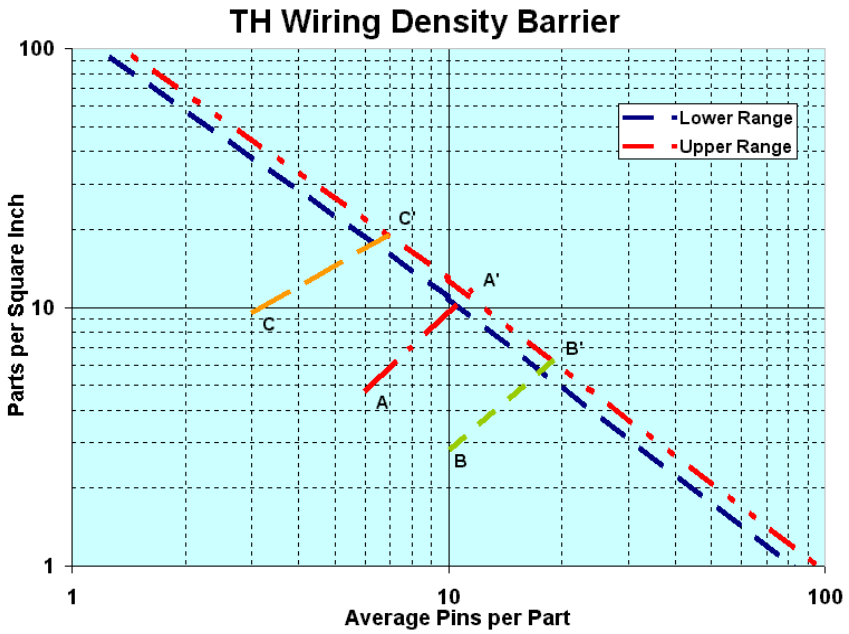


TEA CO2 laser
(Transversely Excited Atmospheric) has a gas mixture that nearly 90% of the energy is absorbed by all PWB laminates, prepreg and woven glass

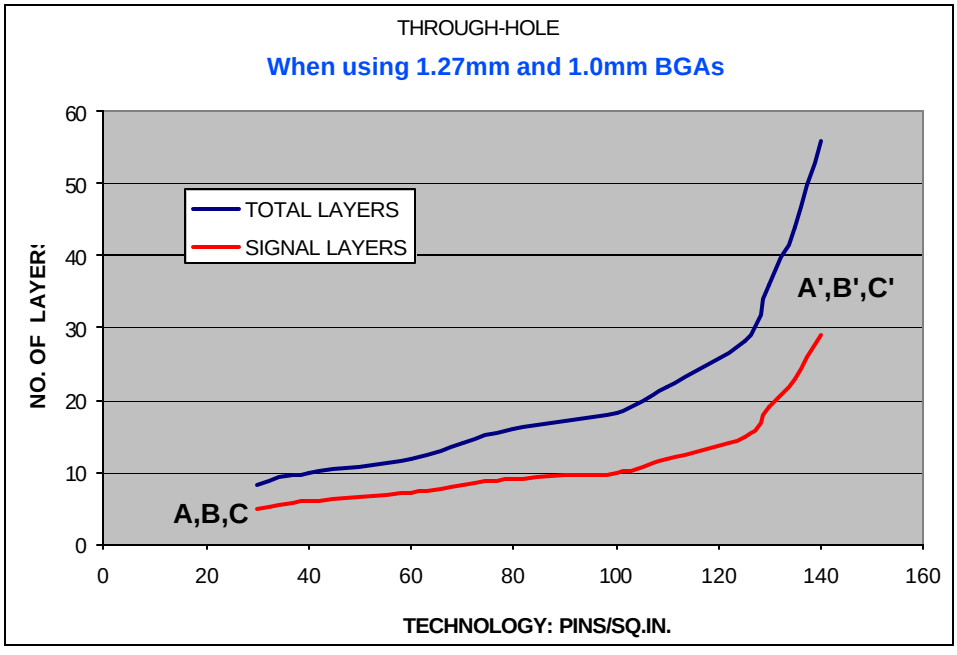
New YAG lasers require no gases, are very compact and can drill up to 120 vias per second.

CO2 laser can drill both blind and through hole vias in all non-glass laminates and reinforcements

The TH Wiring Density Barrier

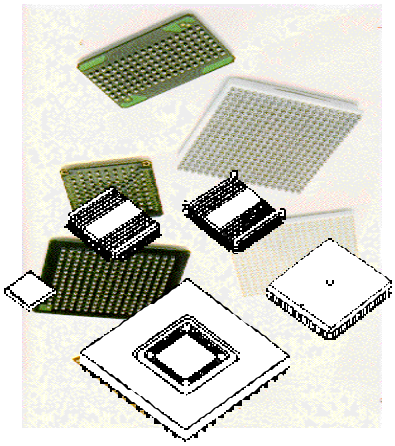


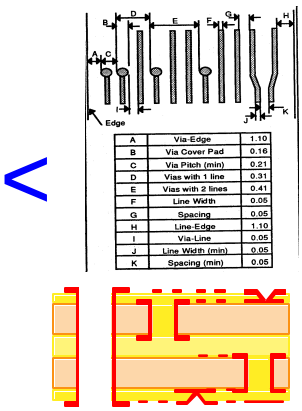
TH Multilayer Diminishing Returns



Balancing The Density Equation

Component's PWB Wiring Demand **< PWBs Design Rules & Construction Wiring Capabilities**





A	Via-Edge	1.10
B	Via Cover Pad	0.16
C	Via Pitch (min)	0.21
D	Vias with 1 line	0.31
E	Vias with 2 lines	0.41
F	Line Width	0.05
G	Spacing	0.05
H	Line-Edge	1.10
I	Via-Line	0.05
J	Line Width (min)	0.05
K	Spacing (min)	0.05

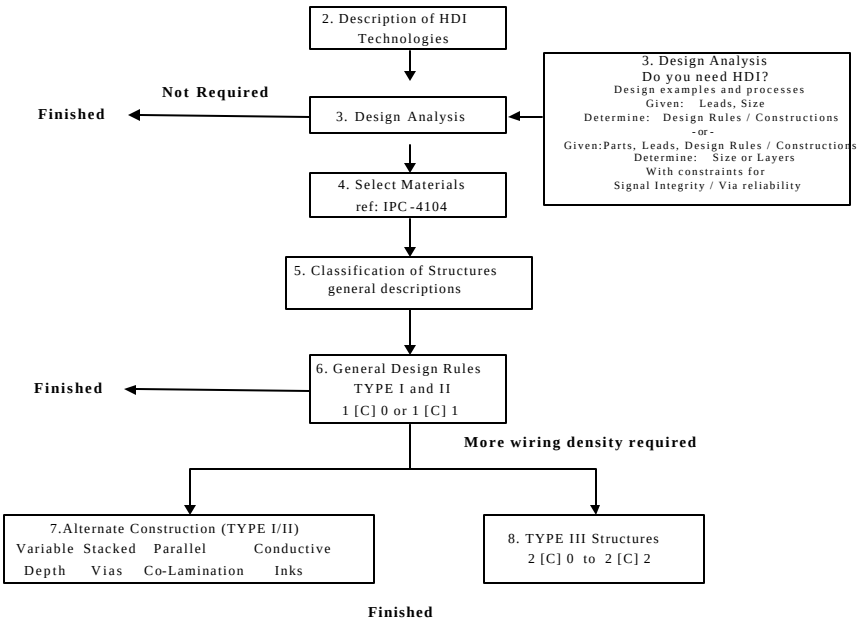
Three Cases of Wiring Demand

⌘ **Break-out from a component**

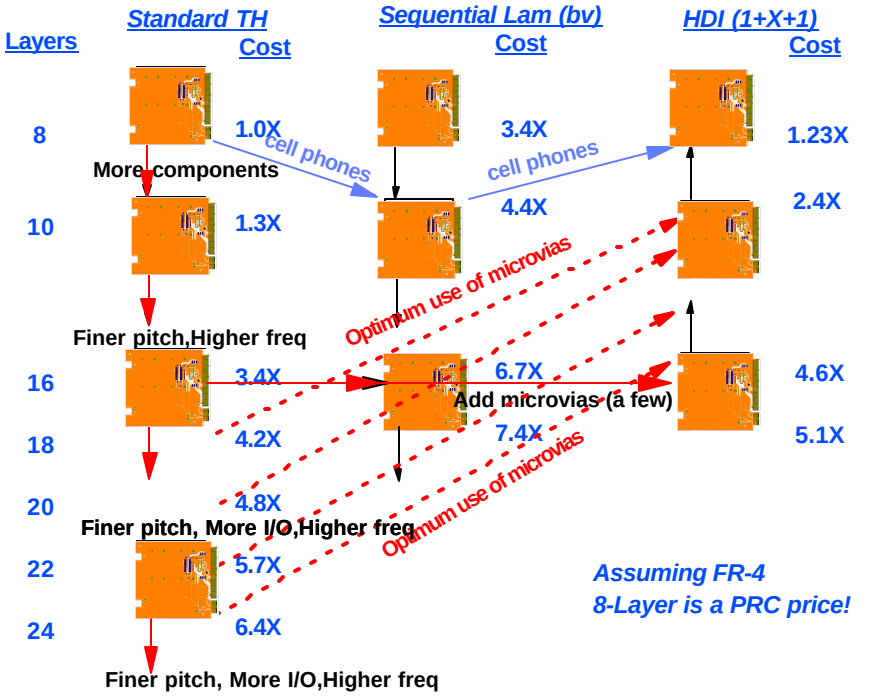
⌘ **Wiring between two or more tightly coupled components (CPU & cache)**

⌘ **The demand produced by all components on both sides of a board**

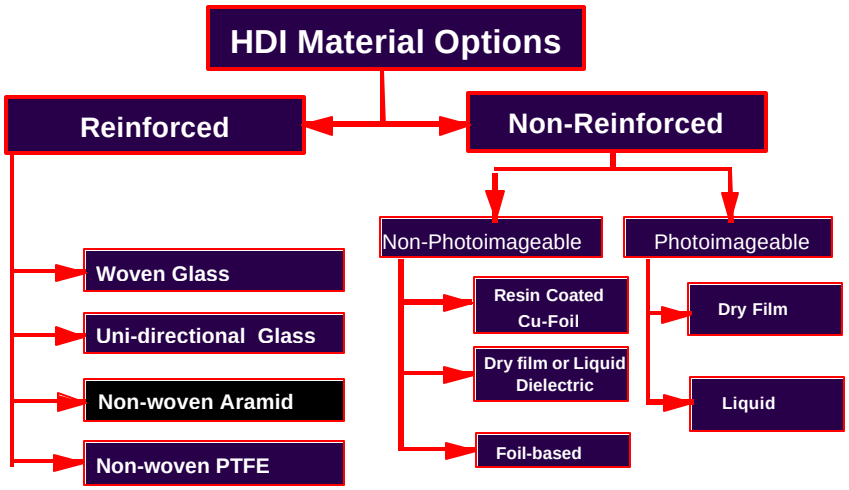
FLOWCHAT OF HDI DESIGN GUIDELINE



Layout Evolution (Jump the Gap)



Material Options by Reinforcement

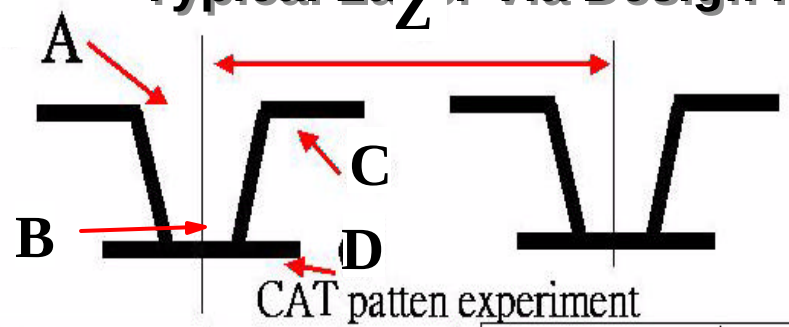


Laser Via Materials

Laser material table

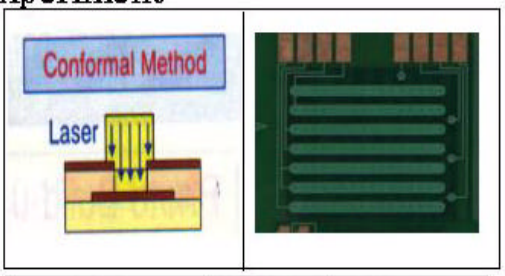
MATERIAL		PHOTO
FR4 Tg (140) FR5 Tg (170)	1080 1080X2 2112 2116	
Nanya RCC Kyocera HF RCC	60um 80um 60+80um	
Aramid pp	75um 75+75um	

Typical Laser Via Design Rules



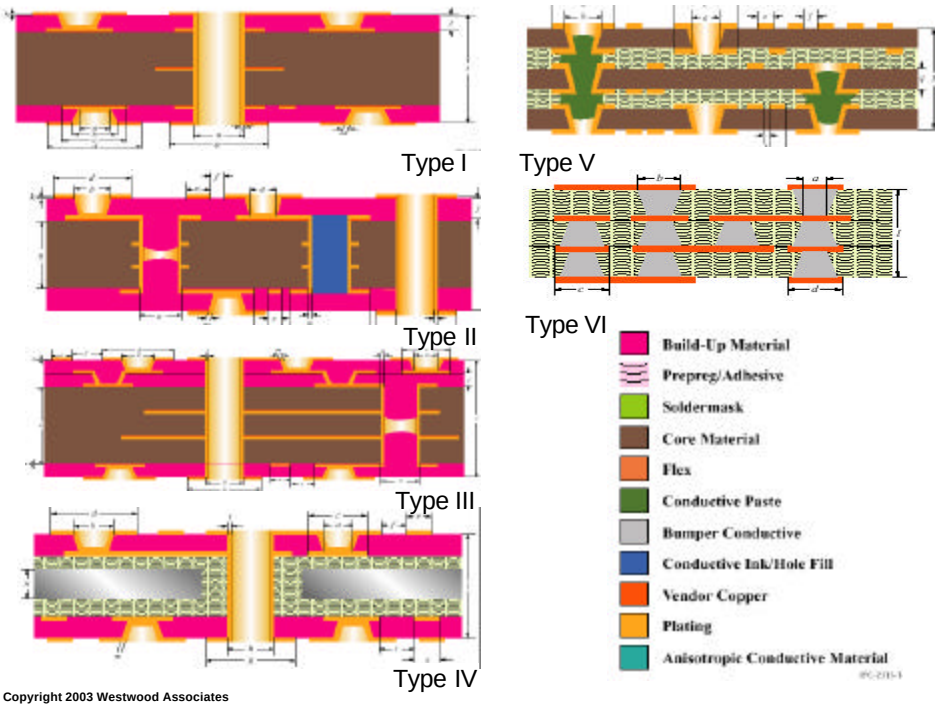
CAT patten experiment

ITEM		ABILITY
Laser via diameter	A B	4mil(min)
O/L pad	C	10mil
I/L pad	D	10mil
BGA Via to via pitch	Z	16mil (mil) (0.4mm)



SPEC	DR+6MIL	DR+8MIL
YIELD SIZE(19X22)	98%	100%

IPC-2226 HDI Constructions



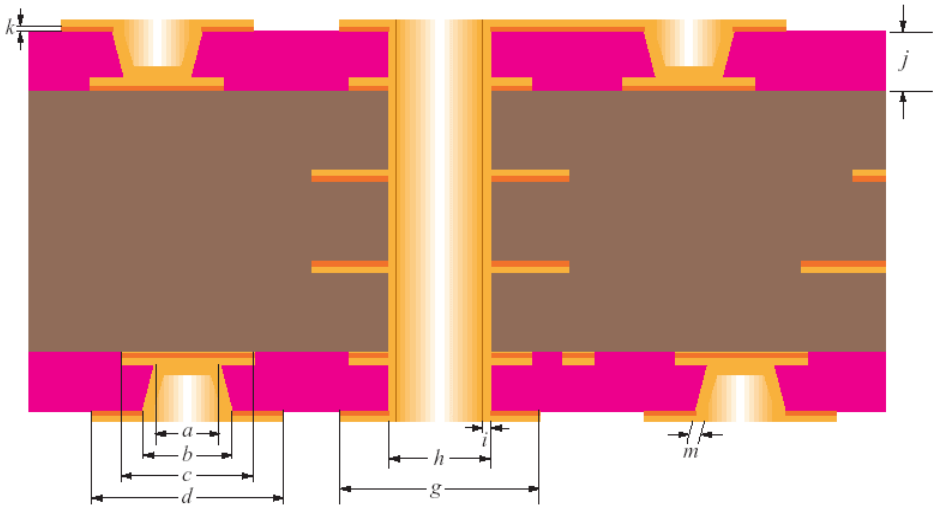
Design Guidelines

Symbol	Feature	Level A	Level B	Level C
a	Microvia diameter at target land (as formed, no plating)	102 µm [4 mil]	76 µm [3 mil]	51 µm [2 mil]
b	Microvia diameter at capture land (as formed, no plating)	152 µm [6 mil]	127 µm [5 mil]	76 µm [3 mil]
c	Microvia target land size = [(a + 2x annular ring) + FA (1)	406 µm [16 mil]	330 µm [13 mil]	229 µm [9 mil]
	FA for c =	203 µm [8 mil]	152 µm [6 mil]	102 µm [4 mil]
d	Microvia capture land size = [(b + 2x annular ring) + FA (1)]	406 µm [16 mil]	330 µm [13 mil]	229 µm [9 mil]
	FA for d =	203 µm [8 mil]	152 µm [6 mil]	102 µm [4mil]
s	Internal conductor trace width	127 µm [5 mil]	75 µm [3 mil]	50 µm [2 mil]
t	Internal conductor spacing	127 µm [5 mil]	100 µm [4 mil]	50 µm [2 mil]
e	External conductor trace width	127 µm [5 mil]	75 µm [3 mil]	45 µm [1.77 mil]
f	External conductor spacing	127 µm [5 mil]	100 µm [4 mil]	45 µm [1.77 mil]
g	Through via land size = [(h + 2x annular ring width) + FA (1)]	See 9.1.1 of IPC-2221	See 9.1.1 of IPC-2221	See 9.1.1 of IPC-2221
h	Through via diameter (as formed, no plating)	See Table 5-2	See Table 5-2	See Table 5-2
i	Minimum through via hole wall plating thickness	See IPC-2221, Table 4-3	See IPC-2221, Table 4-3	See IPC-2221, Table 4-3
j	Dielectric thickness (HDI blind microvia layer) (2)	64	64 µm [2.5 mil]	<50 µm [2 mil]
k	External Cu foil thickness (if Cu foil utilized)	1/2 oz (See IPC-2221, Table 10-2)	3/8 oz (See IPC-2221, Table 10-2)	1/4 oz (See IPC-2221, Table 10-2)
m	Minimum blind microvia hole plating thickness	10 µm [0.3937 mil]	10 µm [0.3937 mil]	15 µm [0.5906 mil]
m'	Minimum buried microvia hole plating thickness	10 µm [0.3937 mil]	10 µm [0.3937 mil]	15 µm [0.5906 mil]
n	Minimum buried via hole wall plating thickness	See IPC-2221, Table 4-3	See IPC-2221, Table 4-3	See IPC-2221, Table 4-3
o	Buried via diameter (as formed, no plating)	See IPC-2221, Table 9-4	See IPC-2221, Table 9-4	See IPC-2221, Table 9-4
p	Buried via land size = [(o + 2X annular ring) + FA (1)]	See 9.1.1 of IPC-2221	See 9.1.1 of IPC-2221	See 9.1.1 of IPC-2221
q	Buried via core thickness (excluding outermost conductors)	75 µm [3 mil]	63 µm [2.5 mil]	<63 µm [2.5 mil]
r	Buried via Cu foil thickness (outermost layer)	1/2 oz (See IPC-2221, Table 10-2)	3/8 oz (See IPC-2221, Table 10-2)	1/4 oz (See IPC-2221, Table 10-2)
u	Core board thickness (excluding conductors)	75 µm [3 mil]	63 µm [2.5 mil]	<63 µm [2.5 mil]
	Staggered via pitch	(p+c)/2	(p+c)/2	(p+c)/2

1. F.A. = Fabrication Allowance which considers production master tooling and process variations required to fabricate printed boards.
2. Measured from top surface of Layer 2 Cu to bottom surface of Layer 1 Cu.

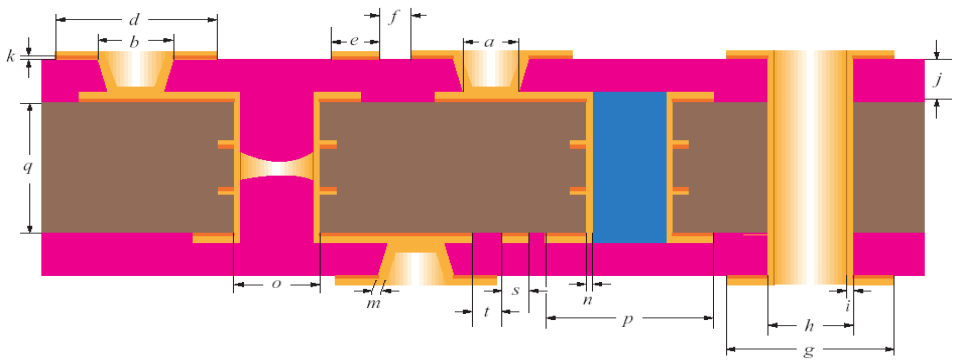
Design Guidelines

TYPE -I
Through-Hole Vias



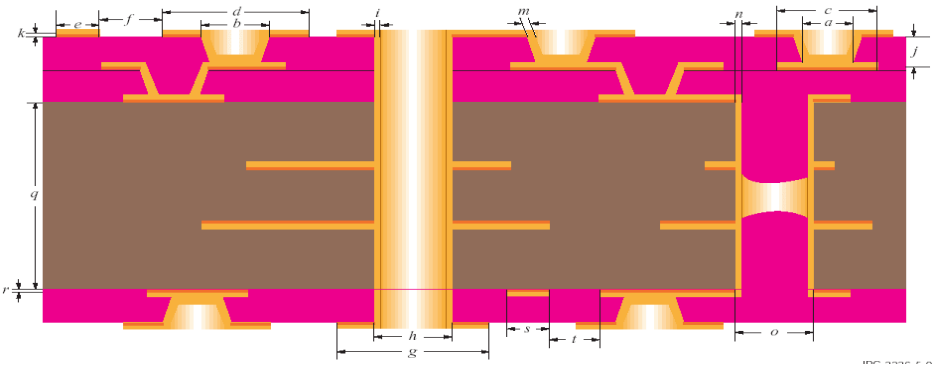
Design Guidelines

TYPE -II
Buried Vias



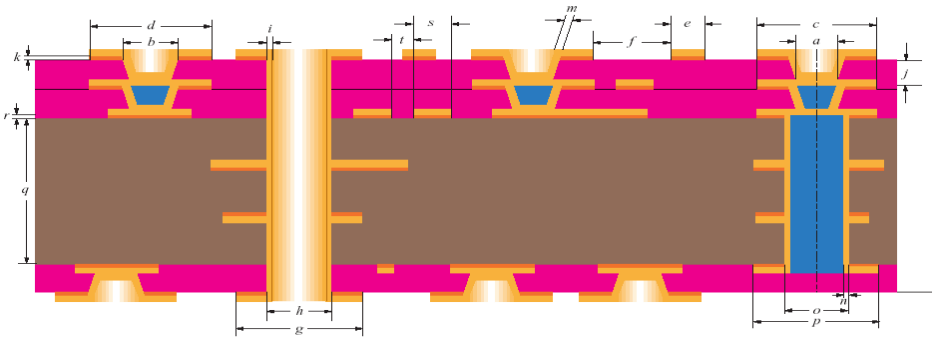
Design Guidelines

TYPE -III
Multiple Build-Up w/Buried vias



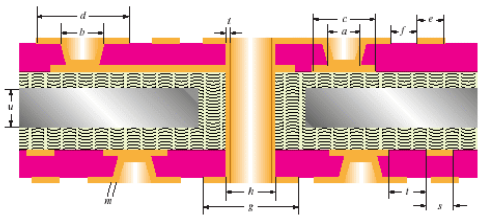
Design Guidelines

TYPE -III w/stacked vias



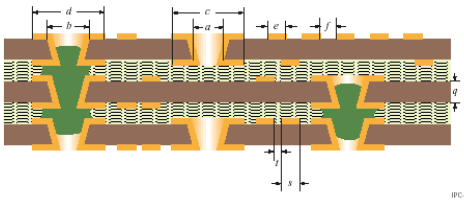
Design Guidelines

TYPE -IV (European)



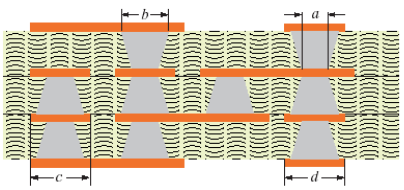
ure 5-7 Type IV HDI Construction

TYPE -V (Ormet)

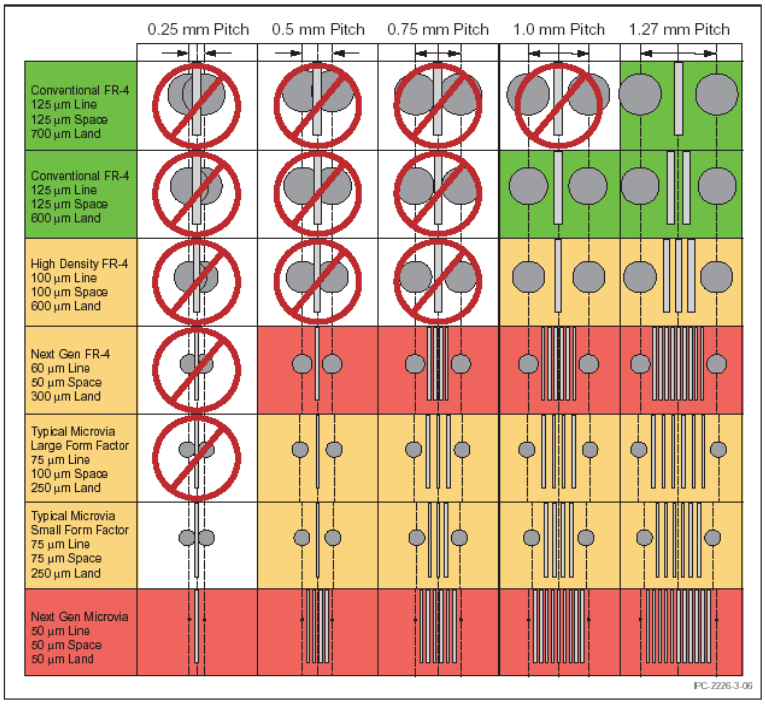


ure 5-8 Coreless Type V HDI Construction

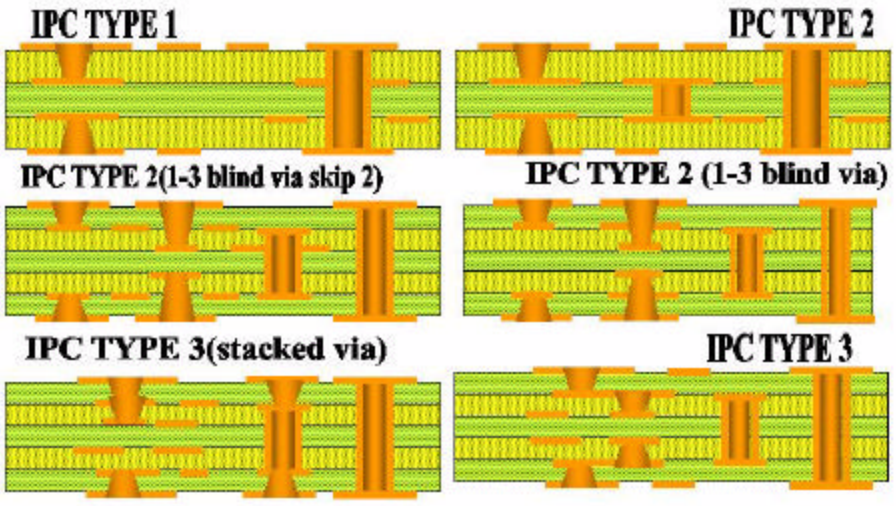
TYPE -VI (ALIVH)



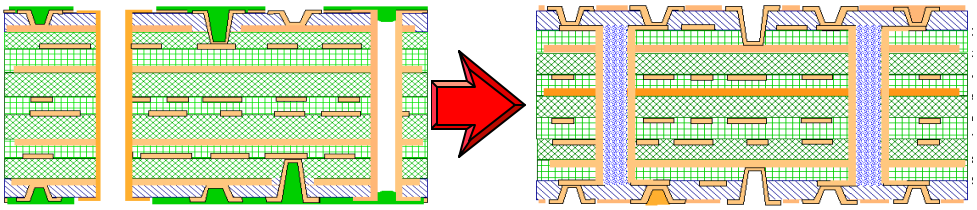
Design Guidelines



IPC HDI TYPE



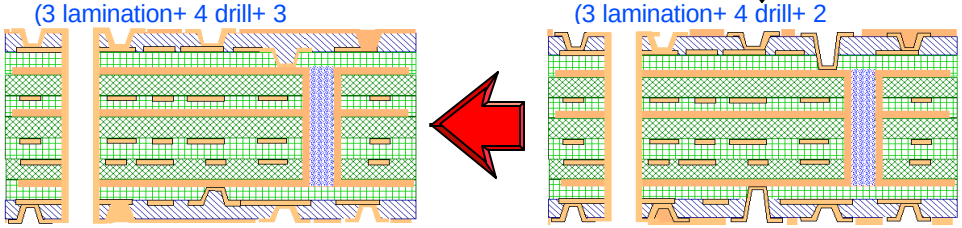
Esculation Progression



10 layer Type I (1+8+1)
(1 lamination+ 2 drill+ 1 plating)

10 layer Type II (1+8+1)
(2 lamination+ 4 drill+ 2 plating)

(3 lamination+ 4 drill+ 2



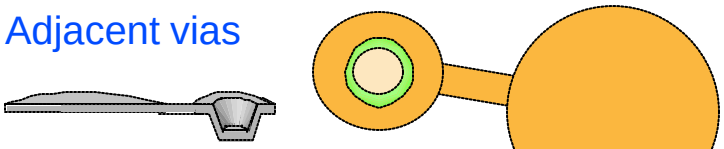
(3 lamination+ 4 drill+ 3

10 layer Type III (2+6+2)

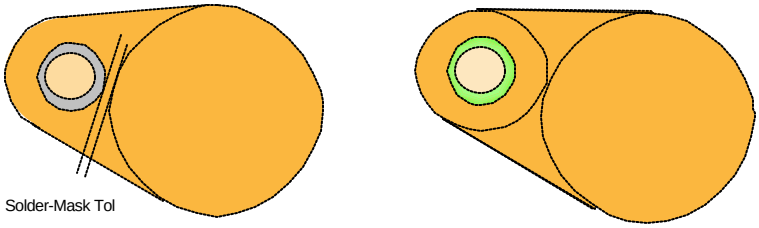
10 layer Type I (1+1+6+1+1)

HDI MicroVia Structures

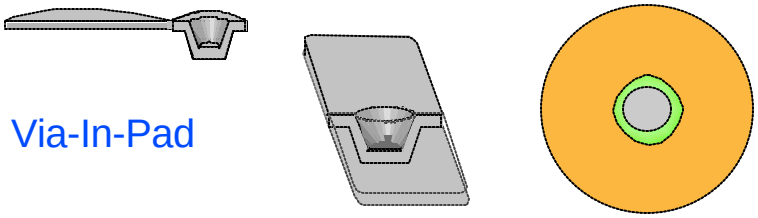
Adjacent vias



Inset vias

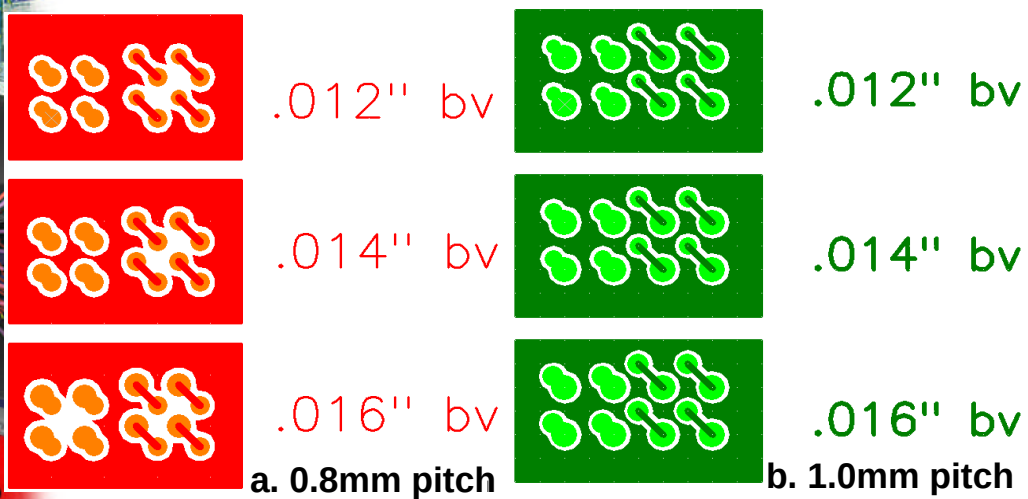


Solder-Mask Tol



Via-In-Pad

HDI MicroVia Structures (NVIP)



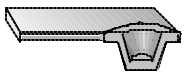
a. 0.8mm pitch

b. 1.0mm pitch

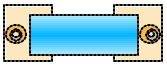
Near via-in-pad allows plane fill but without the assembly via fill need

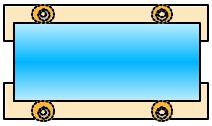
HDI MicroVia Structures (SMT Chip)

Edge of via hole is .001" away from device body outline



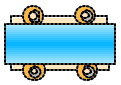
Via is tangential to inside edge of device pad farthest away from device center





0402

0306

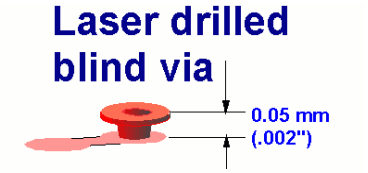


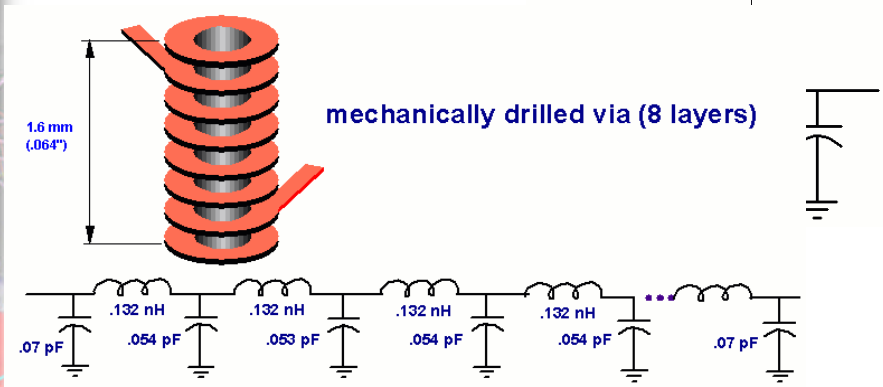
0603

0612

2-microvias in parallel cancels the mutual-self inductance

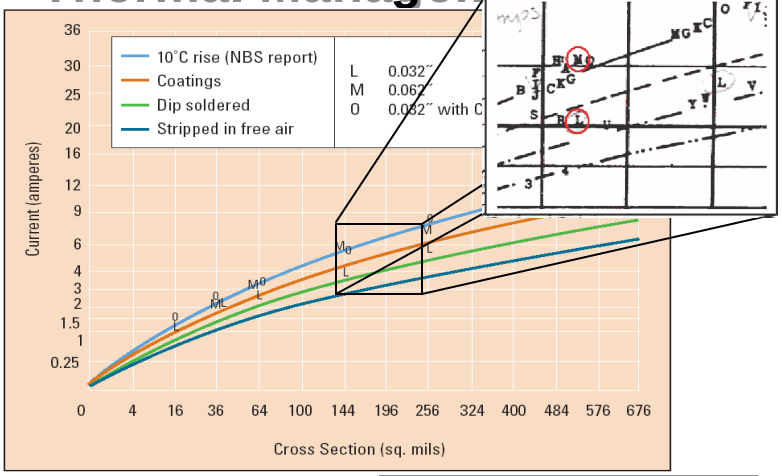
Electrical Performance



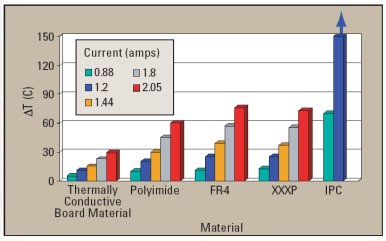


Thermal Management

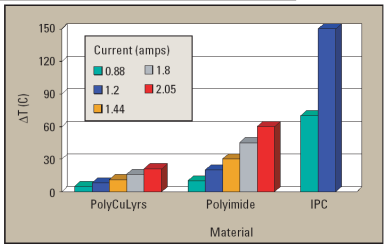
New Data on current carrying vs.PCB thickness for IPC-2152



Material thermal conductivity impact

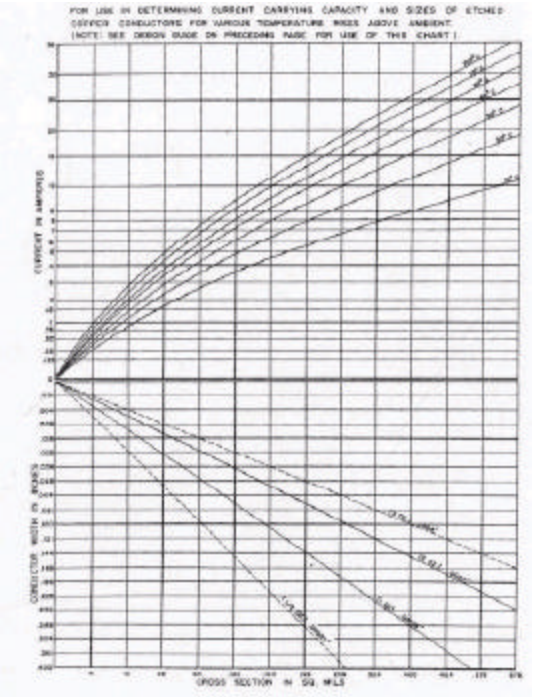


Composite thermal conductivity



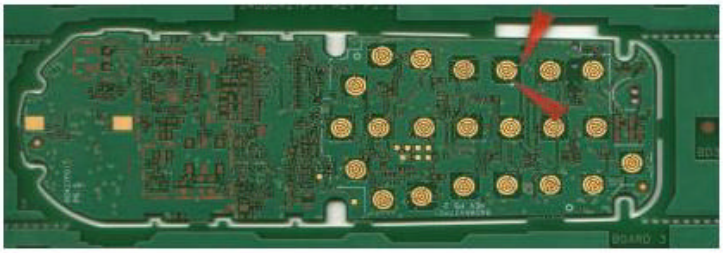
Thermal Management

IPC-2221 Current carying capacity chart is being replaced by IPC-2152



HDI Surface Treatments

Method: a: Immersion silver
b: Immersion tin
c: HASL
d: ENTEK
e: Electroless Ni/Au
F: Selective electroless Ni/Au



How To Get Started in HDI With Microvias

1. Do you need HDI?

- Density
- Fine-pitch BGAs
- High I/O area Arrays

2. OK - You Do !

- IPC Standards: 2315, 4104, 6016
- Select Materials (IPC-4104)
- Determine Stackup and Design Rules: (IPC-2315)
- Layout Efficiency
- Evaluate Fabricators (IPC-9151)

3. Start with a test vehicle

- Learn to assemble and test
- HDI Reliability
- Validate higher electrical performance

4. Redesign a HLC Board

- Gain volume experience

5. Pick a Project or Candidate for HDI

- Evaluate CAD limits and issues
- Channel routing
- Surface ground planes
- Auto routing tuning

FINISH