Presented at IPC Printed Circuits Expo®
SMEMA Council APEX®
Designers Summit 04

Study of SMT Assembly Processes for Fine Pitch CSP Packages

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Abstract

The SMT (surface mount technology) assembly process for 0.4 mm pitch CSP (chip scale package) components was studied in this work. For the screen printing process, the printing performance of different solder pastes, aperture shapes and sizes was investigated. Square apertures and a fine particle size in the solder paste provided a better paste release. Besides optimizing the printing process capability and minimizing the printing defects such as bridging and missing paste, the total volume of solder consisting of the paste and the solder ball has to be considered in order to maximize the final process yield.

For the pick & place process, the accuracy required for the placement equipment was determined by studying the self-alignment of the lead-free CSPs (with Sn/4.0Ag/0.5Cu balls) during the reflow process using lead-free Sn/3.9Ag/0.6Cu paste. The components were intentionally misplaced up to ~50% off-pad. After reflow, the x-ray inspection showed that the components had aligned to the pad. By considering the stack-up of the PCB (printed circuit board) pad location and size tolerances, the solder paste printing tolerances and the placement tolerances, the required alignment accuracy for the pick & place equipment was established to meet the total process capability requirement.

Introduction

Miniaturization and the integration of a growing number of functions in portable electronic devices require a high packaging density for electronic components. One way to increase the packaging density is to reduce the size of the packages and at the same time increase the density of the I/Os. This means that the size and pitch of leads, solder balls or pads in electronic component packages will continue to shrink.

The use of fine pitch components poses a number of challenges for the SMT (surface mount technology) assembly process. First, a feasible screen printing process must be achieved. For reliable interconnections, a sufficient amount of paste is needed and the variations in the solder paste volume have to be minimized. Many factors influence the quality of the screen printing process. The basic factors are stencil thickness, stencil type, paste characteristics, paste type (particle size) and screen printing parameters such as printing speed, pressure and separation speed. Other factors such as the mechanical condition of the stencil, cleaning frequency, flatness of the printed circuit board, and the method of supporting the PCB (printed circuit board) during the screen printing process also contribute to the process capability.

The next questions concern the pick & place process. The capability of the current equipment for an accurate and repeatable alignment has to be verified. The required placement accuracy depends on the ability of the components to self-align during the reflow process. Theoretically, the self-alignment is determined at least by the solder paste composition (eutectic Sn/Pb versus lead-free),[1] reflow atmosphere[1] which may change the surface tension of the solder, PCB surface finish and the ratio of the component weight versus the soldered area.

The first objective of this work was to establish printed circuit board design rules and recommendations that allow a reasonable PCB cost and a high assembly process yield. The second task was to evaluate and develop screen printing and pick & place processes for 0.4 mm pitch CSP components.

Test Vehicle and Components

A test vehicle (Figure 1) was designed for the project. The overall size of the vehicle was (310 x 145 x 1.0) mm and it was divided into four boards of equal size. Furthermore, board areas were divided into eight different sections. Each section was designed for a specific purpose, for example to study different pad types, pad sizes, or stencil aperture sizes regarding their assembly process or reliability performance.

The test vehicle had six copper layers as shown in Figure 2. The core material was FR-4 laminate, and several build-up materials were used for the outer layers. The nominal diameter of the microvias was 75 µm.

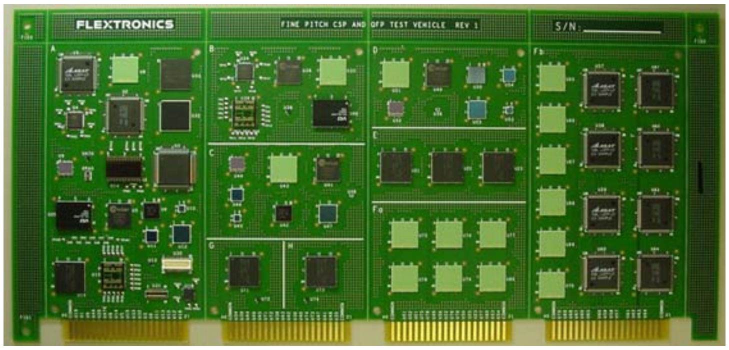

Figure 1 – Test Vehicle

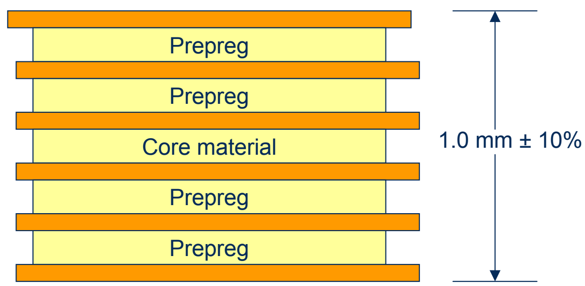

Figure 2 – A Schematic Illustration of the Build-up Layers of the PCB

The description of the 0.4 mm pitch CSP (chip scale package) components used in the study is provided in Table 1. The solder balls of CSP I and CSP II were arranged in four arrays at the perimeter, whereas the other CSPs were of full array type. Full array was possible because the components were only daisy-chained. For functional components, the number of arrays would be more limited due to PCB routing issues.

Table 1 – Description of the Fine Pitch Components

Name	Type/ description	Body size (mm x mm)	I/O count	Pitch (mm)
CSP I	Plastic package	10 x 10	288	0.4
CSP II	Wafer-level	7 x 7	192	0.4
CSP III	Wafer-level	2.4 x 2.4	34	0.4
CSP IV	Wafer-level	4.8 x 4.8	136	0.4
CSP V	Wafer-level	7.2 x 7.2	306	0.4

Furthermore, the influence of the PCB pad type was studied. The test vehicle included three different pad types: NSMD (non-solder mask defined), SMD (solder-mask-defined) and “Window” (no solder mask between the pads). The details of the layouts are provided in Figure 3. SMD pad design is generally not recommended, but was included because these pads are not as easily ripped off as the NSMD or “window” ones during rework.

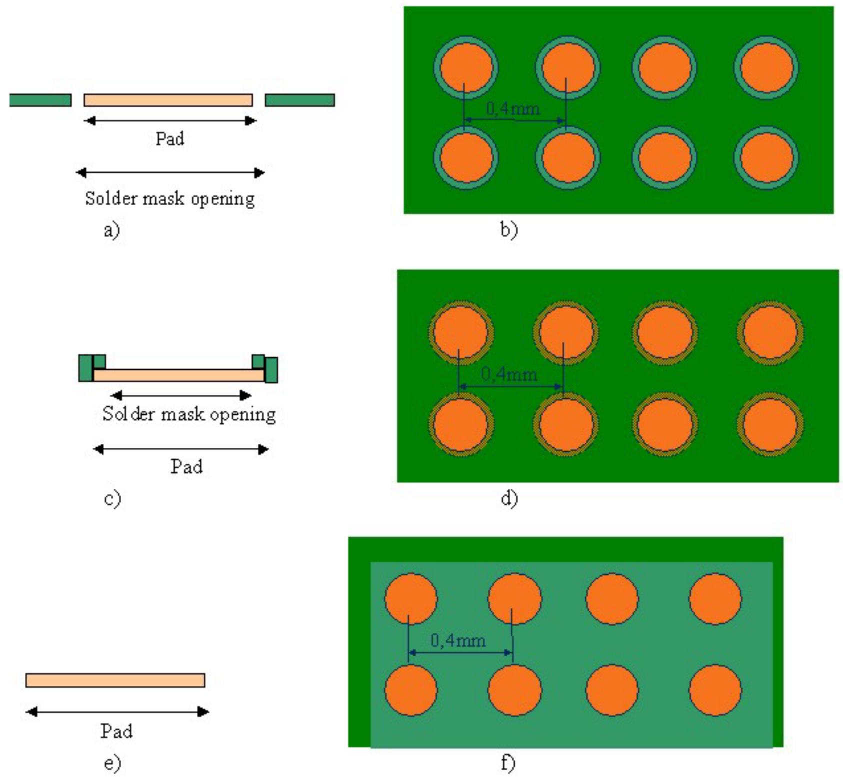

Figure 3 – Schematic Illustrations of the Three Different Pad Designs Studied, a) NSMD, Side View, b) NSMD, Top View, c) SMD, Side View, d) SMD, Top View, e) "Window," Side View, f) "Window," Top View

Solder Pastes and Stencils

Four different solder pastes were chosen for the study. Three of them had a eutectic Sn/Pb composition and one a Sn/Ag/Cu - composition. Two of the pastes had a particle size of type 4 and two of type 3. Pastes C and D had the same flux chemistry but a different particle size and a slightly different metal content. A summary of the solder paste properties is provided in Table 2.

Table 2 - Properties of the Solder Pastes

	Paste A	Paste B	Paste C	Paste D
Composition	Sn/3.9Ag/0.6Cu	Sn/37Pb	Sn/37Pb	Sn/37Pb
Metal content (wt-%)	88	90	90	89.5
Flux classification per J-STD-004	ROL0	ROL0	ROL0	ROL0
Particle size	Type 4	Type 3	Type 3	Type 4

Regarding the stencil, the target was to be able to use a 125 µm (5 mil) thick, laser-cut and electropolished stencil as this is considered as a low-cost option for volume manufacturing. From previous experience and earlier studies, it was known that electroformed stencils and stencils having a lower thickness could possibly perform better than the 125 µm, laser-cut and electropolished one.[2] However, in actual applications, thinner stencils may not be able to provide sufficient solder paste volume for the other components on the board, and electroformed stencils generally cost more than laser-cut stencils.

Different stencil aperture sizes and shapes were investigated. Both round and square apertures were included, sizes ranging from 250 µm to 305 µm. The combinations of aperture shapes, sizes and area ratios are shown in Figure 4. The area ratio (AR) is defined as the ratio of the opening area of the aperture to the wall area of the aperture.

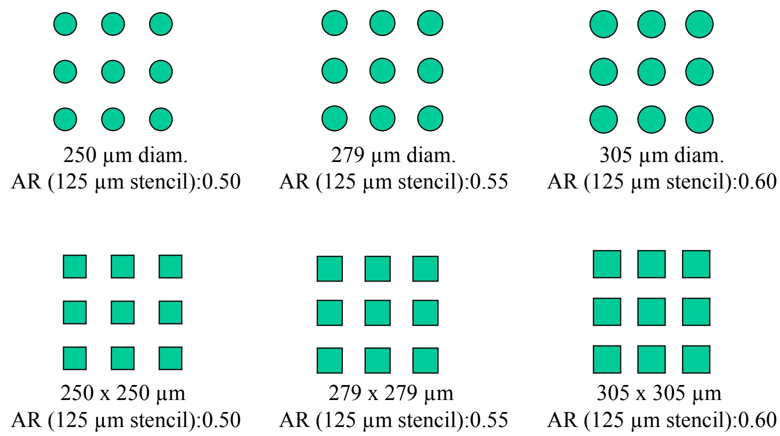

Figure 4 – Stencil Aperture Shapes, Sizes and Area Ratios Studied for 0.4 mm Pitch CSP Components

Reflow Process

Reflow was carried out in air atmosphere, in a reflow oven typically used for high-volume electronics manufacturing with eight heating zones and one cooling zone. The lead-free temperature profile used for Sn/Ag/Cu solder is shown in Figure 5. Three of the thermocouples (#1, #2, and #3) were measuring solder joint temperatures and one was monitoring the air temperature in the oven.

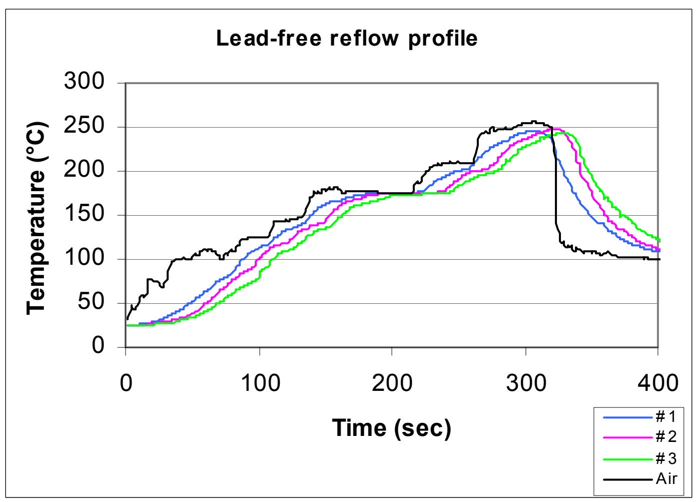

Figure 5 - Lead-Free Reflow Profile

Printed Circuit Board Design Considerations

0.4 mm pitch CSP is pushing the limits of the capability of the current PCB fabrication processes. At the beginning of the project, two different pad designs were considered – one with a microvia in pad (Figure 6) and another without microvias (Figure 7). It turned out that only the microvia-in-pad option was possible for this fine pitch; otherwise, the minimum required clearances between the vias and CSP pads could not be met. Further, there is no possibility to route a trace between the pads with 0.4 mm pitch CSPs because of the minimum required gap between traces and pads and the minimum trace width. In addition, if traces were routed between pads, they would need to be covered by the solder mask. The adhesion of this fine strip of solder mask, so called "sliver", on top of a trace would also be questionable.

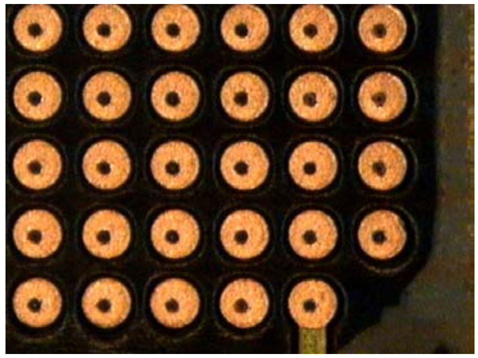

Figure 6 - An example of the PCB Layout for 0.4 mm Pitch CSP (Microvia In Pad)

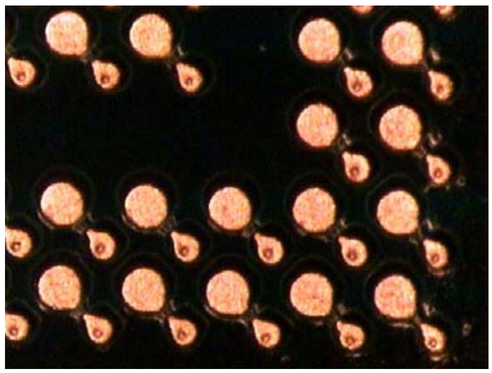

Figure 7 – An Example of the PCB Layout for 0.5 mm Pitch CSP (No Via In Pad)

Screen Printing Process
The objective was to establish a viable paste printing process for fine pitch components. The criterion for a successful paste printing process was that a Cp value of 1.33 should be achieved with an upper tolerance limit of +50% and a lower tolerance limit of –50% of the average measured volume and that no bridges should be formed during the paste printing. A regular screen printer and metal squeegees at 60° were used for paste printing.

A. Optimization of screen printing parameters
First, the printer settings were optimized with a DOE using pastes B and C. The same settings were found to be the best for both pastes, and these settings were used throughout the rest of the study for all pastes. The printing pressure was set at 10 kg, printing speed at 20 mm/min and separation speed at 1.0 mm/sec.

B. Comparison of the performance of different solder pastes
In the second phase, the performance of the different pastes was compared as shown in**Table 3**. One of the main interests was to see whether the particle size of the paste would make a difference. For calculating the average volume and the Cp value, the average volume of solder paste on the six different stencil designs (Figure 4), on a total of 12168 pads, was included.

No missing solder, judged as less than 5 paste particles on a pad, was found in these samples.

As can be seen from Table 3, all of the pastes exceeded the minimum Cp requirement of 1.33, and a finer particle size provided a better paste release and a higher Cp value. At the same time, a finer particle size resulted in slightly more bridging. Pastes of type 4 can be more expensive and may be more prone to solder balling,[2,3] and therefore type 3 pastes are often preferred. In this work, paste A was used for further investigations.

C. Comparison of the printing performance of different stencil apertures
For each aperture, more than 4000 pads (half of which of NSMD type and half of SMD type) were inspected. The data collected for the 5 mil thick stencil is shown in Table 4. No missing paste on these samples was found.

Table 3 – Comparison of the Performance of the Solder Paste - Stencil: 125 mm Thick, Laser-Cut and Electropolished

	Particle size	Average volume (μm³)	Cp volume	Bridged pads after paste printing
Paste A	Type 4	$7.32*10^6$	2.25	0.23%
Paste B	Type 3	$5.59*10^6$	1.48	0.00%
Paste C	Type 3	$6.57*10^6$	1.40	0.07%
Paste D	Type 4	$6.89*10^6$	1.86	0.12%

Table 4 – Comparison of Stencil Apertures for 0.4 mm Pitch CSP COMPONENTS USING 5 mil Thick, Laser-Cut and Electropolished Stencil and Paste A

Aperture	Average volume (μm³)	Cp volume	Bridged pads after paste printing
Round 250 μm diam.	$4,75*10^6$	1,18	0%
Round 279 μm diam.	$6,07*10^6$	1,97	0%
Round 305 μm diam.	$7,98*10^6$	2,39	0,69%
Square 250 x 250 μm	$6,62*10^6$	2,43	0%
Square 279 x 279 μm	$7,94*10^6$	2,53	0%
Square 305 x 305 μm	$10,60*10^6$	2,87	0,49%

As can be seen from Table 4, the round and square 305 μm apertures resulted in the largest solder paste volume and consequently more bridging after the paste printing. Square apertures generally provided a more stable printing process than the round apertures, also reported in earlier studies.[4] Although only the results with paste A are presented in Table 4, the results were fully consistent with the other pastes, with the square 279 x 279 μm aperture giving the best overall paste printing results.

D. Selection of stencil aperture for 0.4 mm pitch CSP components based on screen printing performance and assembly process yield

With 0.5 mm (and above) pitch CSPs, reaching a screen printing process that provides the desired Cp value and no bridging after printing has been sufficient. The square 279 μm aperture appears to meet this criterion. However, during this study, it was found that with 0.4 mm pitch CSPs, the total volume of solder is also critical. With the square 279 μm stencil aperture and paste A, although no bridging occurred after paste printing or after the pick & place process, bridging was commonly observed after the reflow process. This means that the total volume of solder, made up by the paste and the ball on the component, was too large in proportion to the gap between the solder joints. Finally, only square 250 μm and round 279 μm apertures were found to be feasible for 0.4 mm pitch CSP components with paste A.

PCB Design

The PCB pad designs were compared based on the assembly yield measured through electrical daisy-chain continuity measurements. A slightly lower yield was observed for the "window" design (**Table 5**). The cause was identified as insufficient solder (Figure 8). The reason is assumed to be the gasketing of the stencil during screen printing. The "window" design does not provide as solid gasketing as the NSMD or SMD designs, which can result in a bigger variation in the solder paste volumes.

Table 5 – Electrical Yield after Assembly versus Different PCB Pad Designs

Pad design	Number of components assembled	Yield, %
NSMD	98	99
SMD	140	99
"Window"	83	94

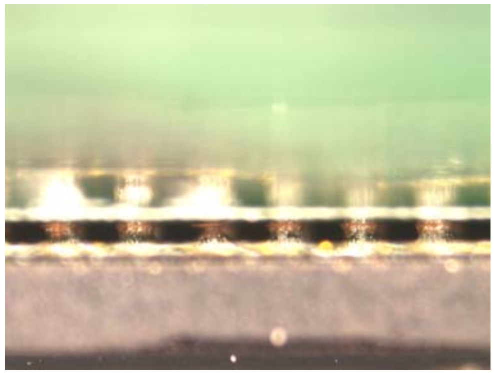

Figure 8 – Example of Open Solder Joint with "Window" PCB Pad Design - The Open Joint is Third from the Left

Pick & Place Process

The objective was to determine the required accuracy for the pick & place equipment to place the fine pitch CSP components. For that purpose, the self-alignment of misplaced components during reflow was studied with CSPs with Sn/4.0Ag/0.5Cu balls reflowed on Sn/Ag/Cu paste. The components were misplaced 25% and 50% off-pad. The result after reflow was considered acceptable if the registration after reflow was straight and there was no pad overhang or rotation.[5]

Figure 9 is the x-ray image of the assembly after the pick & place process, where the CSP component was intentionally misplaced by ~50% off-pad.

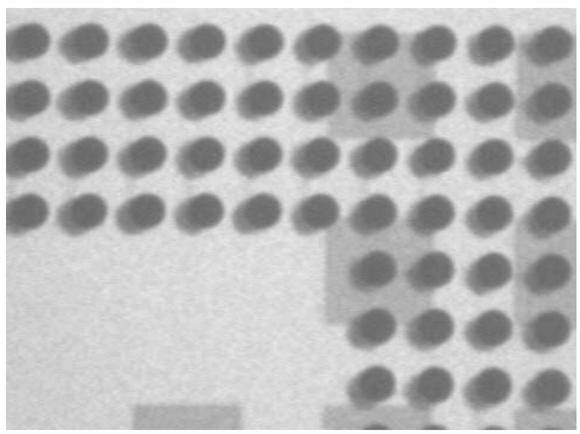

Figure 9 - 0.4 mm Pitch CSP Misaligned ~50% in Pick and Place Process Using CSP with Sn/Ag/Cu Balls and Sn/Ag/Cu Paste

Figure 10 is the x-ray image of the misplaced component after reflow. It can be seen that the component has fully self-aligned. Therefore it can be concluded that up to ~50% misalignment can be accepted in the pick & place process. It is important to note, however, that these results may not always apply. If, for example, the number of solder balls is small as compared with the size or weight of the components, a weaker self-alignment would be expected.

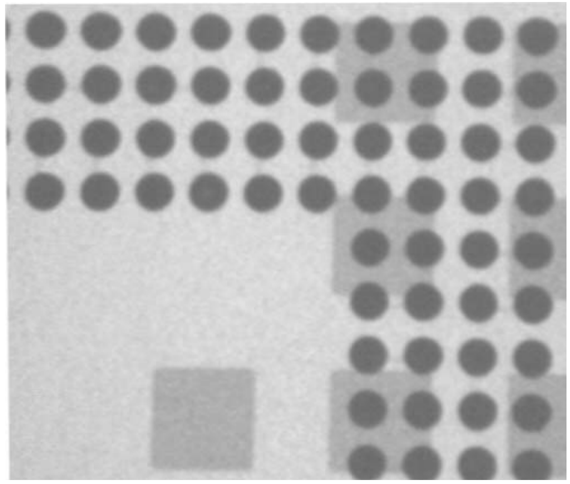

Figure 10 - 0.4 mm Pitch CSP, Misaligned ~50% in Pick & Place Process, after Reflow, Using CSP with Sn/Ag/Cu Balls and Sn/Ag/Cu Paste

Required Placement Accuracy

To calculate the required placement accuracy to meet the 50% off-pad placement criterion, the tolerances of the pad position and width and of the solder paste printing process must be considered. A typical value for the pad width tolerance obtained from PCB manufacturers is ±30 µm, which yields ±15 µm on both sides of the pad. The pad position tolerance was assumed to be ±45 µm based on the size of the panel using global fiducials and based on current PCB fabrication capabilities for volume manufacturing. According to the specifications of some of the most common screen printers, the alignment tolerance of the solder paste is ~±25 µm.

In the following calculations, the tolerance of the CSP ball size was not considered since it is assumed that the CSP will self-align as long as the center of the ball touches the edge of the PCB pad. For simplicity, other possible tolerances such as the distortion of the fiducial marks of the PCB were considered to be of secondary importance and were left out from this investigation. If more accurate values are desired, these tolerances can be included. The solder mask registration tolerance was not included, as NSMD or "window" pad designs were of most interest in this study.

For 0.4 mm pitch CSP, the tolerance limits for placement accuracy are determined by the pad size. In the following calculations, pad size of 200 µm is used, giving +100 µm for the upper tolerance limit (UTL) and –100 µm for the lower limit, for 50% off-pad placement (Figure 11).

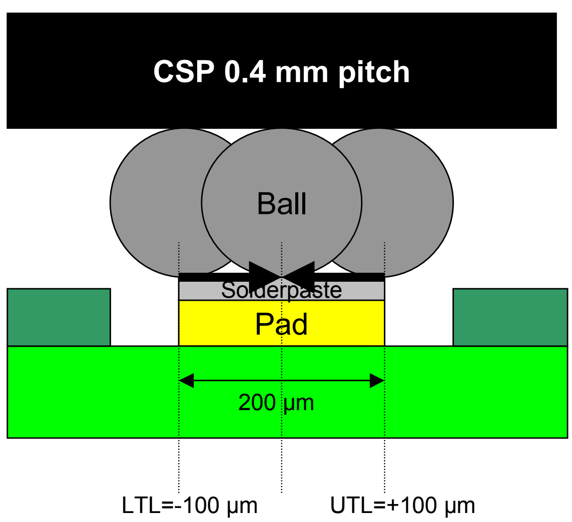

Figure 11 – Tolerance Limits for 0.4 mm Pitch CSP and 200 µm PCB Pad Size

To ensure a stable process, a Cp of 1,33 has to be obtained. The required tolerances to achieve this Cp value can be calculated as

$$\text{Required tolerances} = \frac{\text{Tolerance limits}}{C_p} \qquad [1]$$

In the case of 0.4 mm pitch CSP having 200 µm pad size, we get

$$\text{Required tolerances} = \frac{\pm 100\mu m}{1{,}33} = \pm 75\mu m \qquad [2]$$

The required tolerance includes the stack-up of all the different tolerance contributions. On Ni/Au (electroless nickel/immersion gold) finished PCBs, both the Sn/Pb and Sn/Ag/Cu solder pastes typically self-align to the pad. In this case, the solder paste alignment tolerance can be neglected and thus the tolerances consist of the pad width tolerance (Tol_1), pad position tolerance (Tol_2) and the placement tolerance (Tol_3). The required tolerance can be expressed as:

$$\text{Required tolerances} = \sqrt{(Tol_1)^2 + (Tol_2)^2 + (Tol_3)^2} \qquad [3]$$

Finally, we get for the placement tolerance:

$$Tol_3 = \sqrt{(\pm 75\mu m)^2 - (\pm 45\mu m)^2 - (\pm 15\mu m)^2} = \pm 58\mu m \qquad [4]$$

This analysis indicates that a placement accuracy of ±58 µm @3σ is required for the placement equipment for 0.4 mm pitch CSPs that are assembled on Ni/Au finished PCBs.

When Sn/Ag/Cu solder paste is used together with OSP (organic solderability protection) finished PCBs, besides the pad width/position tolerances (Tol_1, Tol_2) and the placement tolerance (Tol_3), the solder paste alignment tolerance (Tol_4) has also to be considered, because the solder paste does not self-align to the pad but rather stays where printed.[5] In this case, the required tolerance can be expressed as:

$$\text{Required tolerances} = \sqrt{(Tol_1)^2 + (Tol_2)^2 + (Tol_3)^3 + (Tol_4)^4} \qquad [5]$$

For the placement tolerance, we get:

$$Tol_3 = \sqrt{(\pm 75\mu m)^2 - (\pm 15\mu m)^2 - (\pm 45\mu m)^2 - (\pm 25\mu m)^2} = \pm 52\mu m \qquad [6]$$

This analysis indicates that a placement accuracy of ±52 µm @3σ is required for the placement equipment for 0.4 mm pitch CSPs that are assembled on OSP finished PCBs.

The placement capability of the pick & place equipment is, among other features, also determined by the resolution of the camera. Normally 4-5 pixels is required both in x and y directions for the camera to find a bump (Figure 12). Typically, for 0.4 mm pitch CSPs, the size of the bump base metal is ~200 µm. Therefore the resolution of the camera should be minimum 50 µm/pixel. Too low a resolution for the camera would have a negative impact on the reject rate and throughput since the equipment would not be able to find the bumps and therefore would reject the part.

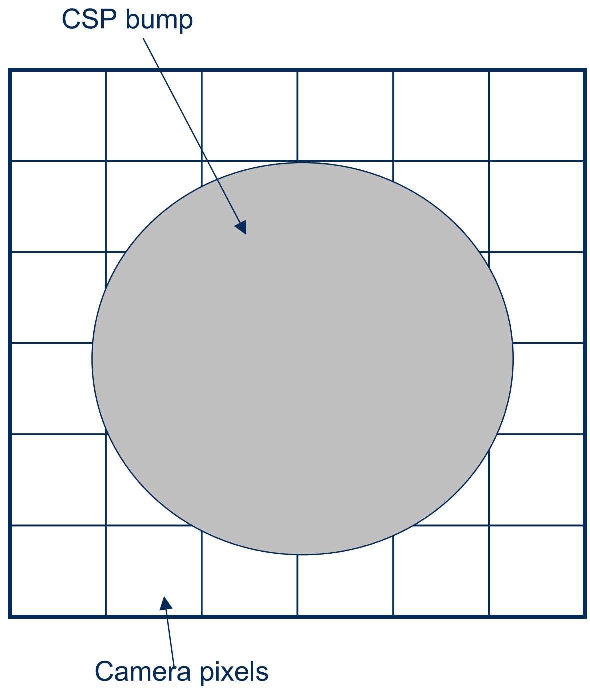

Figure 12 – A schematic Illustration of the Camera Pixels versus the Bump Size

Conclusions

It was shown that a new approach is required to optimize the screen printing process for 0.4 mm pitch CSP components. With this fine pitch, it is no longer sufficient to optimise only the printing process capability and minimize the printing defects such as bridging or missing paste. The total volume of solder consisting of the paste and the solder ball of the CSP component versus the gap between the solder joints has to be considered as well. Square 250 µm or round 279 µm apertures provided the best final process yield, although square 279 µm apertures provided the best screen printing process yield.

The capability of misplaced CSPs to self-align during the reflow process determines the required accuracy of the pick & place equipment. In the study, Sn/A4.0g/0.5Cu balled CSP components on Sn/3.9Ag/0.6Cu solder paste were intentionally misaligned up to ~50% off-pad. After reflow, the x-ray inspection showed that the components had aligned to the pad. By considering the PCB pad size/location tolerances, solder paste alignment tolerances and the total allowed process tolerance calculated from the targeted Cp value, the required alignment accuracy for the pick & place equipment was calculated to be ±52µm @3σ.

Acknowledgements

The authors would like to thank Alington Lewis and Hoang Phan at Flextronics San Jose, USA, for their assistance in the experimental work.

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