

## **Evaluation of Underfill Material on Board Level Reliability Improvement of Wafer Level CSP Component**

A.C. Shiah, Ph.D.  
Soletron Technical Center,  
Milpitas, CA

Tom Liu and Ken Lee  
Maktron Corp.  
Taoyuan, Taiwan

Y.S. Chen, Ph.D. and C.S. Wang  
Yuan Ze University  
Taoyuan, Taiwan

### **Abstract**

In recent years, Wafer Level Chip Scale Packages (WLCSP) are used not only in the hand held devices but also in high-end networking and telecommunication products. Due to their small footprint and the bare die structure, long-term board level reliability is a concern particularly in high-end applications. Using underfill material in these WLCSP components may present a possible solution for reliability improvement. Non-reworkable underfill material is generally used in low cost, small, hand-held devices for better reliability. However, in high end products with expensive boards, the option to rework WLCSP components need to be considered. It is therefore important that an underfill material with both good “reworkability” and “reliability” be identified. This paper examines the board level reliability improvement of six (four nonreworkable and two reworkable) underfill materials on 0.5 mm pitch WLCSP component. The possible correlation of different material properties to reworkability and reliability of the underfill material will be discussed. An underfill material with good reworkability may sacrifice the reliability at the same time. The findings have confirmed the fact that proper selection of the underfill material for small footprint WLCSP component can improve the reworkability and reliability in high end products.

### **Introduction**

The increasing demand to improve performance while decreasing real estate in Integrated Circuit (IC) designs has led to the popularity of 0.5 mm pitch Chip Scale Packages (CSPs). A Wafer Level Chip Scale Package (WLCSP), which involves the direct attachment of solder bumps on the silicon die in a wafer form, was developed to further reduce the size as well as the cost of the CSPs.<sup>1,2</sup> One new type of 0.5 mm WLCSP package contains solder balls that are about 50% larger in volume than the typical CSP component for this pitch. The footprints of these packages are only about half the size of a 0.8 mm-pitch CSP but they require much tighter control of the assembly process. The enlarged ball on a 0.5 mm pitch device introduces new challenges in the assembly process.

Recently, the WLCSP component was used not only in the hand held devices but also in high-end networking and telecommunication applications. In mixed technology high-end boards, the board is populated with different type of BGA, CSP, and WLCSP packages. The BGA type of component with larger ball diameter is theoretically more reliable than the small footprint CSP and WLCSP components during thermal cycling. Since maintain the overall reliability of a system is determined by its weakest component, it becomes very important to focus on increasing the board level reliability of the least reliable small footprint components. Previously, Soletron Technical Center (STC) has conducted board level reliability study of this WLCSP component without applying underfill material. The high volume production at Soletron manufacturing sites has proven the robustness of the optimized manufacturing process developed at STC.<sup>3,4</sup>

This paper focuses on the development of underfill process and the reliability improvement by using different underfill materials. The reliability tests done in this study can be classified into two categories: thermal stress tests (thermal cycling from -40 °C to 85 °C and 0 °C to 100 °C) and mechanical stress tests (shock, bend, and shear tests). Cross Section, SEM, EDX, and Dye-Pry techniques were used to understand the failure modes of solder joints induced by the destructive thermal or mechanical stress tests.

### **Description of the Test Vehicle**

Traditionally, the ball diameter of a 0.5 mm pitch CSP package is 0.3 mm. A 0.35 mm WLCSP with oversized ball was introduced to improve electric performance and board level reliability (see Figure 1). The component specification is outlined in Figure 2.

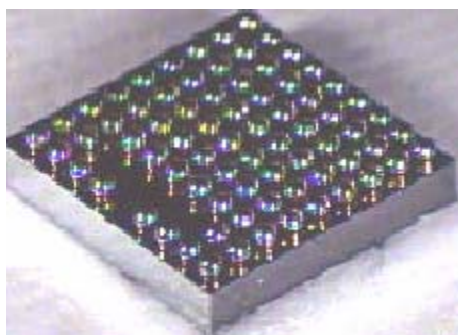


Figure 1 – 0.5 mm WLCSP bottom Side View

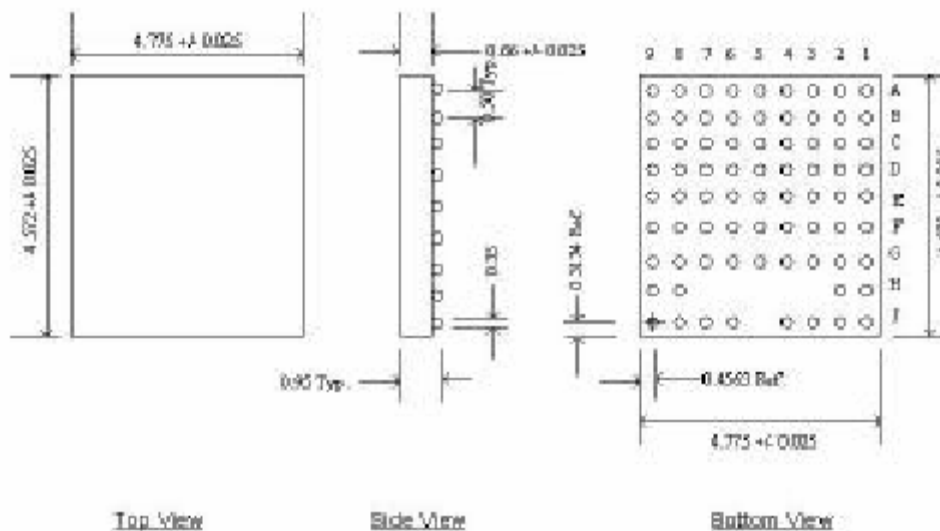


Figure 2 – Physical Dimensions

The test vehicle has only one daisy chain connection (from A6 to A8) through the entire package as seen in Figure 3. The test pads are designed to extend to the edge of the package to facilitate the detection of open solder joints. The test board is 62-mil thick with immersion Ag finish and Solder Mask Defined (SMD) pads (see Figure 4). The information of solder paste, stencil design, and PCB are shown in Table 1.

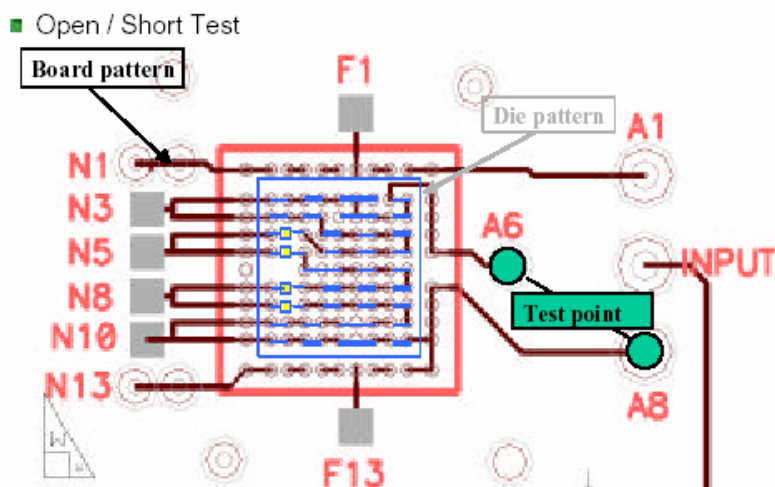


Figure 3 – Daisy Chain Design

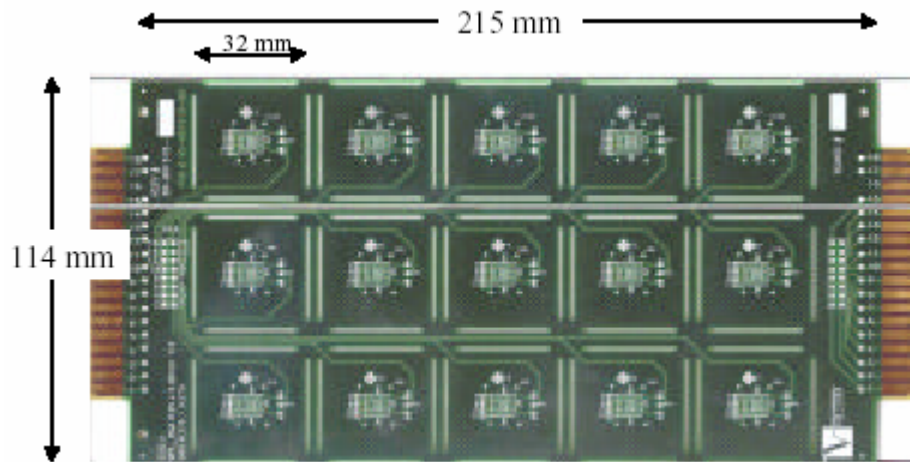


Figure 4 – Test Board Designs

Table 1 – Materials Lists

| Material                      | Parameters                                                                                                                             |
|-------------------------------|----------------------------------------------------------------------------------------------------------------------------------------|
| Solder Paste (Indium SMQ 92J) | Composition = 63%Sn, 37%Pb<br>Metal % = 90.25%<br>Flux = NC-SMQ92J<br>Mesh size = -325 – 500                                           |
| Stencil                       | Thickness = 4 mil<br>Aperture Size = 10 mil Square<br>Laser Cut w/ electro polish                                                      |
| Test Board                    | Thickness = 62 mil<br>Number of layers = 6 layers<br>Nominal Pad Size = 11 mils<br>Pitch = 0.5 mm<br>Surface Finish = Immersion Silver |

### Assembly Process

The assembly process flow is shown in Figure 5. The parameters chosen for the DOE matrix are print speed, print pressure, and snap off speed. The high paste volume and low variance of the paste volume were chosen as the desirability of the DOE study. The optimized DOE parameters were print speed=29 mm/sec, print pressure=10 kg, and snap off speed=1.5 mm/sec.

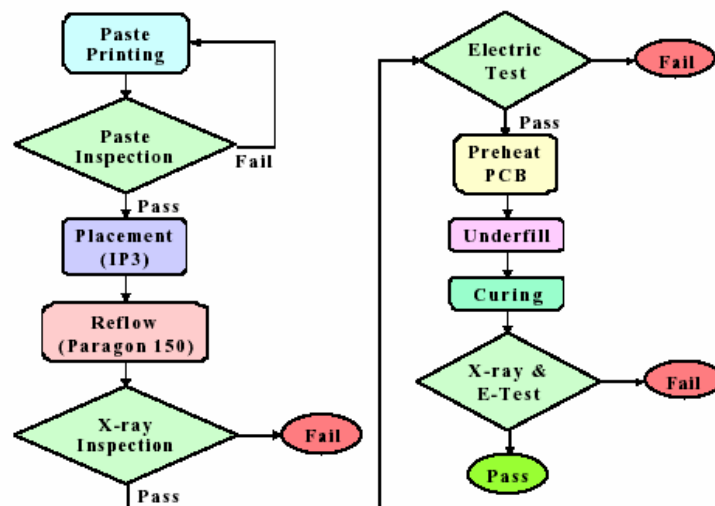


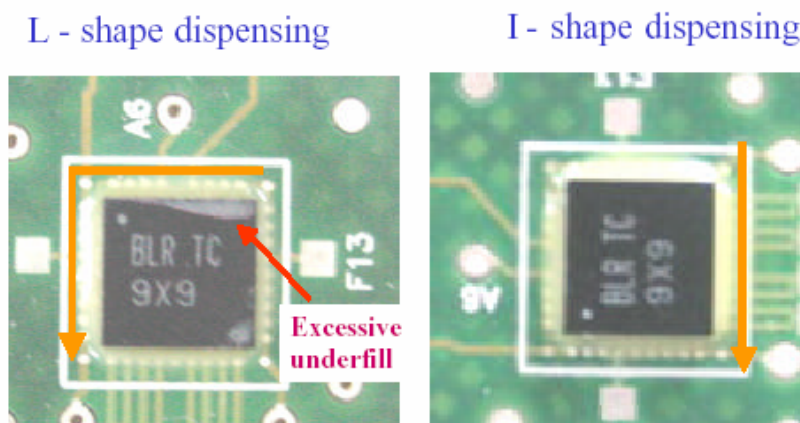
Figure 5 – Assembly Process Flow

The underfill glue can generally be used to improve the reliability of Flip Chip or CSP type components. There are four capillary flow reworkable and two nonreworkable underfill materials evaluated in this study. The material properties and process parameters of all the underfill materials tested are listed in Table 2.

**Table 2 – Properties of the Underfill Materials**

| Properties of Underfill Materials |                  |                  |                   |                   |                   |                   |
|-----------------------------------|------------------|------------------|-------------------|-------------------|-------------------|-------------------|
| Type                              | A                | B                | C                 | D                 | E                 | F                 |
| Vendor                            | Vendor A         | Vendor A         | Vendor A          | Vendor B          | Vendor B          | Vendor C          |
| Model                             | A                | B                | C                 | D                 | E                 | F                 |
| Reworkable                        | No               | No               | No                | No                | Yes               | Yes               |
| specific gravity @25c             | 1.16             | 1.44             | 1.53              | 1.52              | 1.32              | 1.1               |
| CTE (ppm/°C)                      | 60               | 45               | 41                | 35                | 40                | 80.2              |
| T <sub>g</sub> (°C)               | 135 °C           | 115 °C           | 120 °C            | 130 °C            | 70 °C             | 35 °C             |
| Filler Content                    | 0%               | 40%              | 50%               | 40%               | 30%               | 0%                |
| Shelf life                        | 6 months (-5 °C) | 6 months (-5 °C) | 6 months (-40 °C) | 6 months (-40 °C) | 6 months (-40 °C) | 3 months (-20 °C) |
| Pot life (25 °C)                  | 14 days          | 7 days           | 2 days            | 8 hours           | 30 hours          | 4 days            |
| Viscosity (25 °C)                 | 7250 cps         | 5000 cps         | 6000 cps          | 8000 cps          | 300-2000 cps      | 2700 cps          |
| Preheat temp.                     | 90 °C            | 90 °C            | 90 °C             | 100 °C            | 100 °C            | 70 °C -100 °C     |
| Curing Temp                       | 165 °C           | 150 °C           | 150 °C            | 165 °C            | 165 °C            | 165 °C            |
| Curing Time                       | 5 min            | 5 min            | 4-15 min          | 5 min             | 7 min             | 6 min             |

For CSPs, a rule of thumb is to accept underfill fillet height  $\geq 50\%$  of CSP height. In order to select the appropriate machine parameters, it is necessary to know the required volume of the underfill material for WLCSP component. Since the L-shape dispensing pattern may result in excessive underfill material on top of the WLCSP component, the I-shape dispensing pattern is used in this study (see Figure 6).



**Figure 6 – Underfill Dispensing Pattern**

Between the two reworkable underfill materials E and F, F appears to be easier to rework than E. In the study, it is found that the suggested rework process of underfill E material from the vendor may damage the solder mask or PCB pads. A further development of the rework process for WLCSP component is necessary if underfill E is to be used in production.

### Accelerated Thermal Cycle (AT) Tests

During operation, as temperature changes, thermal stress is induced as a result of the mismatch in the Coefficient of Thermal Expansion (CTE) between different materials. For example, the CTE of copper is about 17.7 ppm/ °C, CTE of solder is about 25 ppm/ °C, and CTE of silicon die is about 3 ppm/ °C at 25 °C. This stress will lead to solder joint fatigue in the long-term. Thus, it is very important to understand the actual field application environment and stress test the product under simulated lab environment by subjecting the product to Accelerated Thermal Cycling (ATC).

In this study, our samples are tested with two different ATC test specifications. One according to test condition specified in IPC-9701 and the other in compliance with the internal qualification specification of one of the major OEM companies (see Table 3). The daisy chain connections are continuously monitored by event detector with the resolution of 0.2  $\mu$ sec. When the resistance of the daisy chain net exceeds 1000 ohms, the computer will record the signal from event detector and flag as one failure event. The cycle to failure is defined as the number of tested cycles completed at the time of first verified failure event. Test continues until the percentage of cumulative failure for each group of the components exceeds 63.2%.

**Table 3 – ATC Test Specs**

| Accelerated Thermal Cycle Test       |                                                                                                                                                                                                          |                                                        |
|--------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------|
| Test Condition                       | IPC-9701 Mandated or Preferred Condition                                                                                                                                                                 | Specs Adopted in the Paper                             |
| Test Condition 1                     | 0°C ~100°C (Preferred)                                                                                                                                                                                   | Test Condition 1:<br>0°C (-5/+0 °C) ~ 100°C (+5/-0 °C) |
| Test Condition 2                     | -25°C ~100°C                                                                                                                                                                                             | OEM Spec: -40 (+5/-5 °C) ~ 85°C<br>(+10/-0 °C)         |
| Test Condition 3                     | -40°C ~125°C                                                                                                                                                                                             |                                                        |
| Test Condition 4                     | -55°C ~125°C                                                                                                                                                                                             |                                                        |
| Test Condition 5                     | -55°C ~100°C                                                                                                                                                                                             |                                                        |
| Test Duration                        | Whichever condition occurs first:<br>50% cumulative failure/63.2% cumulative failure (Preferred)<br>OR<br>1000 cycles (Preferred for Test Condition 2,3,4), 6000 cycles (Preferred for Test Condition 1) | More than 63.2% failures or maximum 6000 cycles        |
| Low Temperature Dwell and Tolerance  | 10 minutes, 0°C ~ -10°C (Preferred)<br>0°C ~ - 5°C)                                                                                                                                                      | TC1: 10 minutes, 0°C ~ -5°C;<br>OEM Spec: 15 min       |
| High Temperature Dwell and Tolerance | 10 minutes, 0°C ~ 10°C<br>(Preferred 0°C ~ 5°C)                                                                                                                                                          | TC1: 10 minutes, 0°C ~ 5°C;<br>OEM Spec: 15 min        |
| Temperature Ramp Rate                | $\leq 20^{\circ}\text{C}/\text{minute}$                                                                                                                                                                  | TC1: 10°C/minute;<br>OEM Spec: 15~20 °C/min            |
| Full Production Sample Size          | $\geq 33$ samples (32 test samples and 1 more for cross-section)                                                                                                                                         | See matrix of each tests                               |
| Package/Die Condition                | Daisy-chain                                                                                                                                                                                              | Daisy-chain                                            |

The acceptable product life in the field application is estimated by the modified Coffin-Manson equations<sup>6, 7, 8</sup> as shown below:

$$L_F = AF \times \left( \frac{N_L}{f_F} \right) \quad (1)$$

$$AF = \left( \frac{\Delta T_L}{\Delta T_F} \right)^n \times \left( \frac{f_F}{f_L} \right)^m \times e^{1414 \left( \frac{1}{T_F} - \frac{1}{T_L} \right)} \quad (2)$$

where,

$L_F$  : Life Expectancy at Field (Days)

$AF$  : Acceleration Factor from Lab to Field Operation

$N_L$  : Number of Cycles Tested in Lab (Cycles)

$f_F$  : Frequency of Use (Cycles / Day)

$f_L$  : Frequency of Temp Cycling at Lab (Cycles /

Day)  $\Delta T_F$  : Temperature swing at Field Operation (Kevins)

$\Delta T_L$  : Temperature swing at Lab (Kevins)

$T_F$  : Peak Temperature at Field Operation (Kelvins)

$T_L$  : Peak Temperature at Lab (Kelvins)

$n = 1.9 \sim 2.27$ , general value used in solder thermal fatigue model

$m = (1/3)$ , general value used in solder thermal fatigue model

The number of cycles survived in the lab can be used to project the expected operating life of the component in field application by using equation (1) and (2). Equation of (1) and (2) can be re-written as:

$$N_L = L_F \times f_F \times \left( \frac{\Delta T_F}{\Delta T_L} \right)^n \times \left( \frac{f_L}{f_F} \right)^m \times e^{1414 \left( \frac{1}{T_L} - \frac{1}{T_F} \right)} \quad (3)$$

In order to understand the effect of different ATC test specifications in the lab, the variables to define the field application in equation (3) could be set to a known value. Thus, equation (3) can be further simplified as:

$$N_L \propto (f_L)^m \times \left( \frac{1}{\Delta T_L} \right)^n \times e^{\frac{1414}{T_L}} \quad (4)$$

To compare the number of cycles between 0 °C to 100 °C and –40 °C to 85 °C tests, equation (4) can be written as:

$$\frac{N_{0to100}}{N_{-40to85}} = \left( \frac{f_{0to100}}{f_{-40to85}} \right)^{\frac{1}{3}} \times \left( \frac{125}{100} \right)^{1.9} \times e^{1414 \left( \frac{1}{373} - \frac{1}{398} \right)} \quad (5)$$

In this study,  $f_{0to100} = 36$  (40 min per cycle) and  $f_{-40to85} = 32$  (45 min per cycle) in equation (5). Thus, when  $m = (1/3)$  and  $n = 1.9$ , equation (5) can be simplified as:

$$N_{0to100} \approx 2N_{-40to85} \quad (6)$$

The 0°C to 100 °C ATC test was terminated at 6123 cycles. The -40 °C to 85 °C test was terminated at 2155 cycles for cost reasons. Test results are summarized in Table 4. To compare the Mean Time to Fail (MTTF) data of 0 °C to 100 °C ATC test and -40 °C to 85 °C ATC test for no underfill and underfill F in Table 4,  $N_{0 \text{ to } 100 \text{ °C}} \approx 3N_{-40 \text{ to } 85 \text{ °C}}$  for the case of no underfill and  $N_{0 \text{ to } 100 \text{ °C}} \approx 1.8N_{-40 \text{ to } 85 \text{ °C}}$  for the case of underfill F sample. The results indicate that equation (4) and (5) can describe the correlation between 0 °C to 100 °C and -40 °C to 85 °C ATC tests for the case of WLCSP component with underfill F. However, the equations did not well predict the correlation of two different ATC tests for the case of no underfill. A proper selection of the m and n value in equation (4) is necessary to be studied in the future.

Table 4 – ATC Test Results

| Summary of ATC Test Results |                                    |                          |                                              |                                   |                          |                                              |
|-----------------------------|------------------------------------|--------------------------|----------------------------------------------|-----------------------------------|--------------------------|----------------------------------------------|
|                             | ATC Test Results (-40 °C to 85 °C) |                          |                                              | ATC Test Results (0 °C to 100 °C) |                          |                                              |
| Underfill                   | First Failure Cycle                | Mean Time To Fail Cycles | Number of Samples Survived after 2155 Cycles | First Failure Cycle               | Mean Time To Fail Cycles | Number of Samples Survived after 6123 Cycles |
| No                          | 324                                | 759                      | 0 out of 45                                  | 1266                              | 2294                     | 0 out of 43                                  |
| A                           | 1141                               | N/A                      | 44 out of 45                                 | 1216                              | 3221                     | 15 out of 45                                 |
| B                           | N/A                                | N/A                      | 45 out of 45                                 | 1677                              | 4173                     | 29 out of 45                                 |
| C                           | N/A                                | N/A                      | 45 out of 45                                 | 3854                              | N/A                      | 44 out of 45                                 |
| D                           | N/A                                | N/A                      | 45 out of 45                                 | 4451                              | N/A                      | 44 out of 45                                 |
| E                           | N/A                                | N/A                      | 45 out of 45                                 | 4280                              | 5295                     | 29 out of 45                                 |
| F                           | 482                                | 1324                     | 7 out of 45                                  | 1612                              | 2338                     | 0 out of 43                                  |

It is interesting to know that underfills C and D both show very good survivor rate (44 out of 45 samples) up to 6123 cycles in the 0°C to 100 °C ATC test. Figure 7 shows the Weibull plots of the failed cycles after ATC tests. The WLCSP component applied with underfill F has about 74% reliability improvement compared to the component without underfill under the -40 °C to 85 °C ATC test. However, the underfill F did not show a significant reliability improvement when samples went through the 0°C to 100 °C ATC test.

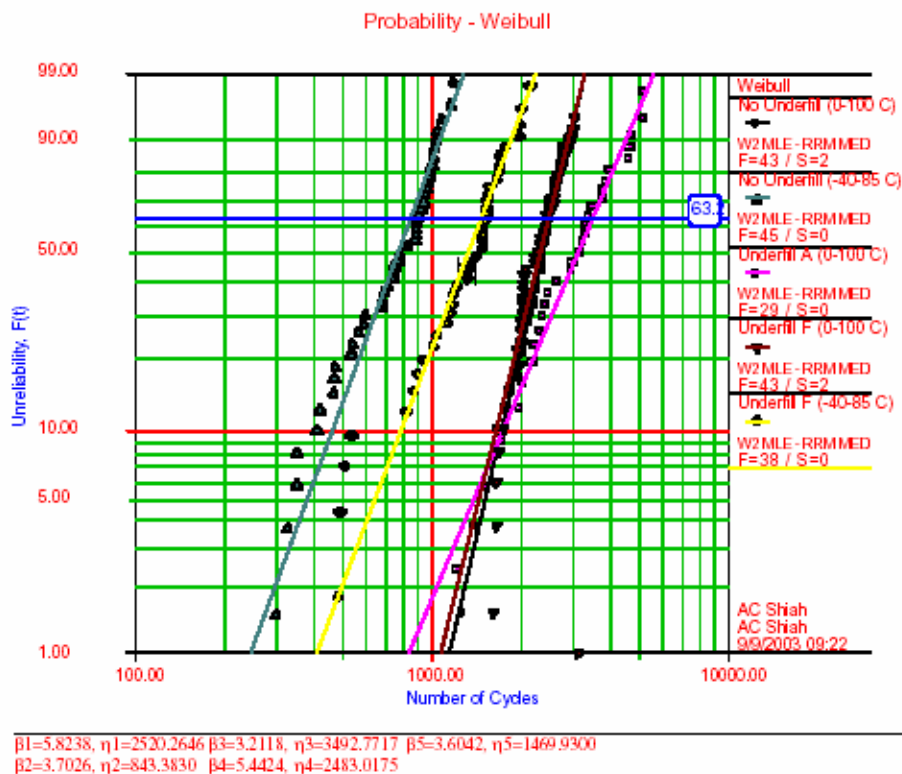


Figure 7 – Weibull Plots of the ATC Test Results



## Mechanical Stress Tests

Instead of ATC test, mechanical stress tests (i.e. shear, shock, and bend tests) can be used to characterize the strength of solder joints under mechanical stress. Shear test can be used to verify if the solder joints can withstand the shear force encountered in processing, handling, or in service conditions. In shear test, the crosshead speed is set as 10 mm/min. Data logger is used to monitor the daisy chain resistance and the sampling rate of the data logger is set as 1000 samples/sec.

Based on the mean shear force data, the reliability performance of WLCSP component with underfill materials are: D (mean=129.6 kgf) > B (mean=128.4 kgf) > A (mean=124.8 kgf) > C (mean=124.4 kgf) > E (mean=121.8 kgf) > F (mean=50.7 kgf) > No underfill (mean=38.1 kgf). There is a 33% increase in maximum shear force when underfill-F is used and more than 200% increase in maximum shear force when other types of underfill materials are used (see Figure 8 and Figure 9).

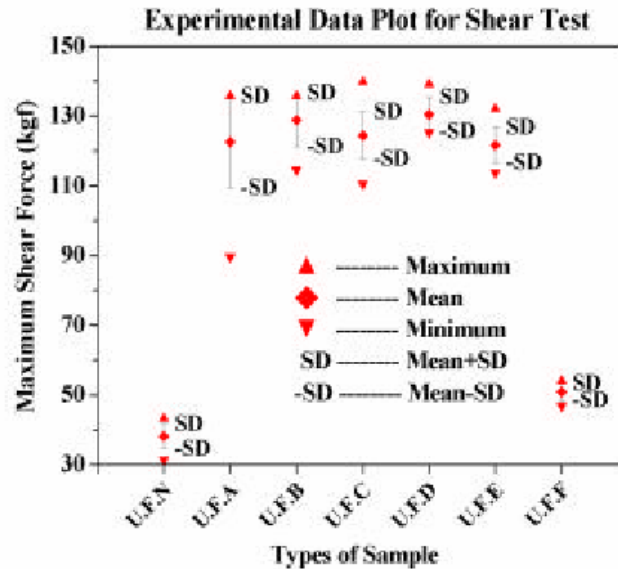


Figure 8 – Shear Test Results

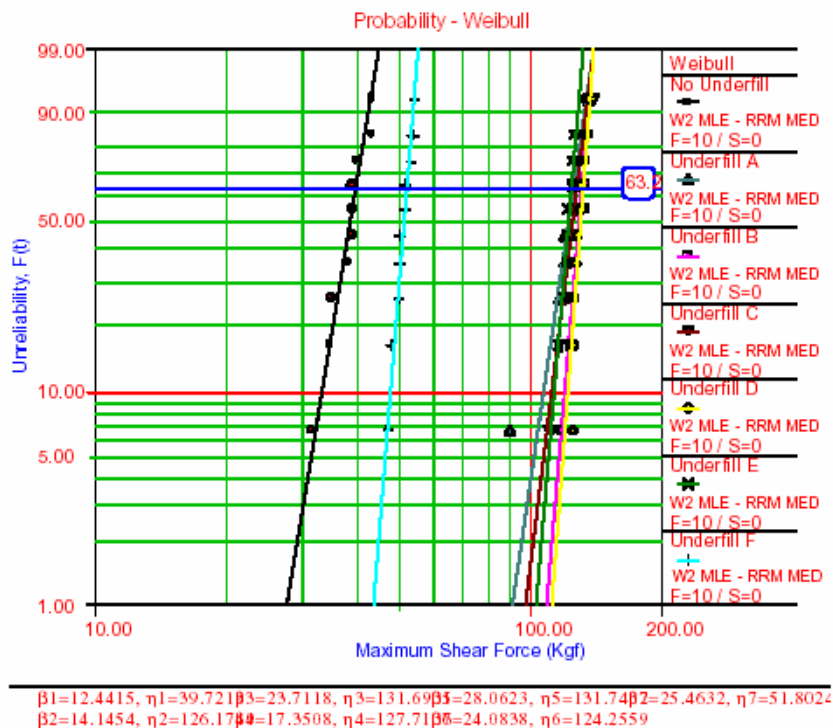


Figure 9 – Weibull Plots of the Shear Test Results



The shock test is set to test the printed circuit boards in positive and negative directions of each of the three directions (vertical, lateral, and longitudinal). Six samples of each combination were tested by shock test. The nominal shock test profile for the WLCSP component is set as a half-sine shock pulse with 30 G (mandatory condition) and 50G (preferred condition) peak acceleration in 5 milliseconds duration. The result shows that all the samples can pass the test without any detected solder joint failure. This indicates that the shock environment may not be an appropriate indicator of solder joint reliability due to the small inertial mass of the WLCSP component.

Bend test is generally used to verify the solder joint strength that can physically withstand the non-repetitive or repetitive bends encountered due to handling, In- Circuit-Test (ICT), transportation, and in service environments. During the pretests with a monotonic fourpoint- bend test, the solder joint is relatively stronger than the PCB which is often damaged before any daisy chain failure occurs. Thus, the bend test used in this study is a three-point bend test for all test components. The bend test condition is to adjust the set-ups so that the strain lies between 500 to 2,500  $\mu$ strain and the strain rate is between 1k to 100k  $\mu$ strain/second. The load cell selected for the test is 10 KN. The load span is 26 mm, the board thickness is 1.6 mm, component width is 4.6 mm, and the diameter of rollers is 2.6 mm, respectively. The test condition of monotonic bend test is to set up the crosshead speed at 5 mm/min. The test conditions for cyclic bend test are a constant velocity of 50 mm/min with a fixed displacement of 0.6 mm.

Due to the limited sample size, only 4 samples of each combination went through monotonic and cyclic bend tests. The monotonic bend test result is shown in Figure 10 and the cyclic bend test result is shown in Figure 12. Figure 11 shows that the resistance during the cyclic bend test starts to fluctuate before the solder joint completely opens.

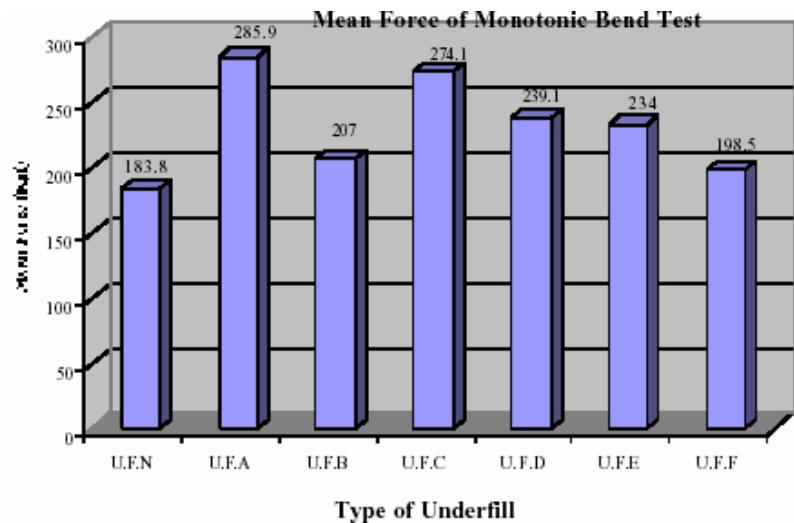


Figure 10 – Mean Force of the Monotonic Bend Test

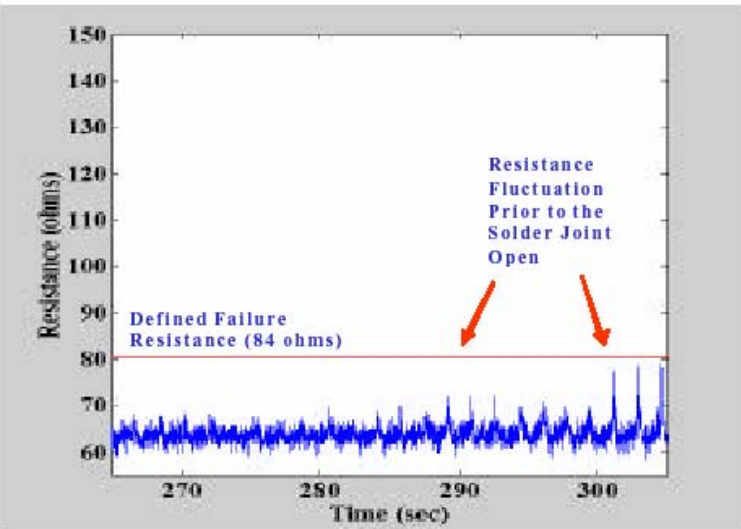
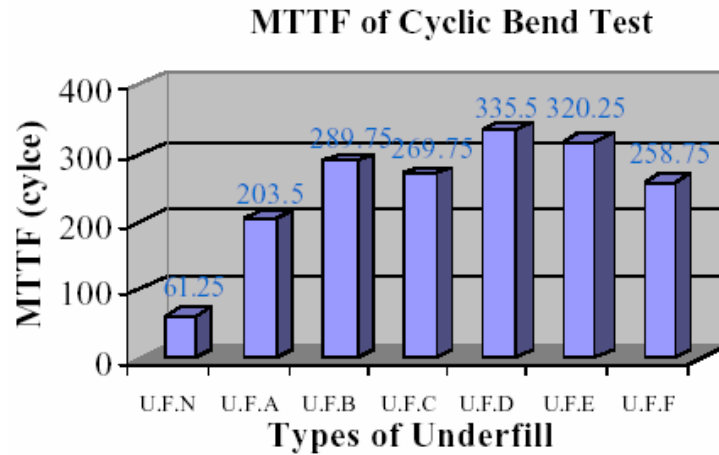


Figure 11 – Resistance Records of a Typical Cyclic Bend Test when Failed

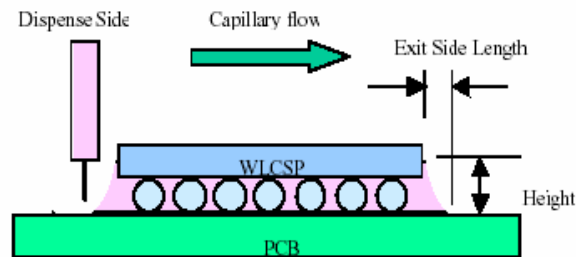


**Figure 12 – Mean Time to Fail Cycles of the Cyclic Bend Test**

#### Failure Analysis

To understand the fillet length and height of the underfill, one cross-sectioned WLCSP sample from each underfill material was measured under microscope (see Figure 13). In general, the dispense side has more underfill than the exit side. However, underfill F has the most evenly distributed underfill on both sides. Figure 14 shows the mean standoff height and diameter of the solder joint is 10.17 mil and 14.96 mil respectively. Figure 15 shows the Under Bump Metallurgical (UBM) thickness is about 1.3  $\mu\text{m}$  ( $\approx 0.05 \mu\text{mil}$ ). From the EDX result, the light area and dark area of the solder joint are Pb rich phase and Sn rich phase individually. It is known that Sn-Cu IMC thickness greater than 5  $\mu\text{m}$  can cause brittleness of the solder joint. In this paper, the IMC layer on PCB side is SnCu rich phase and the thickness is about 2  $\mu\text{m}$ . The Ag finish of the PCB pads is dissolved into the solder joint and cannot be observed in the IMC layer (see Figure 16).

| Underfill Fillet Measurement |                     |        |                 |        |
|------------------------------|---------------------|--------|-----------------|--------|
|                              | Dispense Side (mil) |        | Exit Side (mil) |        |
|                              | Length              | Height | Length          | Height |
| Underfill A                  | 47.4                | 34.7   | 12              | 29.5   |
| Underfill B                  | 49.2                | 32.9   | 11.5            | 24.9   |
| Underfill C                  | 50.2                | 36     | 19.5            | 32     |
| Underfill D                  | 73.9                | 36.7   | 12.7            | 33     |
| Underfill E                  | 48.5                | 33.9   | 13              | 20.2   |
| Underfill F                  | 29                  | 25     | 20.5            | 18.9   |



**Figure 13 – Measurement of Underfill Fillet**

| Solder Joint Measurement |                 |                        |
|--------------------------|-----------------|------------------------|
| Component                | Diameter (mils) | Standoff Height (mils) |
| A10U4                    | 14.75           | 10.19                  |
| A14U11                   | 14.96           | 10.36                  |
| B12U2                    | 14.34           | 10.40                  |
| B14U11                   | 15.04           | 10.07                  |
| C14U11                   | 14.63           | 10.19                  |
| D14U11                   | 14.17           | 10.40                  |
| E11U6                    | 15.25           | 10.03                  |
| E14U11                   | 15.29           | 9.86                   |
| F15U8                    | 16.00           | 10.11                  |
| F16U11                   | 15.13           | 10.11                  |
| Average                  | 14.96           | 10.17                  |
| Variance                 | 0.52            | 0.17                   |

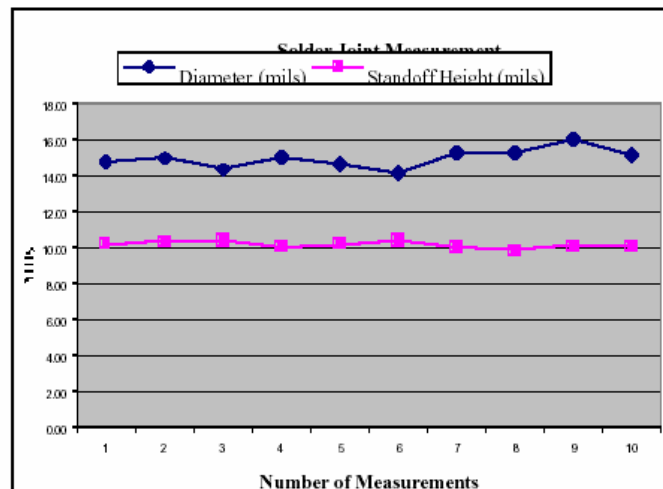
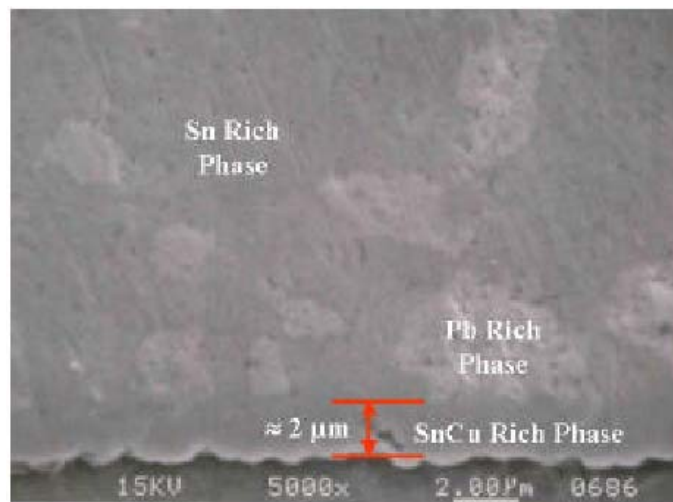


Figure 14 – Measurement of Solder Joint

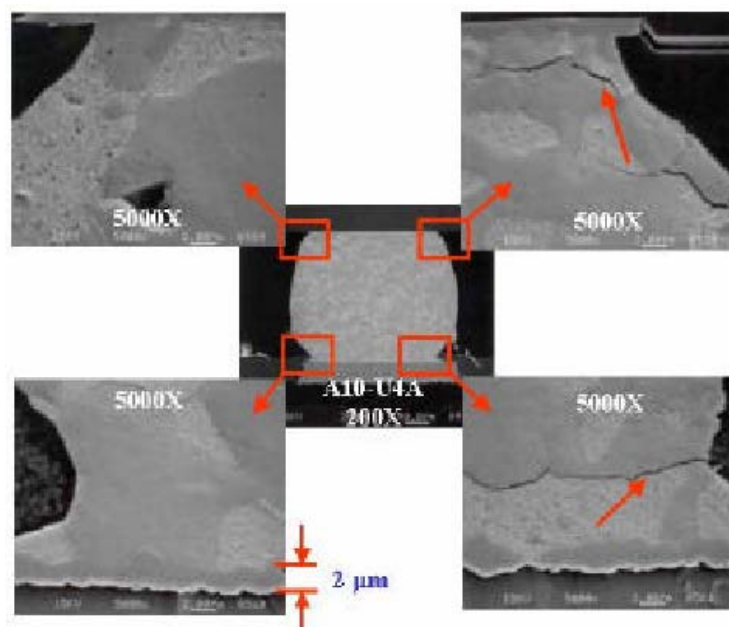


Figure 15 – Under Bump Metal (UBM) Structure (4000 X)



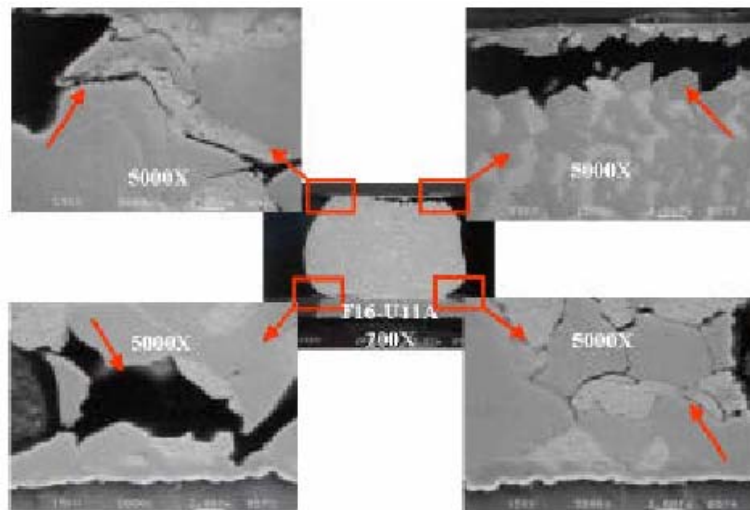
**Figure 16 – Zoom in (5000 X) View of Solder Joint Metallurgical Structure on PCB Side**

Figure 17 and Figure 18 shows typical solder joint fatigue phenomenon after thermal cycle test. The cracks initiate from one side of the solder joint on either component or PCB side and propagate through the granular structure. Since the underfill material prevents the dye from penetrating into the crack area in the solder joint, there is no red dye observed on the PCB after the components were pulled out (see Figure 19 and Figure 20).



**Board A10, U4, 0 to 100 °C, Failed at 1507 Cycles**

**Figure 17 – Board A10, Location U4 (0 to 100 °C ATC Test, Failed at 1507 Cycles)**



Board F16, U11, -40 to 85 °C, Failed at 482 Cycles

Figure 18 – Board F16, Location U11 (-40 to 85 °C ATC Test Failed at 482 Cycles)

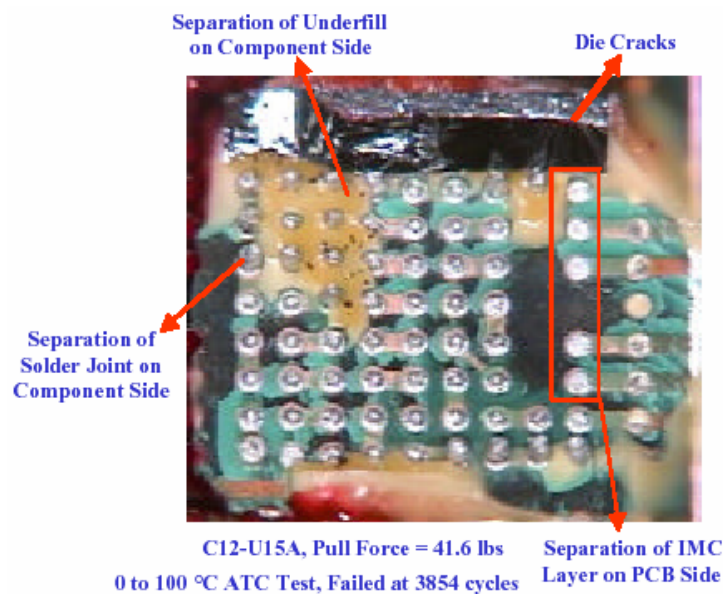


Figure 19 – Dye-pry Test Result for Underfill C Sample

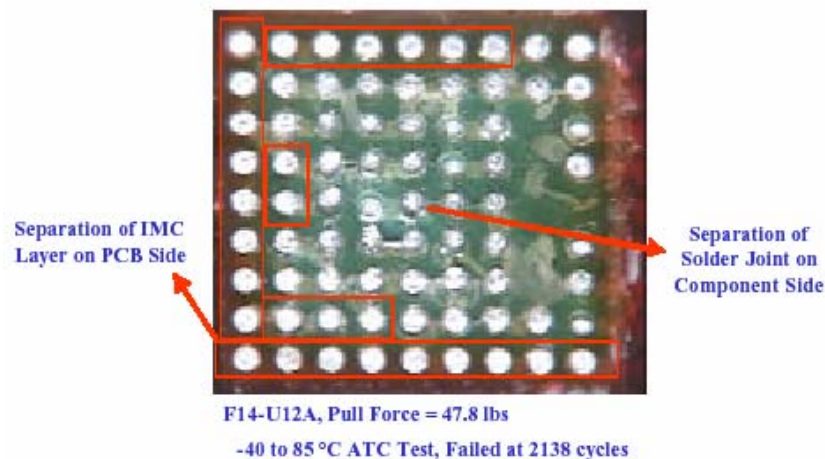


Figure 20 – Dye-pry Test Result for Underfill F Samples

## Summary and Discussion

Table 5 shows the comparison of underfill parameters and Table 6 shows the summary results of the reliability tests. In general, the presence of underfill can significantly improve the board level reliability of WLCSP component. The following is a summary of the results and observation:

- (1) The WLCSP components can pass the shock test (30G in 5 msec, then, 50 G in 5 msec) even without any underfill. This suggests that the component with small inertia mass such as WLCSPs can survive in a high shock environment.
- (2) It is interesting to know that there is a 33% increase of maximum shear force by using underfill-F and more than 200% increase of maximum shear force by using the other type of underfill materials on WLCSP component.
- (3) Since the sample size of monotonic bend and cyclic bend tests are quite small (4 samples per combination), the bend test results can only be used as a reference. The results show that in the case of WLCSP components, the presence of underfill improves reliability. In order to draw a correlation with confidence, a bigger sample size is necessary.
- (4) Based on the 0 to 100 °C and -45 to 85 °C ATC test results, underfills C and D out perform all others. 44 out of 45 underfill C samples survived up to 6123 cycles for the 0 to 100 °C ATC test with one failure occurring at 3854 cycles. 44 out of 45 underfill D samples survived up to 6123 cycles for the 0 to 100 °C ATC test with one failure at 4451 cycles.
- (5) For reworkable underfills underfill E is more reliable than underfill F. However, underfill F is easier to rework than underfill E. An optimized rework process for underfill E material is being developed at the Soletron Technical Center (STC).
- (6) By comparing the parameters of underfill materials, there are some internal correlations between % of filler, viscosity, CTE, and Tg parameters. Among all the underfills tested, C (CTE=41 ppm/ °C), D (CTE=35 ppm/ °C), and E (CTE=40 ppm/ °C) outperform than the others could be due to the low CTE value.

## Conclusion

The presence of underfill definitely improves the board level reliability of WLCSP component. Reworkable underfill with low Tg has a better reworkability, however, the reliability is not as good as the other reworkable underfill material with high Tg. In general, the underfill material with low CTE has a better performance. The choice of underfill material will have to be based on the preference of reworkability over reliability or vice versa. With further optimization of the underfill formulations, this picture can be changed completely.

## Acknowledgements

The authors would like to acknowledge the following individuals to complete this project: Efren Lacap and Subhash Nariani from Volterra, Sunny Zhang, Lodgers Chen, Fowler Chang, and Christina Chen from SLR SuZhou, Xiang Zhou, Teresita Villavert, Charlson Bernal, Terri Zee, Harjinder Ladhar, and Kim Hyland from STC in SLR Corporation.

## References

1. J. H. Lau, *Low Cost Flip Chip Technologies for DCA, WLCSP, and PBGA Assemblies*, McGraw Hill, New York, 1999.
2. J. H. Lau, and R. Lee, *Chip Scale Package, Design, Materials, Process, Reliability, and Applications*, McGraw Hill, New York, 1999.
3. A.C. Shiah and Xiang Zhou, "Board Level Manufacturability and Reliability Assessment of 0.5 mm Wafer Level CSP with Over-Sized Balls", *APEX 2003*, Anaheim, LA, March 29-April 2, 2003.
4. A.C. Shiah, and Xiang Zhou, "Manufacturability and Reliability Assessment of Volterra 0.5 mm Wafer Level CSP Package", *CORSTC-10-100099*, Soletron Corporation, Nov. 2002.
5. IPC, *IPC-9701 Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachment*, IPC, IL.
6. K.C. Norris and A.H. Landzberg, "Reliability of Controlled Collapse Interconnections", *IBM Journal of Research and Development*, May 1969, pp.266- 271.
7. R.C. Blish, "Temperature Cycling and Thermal Shock Failure Rate Modeling", *35th Annual Proceedings of the International Reliability Physics Symposium*, IEEE, 1997, pp. 110-117.
8. Paul Tobias, "Assessing Product Reliability", *Engineering Statistics Handbook*, Chapter 8, NIST/SEMATECH, 2003.