Presented at IPC Printed Circuits Expo®
SMEMA Council APEX®
Designers Summit 04

Qualification of Stacked Microvia Boards for Handset Assembly

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Abstract
The trends of increased functionality and reduced size of portable wireless products, such as handsets and PDAs, are demanding increased routing densities for printed circuit boards. The handheld wireless product market place demands products that are small, thin, low-cost and lightweight and improved user interfaces. In addition, the convergence of handheld wireless phones with palmtop computers and Internet appliances is accelerating the need for functional circuits designed with smallest, low-cost technology.

Historically, the industry has met this challenge through high density interconnect technology and increased silicon integration and component miniaturization. Microvia high density interconnect (HDI) also known as build up technology, is one method for constructing circuit boards with high routing density demands.[1]

For HDI board, vias can be formed using unreinforced dielectric such as Resin Coated Foil (RCF) using processing techniques such as laser drilling or photoimaging. The vias are then metallized using electroless copper / electrolytic plating. The advantage of the HDI construction is the ability to create smaller vias (6 mils) and via pad sizes. This enables higher routing density, lower metal count, reduced board area and increased functionality as compared to conventional boards.

Past board technologies used at Kyocera- Wireless Corporation used single stack of microvias on the outer layers. (Layer 1-2 and Layer 7-8). Current phone technology boards have stacked microvias, Layer 1-2 and layer 2-3. Additionally, these vias are filled with electroplated copper while the single stack vias were plated, but not filled.

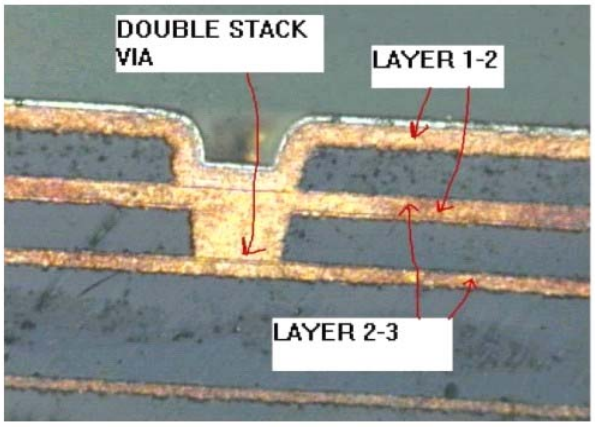
The paper presents the evaluation conducted to ensure the stability of these vias thru the Reflow process. This study was done as a part of a phone product qualification build.

Introduction
Higher density packages and PWB applications requirements are driving the need for high-density interconnect design capabilities using microvias. The benefit of using HDI outer layers is the ability to incorporate high density, high performance area array packages to increase performance of handsets, PDAs etc. Microvias are typically formed on an epoxy resin laminate or dielectric layers on a core substrate and take up configurations such as 2-2-2 or 3-2-3, where the stack up configuration xx-yy-xx means xx layers of build up substrate and yy layers of core substrate.

Stacked microvia technology is emerging in industry, however, and production level reliability data for double-sided surface mount assembly is not readily available. This requires users to establish their own reliability data.

This paper presents the assembly qualification of this technology thru 2 pass reflow and 1 pass rework. Results of solder joint reliability testing, shear test and X-sectional analysis are presented.

PWB Design and Fabrication
The PWB was designed as an 8 layer thin board 0.8 mm thick. The PWB had a combination of single and stacked microvias. The stack–up configuration was 2-4-2, with the outer two layers on top and backside of the PWBs made up of stacked microvia configuration. The microvias (6-mil diameter) were laser drilled and coppers plated and filled. Typical via configuration is shown in Figure 1a and b.



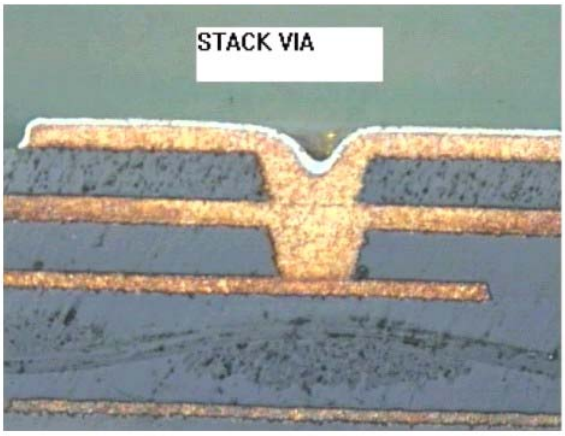


Figure 1 – (a) Double Stack Via **(b) Stacked Via**

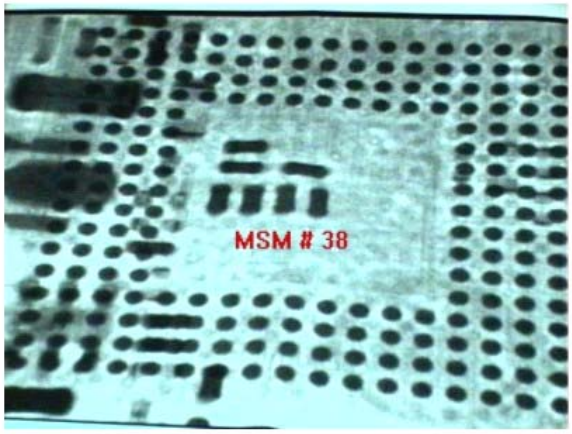
Board Assembly

Board assembly process was a double-sided surface mount assembly soldering of ball grid array packages, connectors, chip resistors, capacitors, and diodes. etc. The assembly was reflowed in convection air at a peak temperature of 219C. The solder paste used for assembly was tin/lead 2% silver (62/36/2)– no clean version.

Post Reflow X-Sections

X-sections were performed on the BGA packages and other components to evaluate the quality of the solder joints and ensure compliance to IPC 610 – Rev C for leaded packages and IPC 7095 for BGA packages. Also microvia integrity was evaluated with X-sectional analysis. X-sections showed acceptable solder joints and no degradation of microvias.[2, 3]

Examples of the X-ray and cross sectional analysis are shown in Figures 2 a and b and 3 a, b, and c.



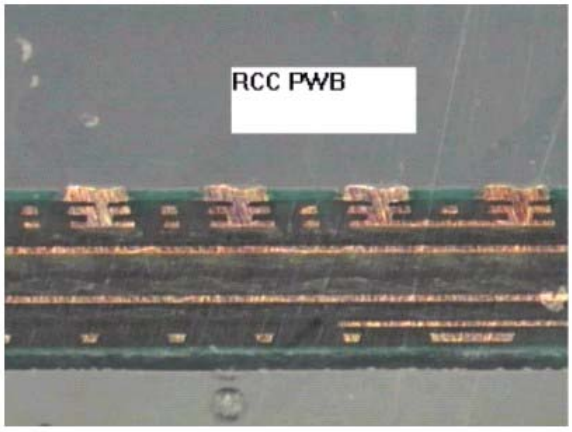
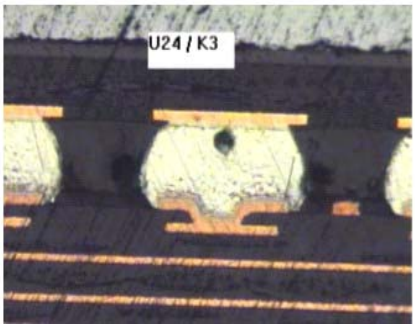
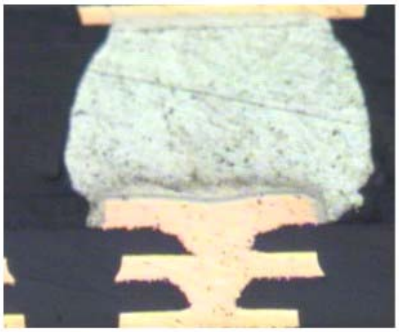


Figure 2 – (a) X- Ray Image BGA **(b) 8 Layer Stack Via PWB**





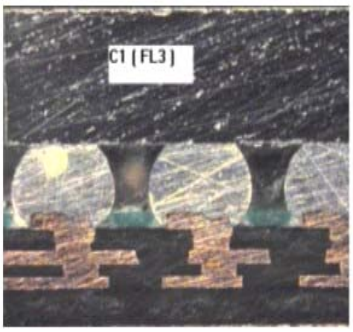


Figure 3 – (a) BGA Joint on Microvia **(b) BGA Joint on Stack Via** **(c) CSP Joint on Stack Via**

Rework Evaluation

Rework of SMT packages is performed using hot air soldering tools and application heat using controlled ramp/soak profile. The concern was damage to microvia connections and PWBs pads during component removal and reattach. Component rework was performed 2X on the leaded packages and 1X on the Ball-Grid Array packages. All packages survived rework. There was no damage to PWB pads, or blistering of solder mask during rework. No damage was seen on microvia connections. A typical rework cross section is shown in Figure 4.

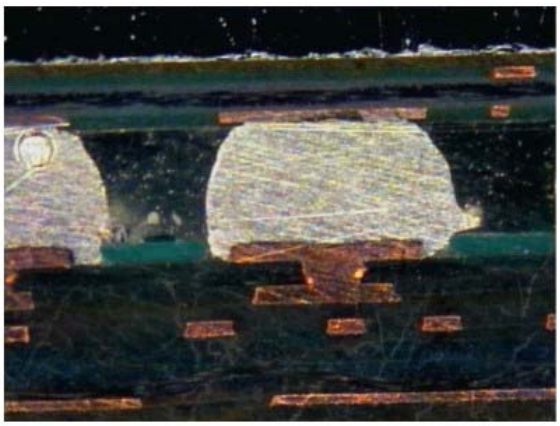


Figure 4 - BGAX-section Post Rework

Shear Testing

Shear testing was performed on SMT packages, post reflow and after thermal shock to evaluate degradation of solder joints as a part of assembly qualification test. Results are shown in Figure 5. Shear values were within the acceptable range.

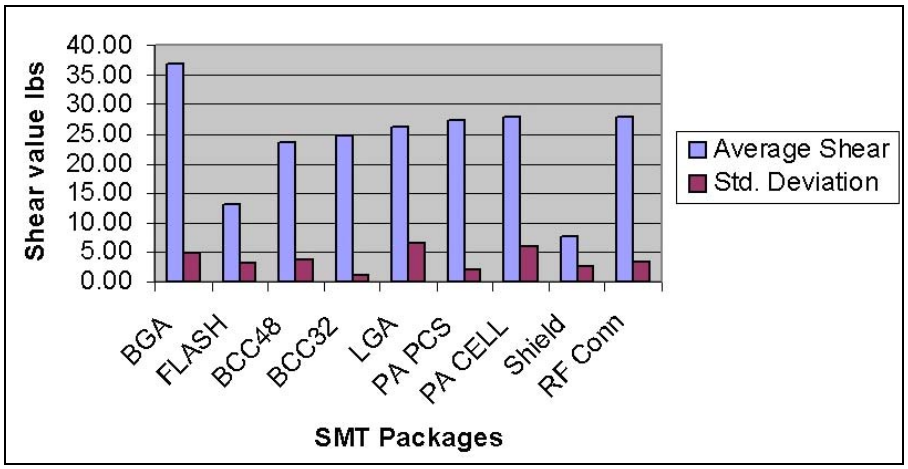


Figure 5 – Shear Test Results-Post Reflow

Solder Joint Reliability Test

Solder joint reliability testing was performed for assembly qualification per IPC SM 785. Assemblies were thermal shock tested from –25C to +125 for 500 cycles.[4] Temperature humidity testing was performed at 85C/85% Relative Humidity for 500 hours. Samples were X-sectioned posttest to evaluate the joint quality. The joints appeared slightly grainy after thermal shock test and oxidized after temp.humidity testing, but no cracks were seen in the joints. Average Shear values post thermal shock was slightly lower than post reflow. A summary of the shear test results is shown in Figure 6a. A typical post thermal shock cross section is shown in Figure 6b.

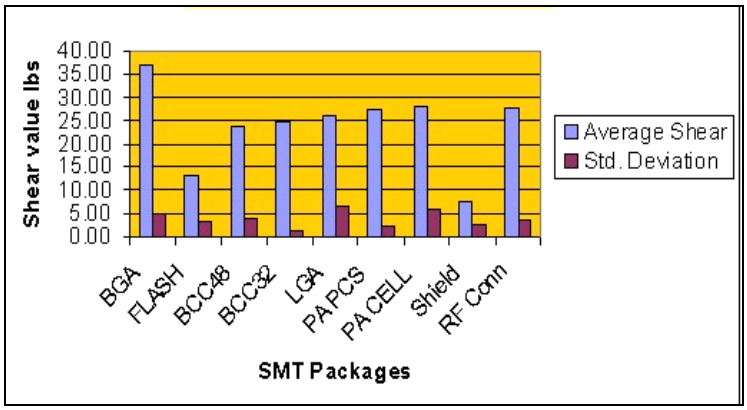
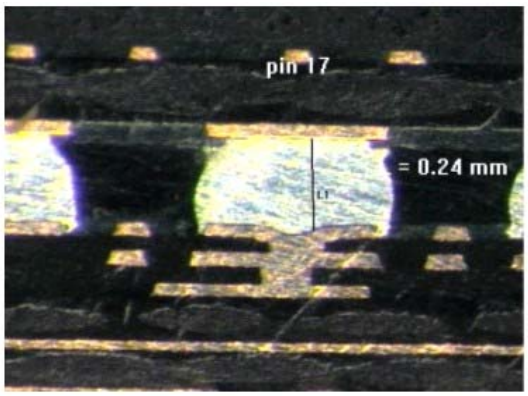


Figure 6a - Sheer Test Results-Thermal Shock



(b) BGA Joint – Post Thermal Shock

Phone Level Drop Test

Phone level drop tests were performed at 1.5 meters on a hard vinyl surface. Assemblies were X-sectioned post drops to evaluate solder joints and microvia connections. No solder joint failures or microvia cracks were seen after drop test.

Conclusion

Stacked microvias PWBs have demonstrated reliability thru 2X reflow and rework operations. The assemblies have survived thermal shock and temp. humidity test and drop shock testing. Since, no failures or cracks were seen in the joints or microvias, the assembly passed qualification testing.

References

1. Microvias for low cost, high density interconnect. John H. Lau, S. W. Ricky Lee.
2. IPC A-610 Rev C – Acceptability of Electronic Assemblies.
3. IPC 7095- Design and Assembly Process Implementation for BGAs.
4. IPC SM 785 – Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments.

Stack Via Assembly Qualification

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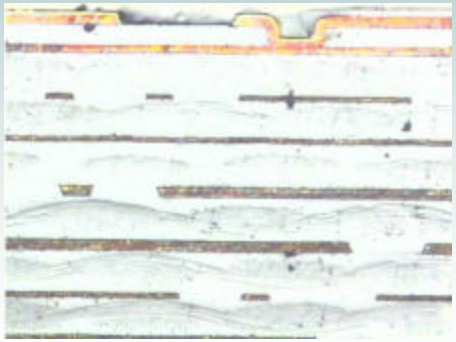
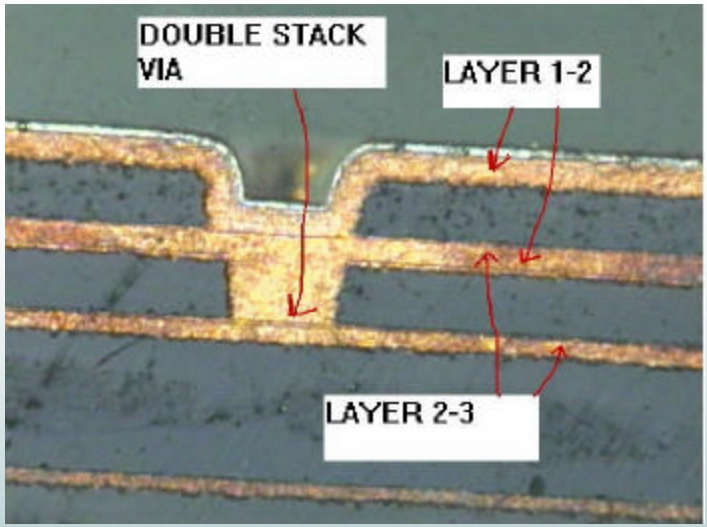
SMT Process Quality
KWC - San Diego

Stack Via Technology Overview

- Handheld Wireless Market
- Advantages
  - > Higher Routing Density
  - > Reduced Board area
  - > Increased functionality
  - > Isolation of ground in RF Boards
  - > Allows 4-6 mils vias - single
  - > Upto 3 mil vias - stacked
- Disadvantages
  - > Fabrication Yields
  - > BGA Solder Joint Voids
  - > Use of Unreinforced Dielectric
  - > Dimensional Stability

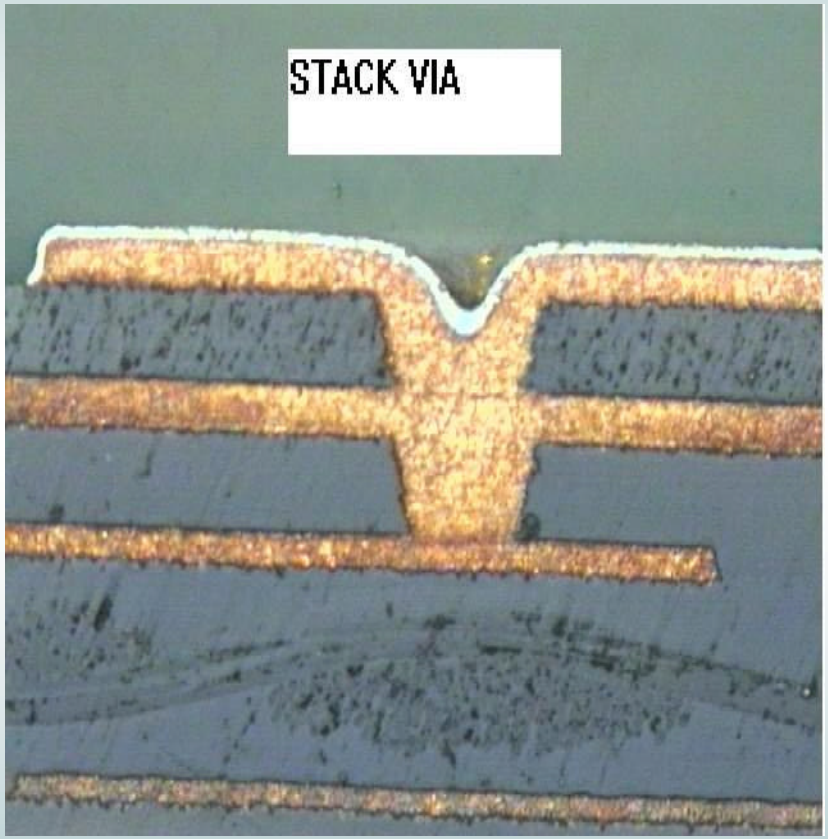


Single Via



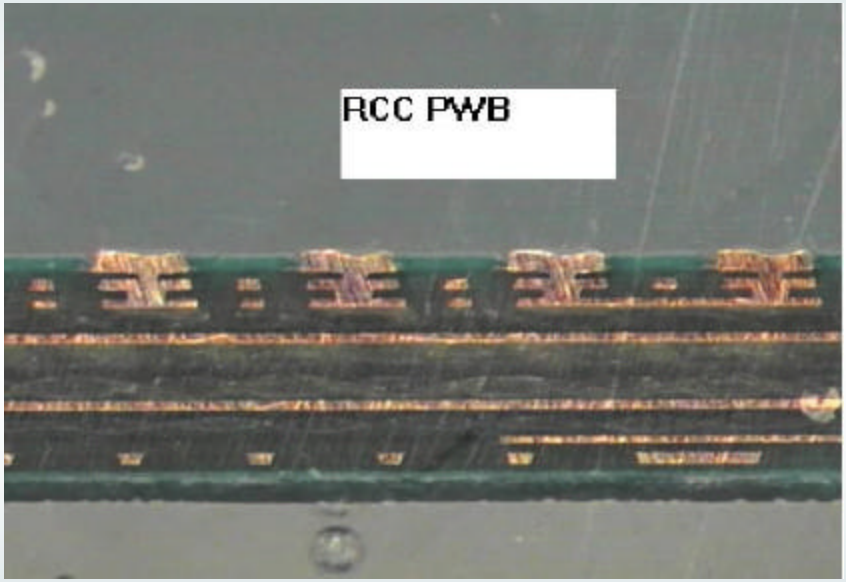
Board Cross Section

- Stack Microvias
- Laser Drilled 6 mil Vias
- Layer 1-2
- Layer 2-3
- Unreinforced Dielectric
- Copper Plated
- 8 Layer PWB
- 0.8 mm Thick
- 3.5” X1.5 “ PWB



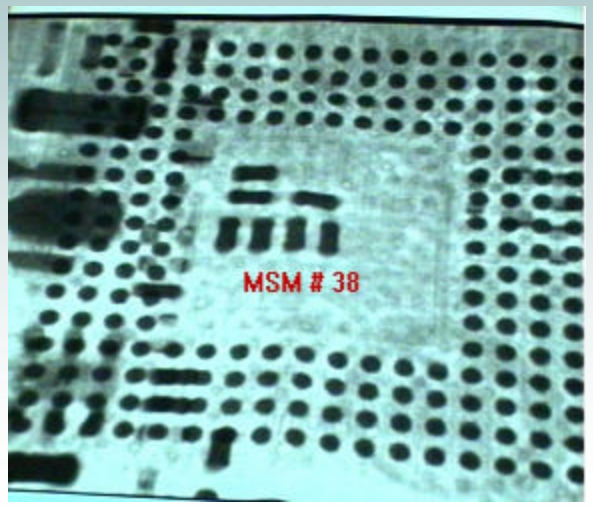
Test Board X-Section

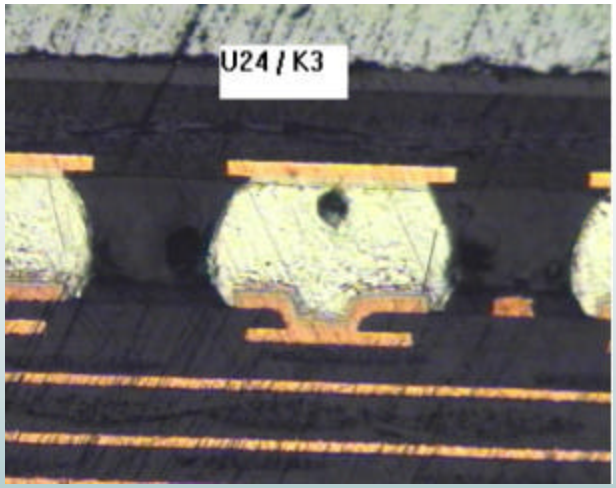
- Single and Stack Microvia
- Copper Filled
- Layer 1-2 Microvias 6 mils
- Layer 7-8 Microvias 6 mils
- 0.8 mm Thick PWB
- Double Sided SMT Assembly



Assembly Challenges

- Thin PWB
- Warpage During Reflow
- Flex in Phone Assembly
- BGA Solderability
- 0.5 mm Package Solderability
- Lead Free Package
- Component Rework
- Microvia Integrity
- Solder Joint Reliability



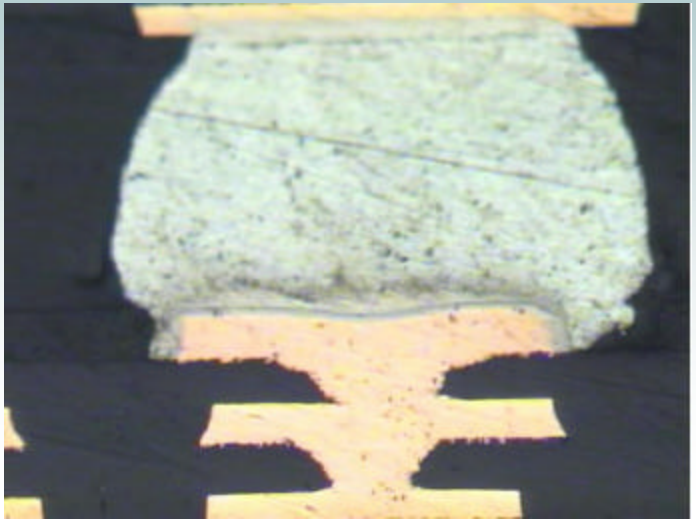


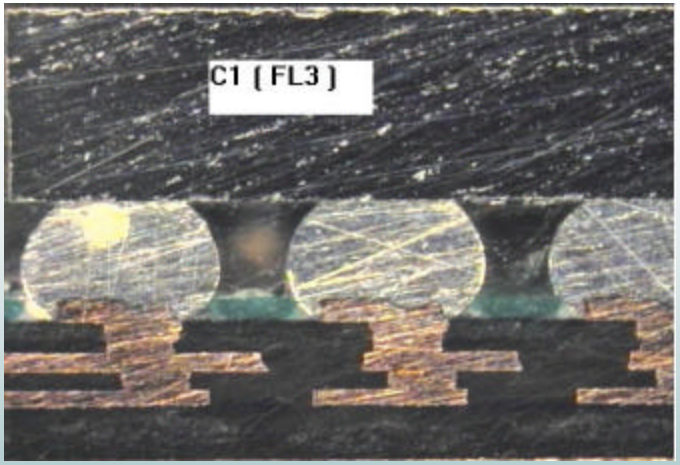
Post Reflow X-Sections

- Solder Joint Profiles
- Voids in BGA Joints
- Microvia Interface Cracks

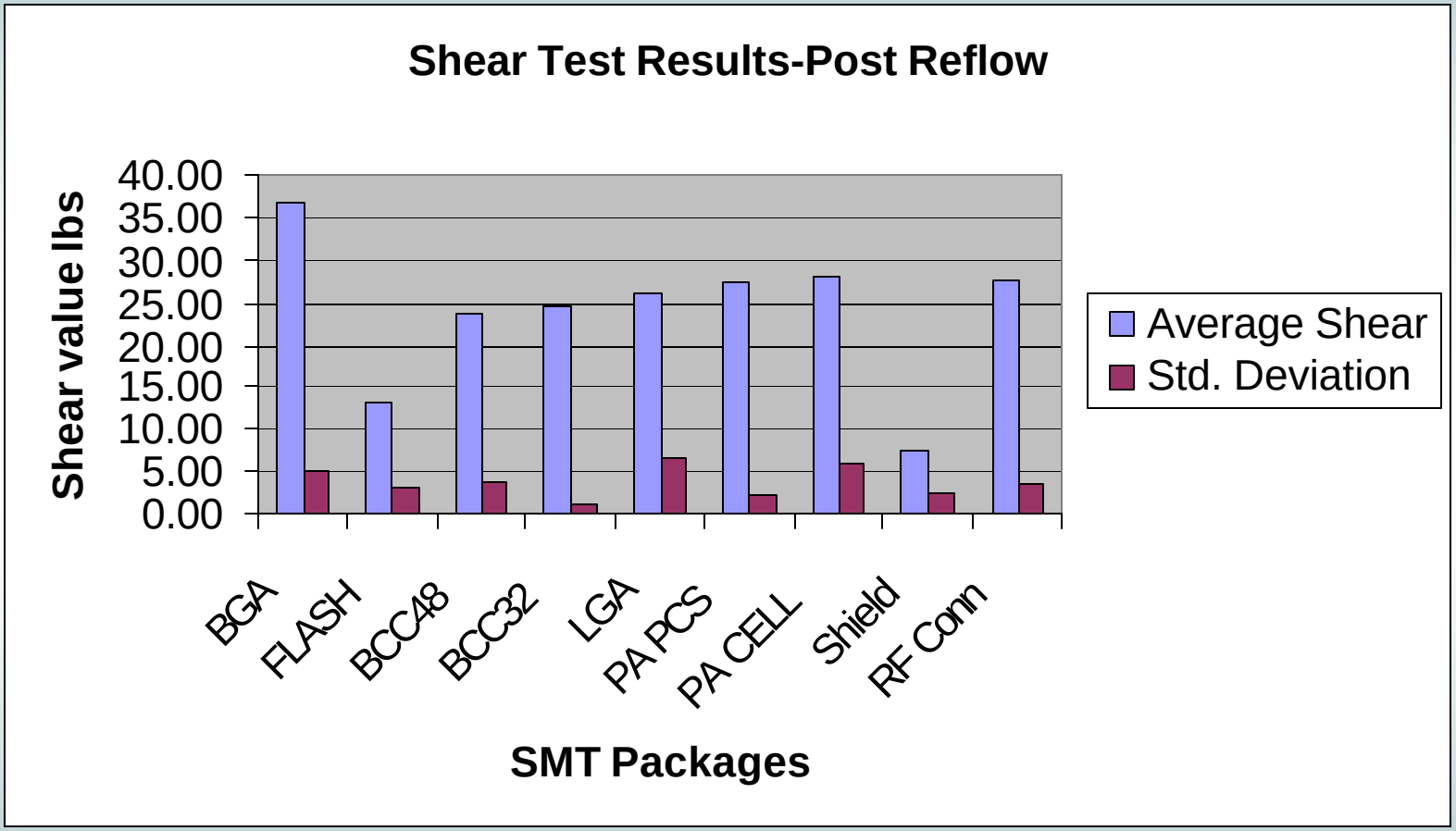
- **Results**

- Acceptable Solder Joints
- Microvia Connections Intact
- Board Warpage on Side 2 Reflow
- Altered Fixturing for warpage



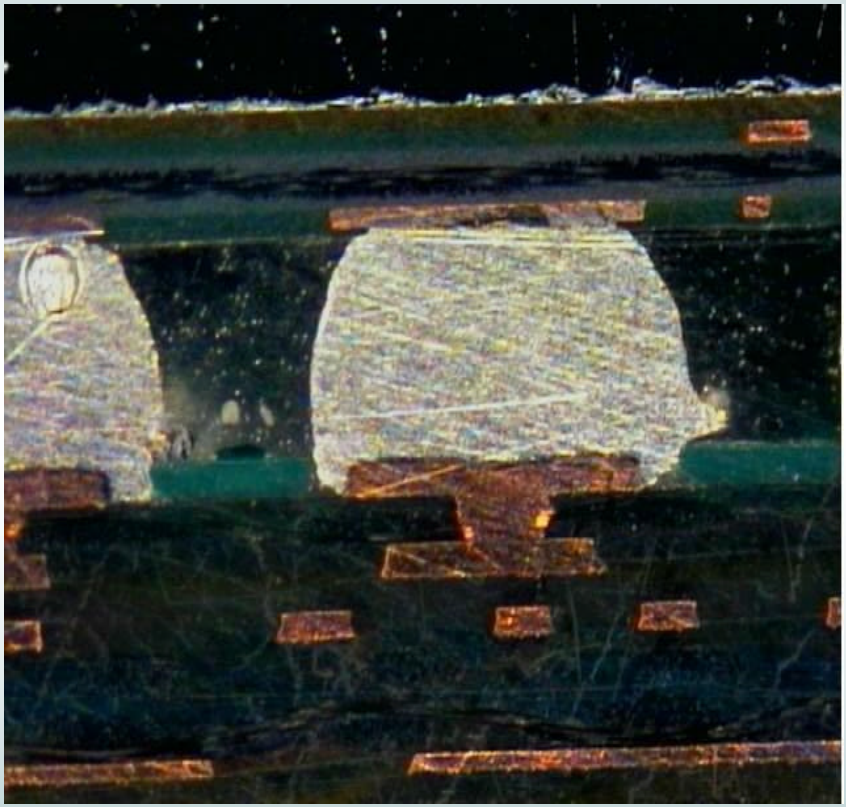


Post Reflow- Shear Test

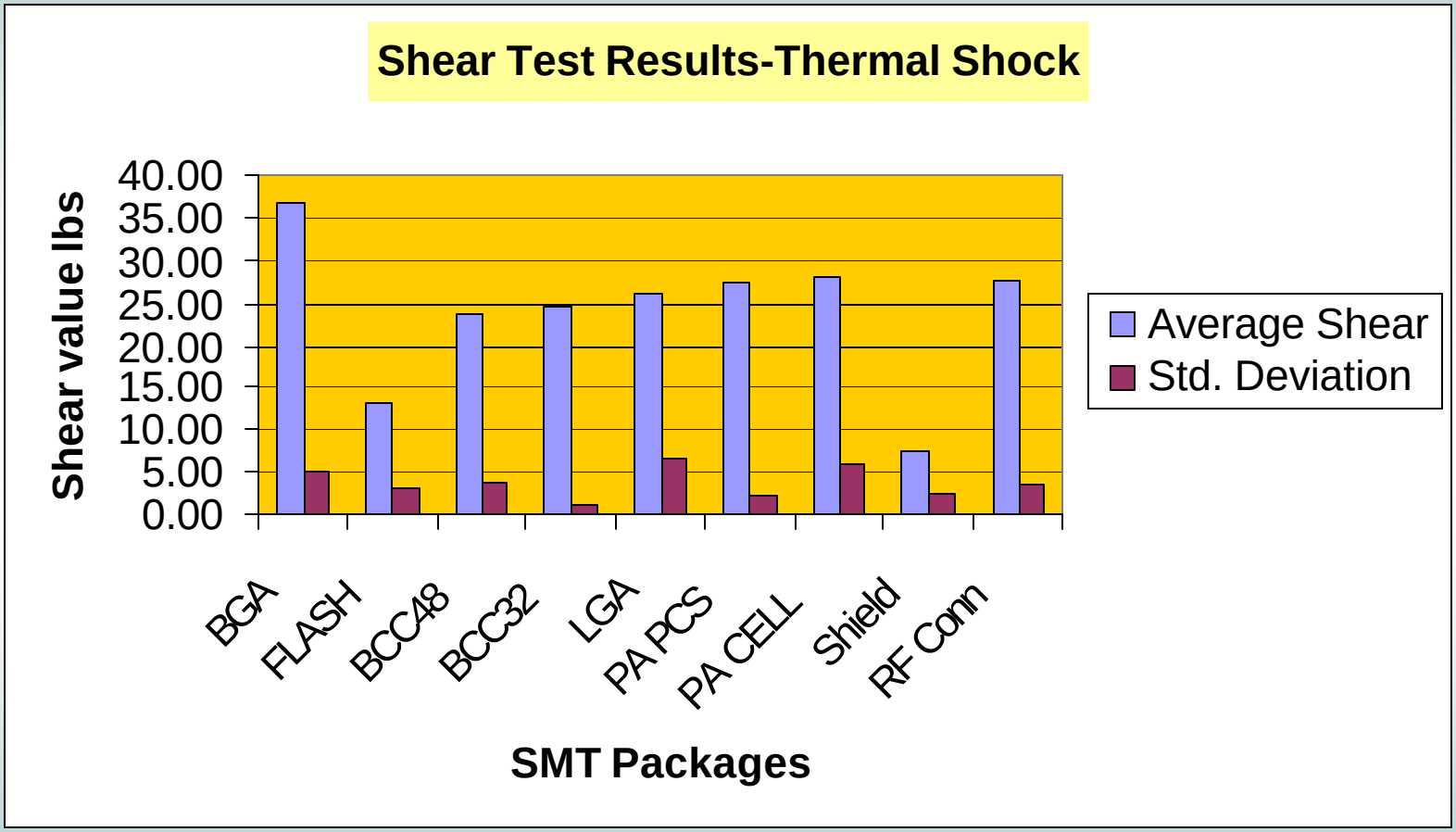


SMT Package Rework Evaluation

- Hot Air Rework
- 2X - SMT Packages
- 1X- BGA Packages
- **Concerns:**
  - > Damaged/Lifted PWB Pads
  - > Board Warpage
  - > Joint Cracking
- **Results:**
  - > Acceptable Rework
  - > No Damage to Lands
  - > No Blistering of PWB
  - > Microvias Intact after 2X Rework

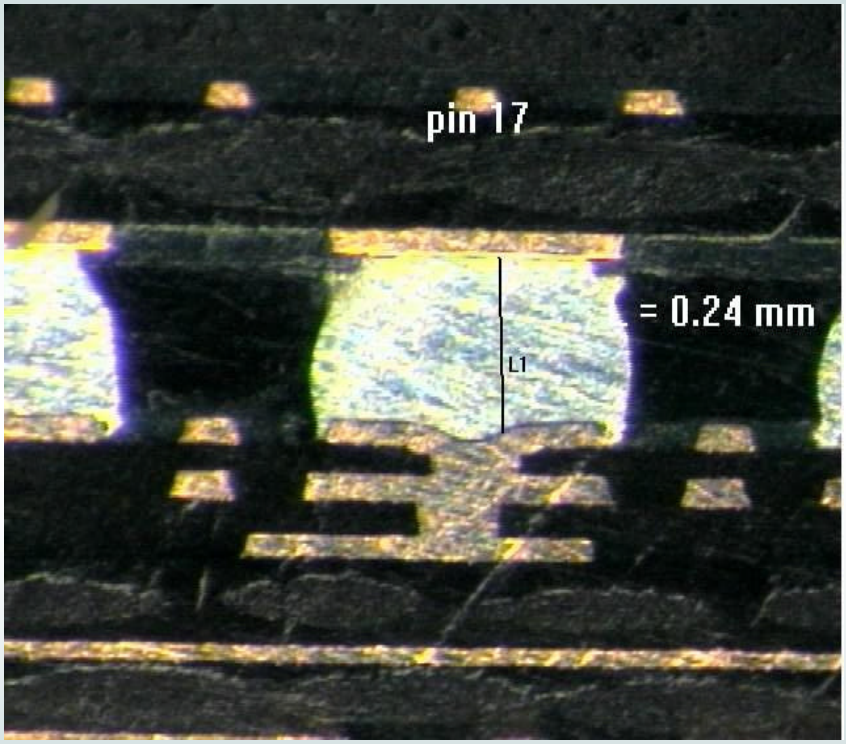


Shear Test - Post Thermal Shock



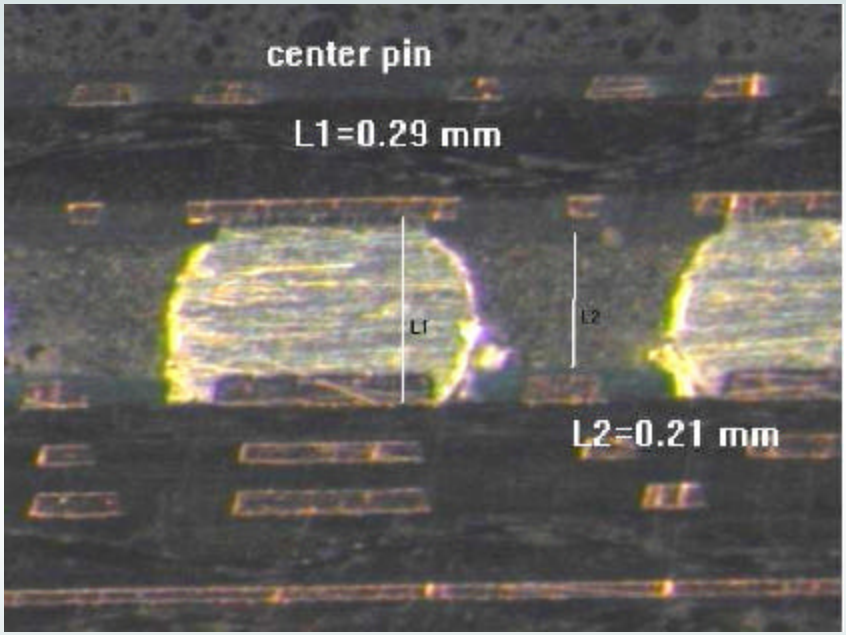
X-Sections Post Thermal Shock

- **Thermal Shock Test**
  - >-25C to +125C - 500 Hours
  - >Evaluate Solder Joint Integrity
  - >SMT and BGA Packages
  - >Joints appear Dull /Grainy
  - >Microvia Connections Intact
  - >BGA Standoff Height - Acceptable
  - >No Cracks/Separation



X- Section - Post Drop

- Phone Level Drop Test
  - > Evaluate electrical /mechanical Integrity
  - > Solder Joint Reliability
- Results
  - > No cracks on SMT Packages
  - > BGA Joints Intact
  - > No open Microvias
  - > No Microvia Interface Cracks



Conclusion

- Stack Microvias PWBs have demonstrated reliability thru:
  - >2X Reflow and Rework
  - >Thermal Shock and Temp. Humidity Test
  - >Drop Shock Test
  - >Reduced BGA Voids with filled Vias
- Recommended for use in Handset Assemblies
- Field Reliability should be tracked for SMT Packages .