Presented at IPC Printed Circuits Expo®
SMEMA Council APEX®
Designers Summit 04

Design of Experiment in Micro-Via Thermal Fatigue Test

T. E. Wong, H. S. Fenger and I. C. Chen
Raytheon Company
El Segundo, CA

Abstract
The objectives of the present study are to design, fabricate, and test various configurations of micro-vias over military thermal environment, and then evaluate the impacts of micro-via design/manufacturing process variables on the thermal fatigue damage of the micro-vias. The selected parameters are solder mask on printed wiring board, micro-via pitch, and micro-via size, with each having either two or four levels of variation. A test vehicle (TV), into which the daisy-chained micro-vias combined with all these selected parameters are incorporated, is first designed and fabricated, and then subjected to temperature cycling from -55ºC to 125ºC with continuous monitoring of micro-via integrity. A total of 26 TVs are used in the present study and the micro-via failure is defined as an electrical discontinuity.

Based on monitored results, a destructive physical analysis (DPA) is conducted to further isolate the failure locations and determine the failure mechanisms of the micro-vias. Test and DPA results indicate that: 1) the smaller the micro-via sizes, the higher the occurrence of manufacturing defects; 2) the micro-vias, having electrical continuities before the test, can survive 1000 temperature cycles; and 3) there is no influence or inclusive observation of the micro-via pitch variation on the micro-via fatigue damage. In addition, a thermo-mechanical analysis with nonlinear finite element computer code applied in a 100 µm (or 0.004 in.) diameter micro-via is performed to illustrate this micro-via integrity when subjected to thermal cycling. Further evaluation of the impacts of the micro-via pitch and diameter variations on the micro-via thermal fatigue damage by finite element analysis is recommended.

Introduction
The emergence of ball grid array (BGA) type package technology is dominating the electronics hardware industry today. The general trend of this technology is using either very large size of BGA with over a thousand balls or smaller BGA type packages, such as a wafer-level chip scale package (WL-CSP) (Lau et al., 2002), which has a redistribution layer to reallocate the very fine-pitch peripheral-arrayed pads on the silicon chip to relatively large-pitch area-arrayed pads with taller solder balls. For WL-CSP, since a significant coefficient of thermal expansion (CTE) occurs between the package and the substrate, e.g. printed wiring board (PWB) or flex, selecting the adequate package size is desirable, which could be achieved by choosing a smaller ball pitch in the package. In other words, a fine pitch of solder pad on the substrate is desirable. A plated-through-hole (PTH) technique is popularly used to connect the top layer of the substrate to the ground plane or other signal layers. However, due to the aspect ratio requirement of the PTH, which is the substrate thickness divided by the hole size and needs to be larger than a certain value, e.g., 6, for minimizing the fracture occurrence of the PTH barrier (mainly caused by CTE mismatches between copper barrier and PWB material) during temperature cycling, the pitch of the substrate's solder pads could not unlimitedly decrease to match with that of WL-CSP. One of solutions to achieve a fine pitch of the substrate's solder pad is to use a micro-via, in which the plated-hole is only through the top layer of the substrate. Figure 1 is the micro-section of the micro-via in the FR4 PWB. However, a concern of the micro-via barrier cracking, which is similar as PTH barrier fracture, is also raised during temperature cycling. This failure mode was also presented in Ramakrishna et al. (2002a/b).

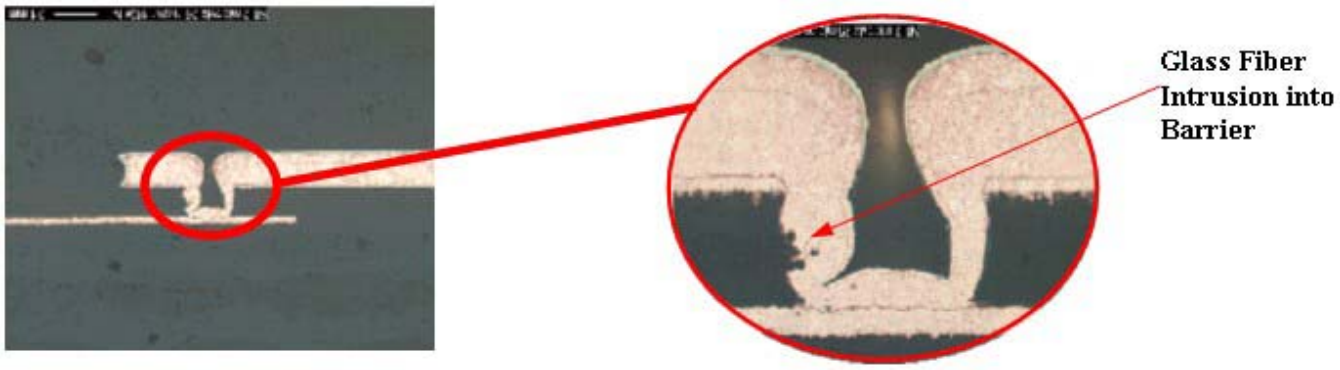


Figure 1 - Micro-section of 100 µm (or 0.004") Micro-via

The objectives of the present study are to design, fabricate, and test various configurations of micro-vias over military thermal environment, and then evaluate the impacts of micro-via design/manufacturing process variables on the thermal fatigue damage of the micro-vias. The approach is to demonstrate the micro-via reliability performance through the design of an electrical daisy-chained patterned PWB test vehicle (TV), in which the design and manufacturing parameters of the micro-via, each having either two or four levels of variation, are included. These parameters are solder mask on PWB, micro-via pitch, and micro-via size. A total of 26 TVs are constructed and subjected to temperature cycling (-55°C to +125°C) with continuous monitoring of the micro-via integrity. Based on monitored results, a destructive physical analysis (DPA) is conducted to further isolate the failure locations and determine the failure mechanisms of the micro-vias. In addition, a nonlinear thermo-mechanical analysis with a finite element computer code is performed to further evaluate the micro-via integrity when subjected to thermal cycling. Note that the micro-via failure is defined as an electrical discontinuity.

Some understanding of the micro-via thermal fatigue damage can be obtained from Hegde et al. (2002), Lau and Lee (2001), Paulus and Petti (1997), Ramakrishna et al. (2002a/b), and Rasul et al. (1997).

Test Vehicle

The TV or Line Replaceable Module (LRM), shown in Figure 2, consists of two single-sided circuit card assemblies (CCAs) and one aluminum heat sink. Each CCA is bonded on one side of the aluminum heat sink with an extremely compliant adhesive, whose elastic modulus is only 0.96 MPa (or 140 psi). This LRM, configured in this manner, is to simulate the most popular design needed for near-term programs. The design parameters (shown in Table 1), each with either two or four levels of variation, are: four different diameters in micro-via (each with a different micro-via pitch) and two solder mask types (including no solder mask).

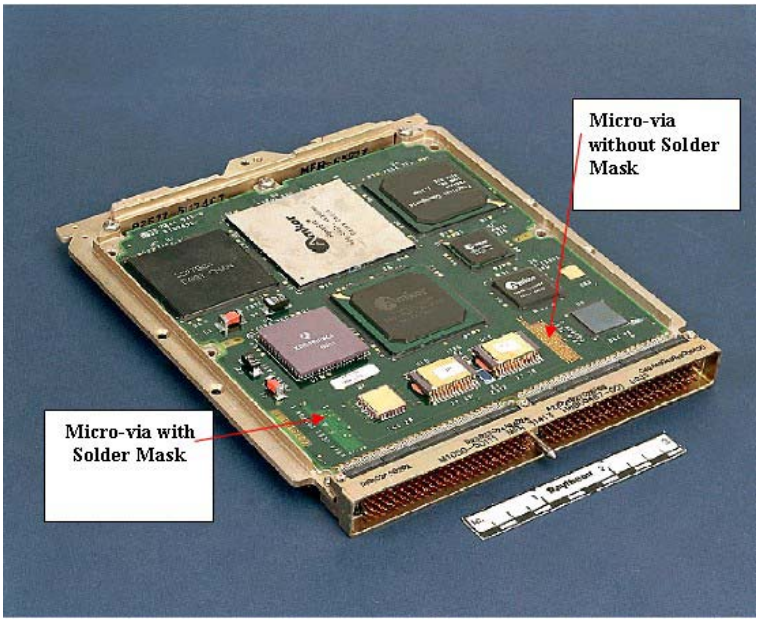


Figure 2 - TV Configuration

Table 1 - Design/Manufacturing Process Parameters & Their Variation Levels

Para-meter	Description	Level			
		1	2	3	4
A	Micro-via Diameter / Pitch (in.)	0.004/ 0.05	0.003/ 0.035	0.002/ 0.02	0.001/ 0.01
B	Solder Mask	No	Yes	-	-

The micro-via PWB interconnects are through a single redistribution layer (RDL). One group of micro-vias has solder mask and the other group has no solder mask. Figure 2 shows the locations of these two groups of micro-vias. The design of the daisy-chain nets in the PWB permitted continuity of select micro-vias. Only one net, shown in Figure 3, is used for each CCA. All daisy-chain nets terminated in a standard pinned connector, precisely identifying continuity to individual and "ganged" nets. High Tg FR-4 PWB is selected. The FR-4 epoxy resin selected is considered to be a preferred mainstream high temperature PWB material standard. Copper trace routing is laid out paying close attention to balance internal metal

mass. This is deemed an important variable in precluding thermal differential expansion/contraction within the composite structure.

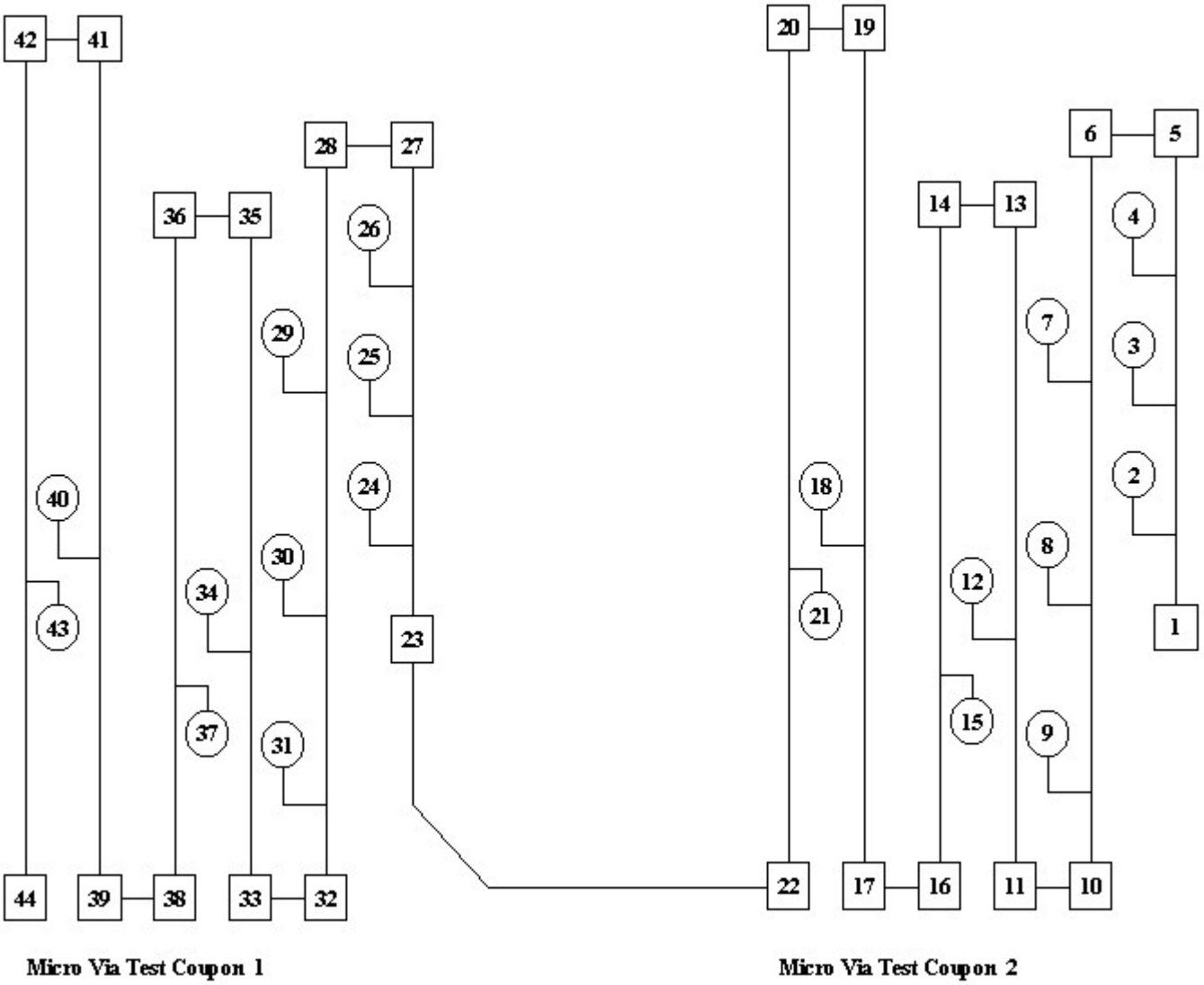


Figure 3 - Micro-via (1 Net)

Note that various types of BGAs are also mounted onto this TV, whose test results cab be found in Wong et al. (2002, 2003) and Fenger and Wong (2003), and will be not discussed in the present study.

Experiment

Test CCAs are mounted to both sides of aluminum heatsinks to replicate actual CTE mismatches experienced at the line replaceable unit levels. A grilled rack is designed to support multiple LRMs and thus replicate slotted style enclosures. This tooling design provides for uniform heating and cooling, minimizing thermal gradients. Six thermocouples per module are used to verify that thermal gradients are acceptable.

During thermal cycling testing, thermocouples are bonded to three different modules, one located at either end of the chamber and one located in the middle. The thirteen modules are installed in the thermal chamber as shown in Figure 4, and the chamber is thermally tuned so that the thermocouples mounted on the modules track the desired thermal profile. This profile consists of alternating high and low thermal extremes with a 20-minute dwell at hot, a 10-minute dwell at cold, and ramp rates of 5.5+/-1°C/minute going hot and 10+/-1°C/minute going cold. All device interconnections are monitored for electrical continuity. Four Anatech Event Detectors are used via a wire harness, through the chamber access port. With a resistance threshold of 500 ohms, a spike duration of 0.2 microseconds for fifteen consecutive evidences constitutes a failure. Temperature cycling is halted, and visual inspection of devices and interconnects is performed at 327, 701, and 1000 cycles. All TVs are exposed up to 1000 cycles.

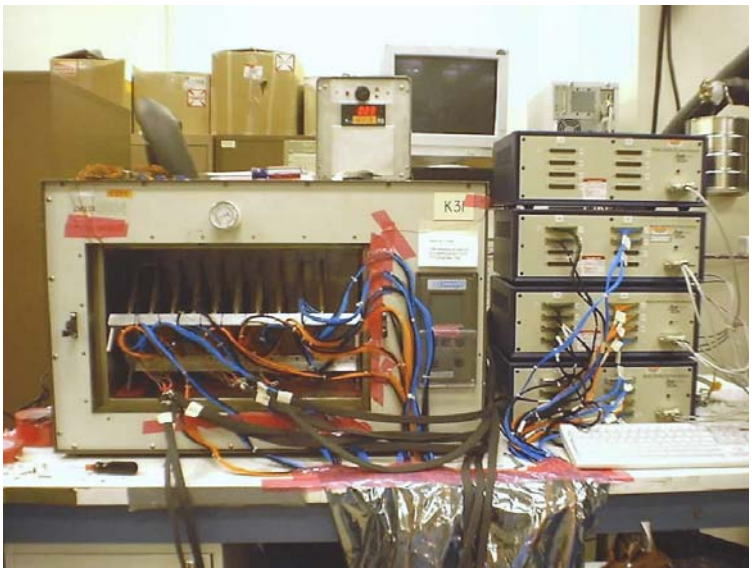


Figure 4 - Test Set-up

Prior to the thermal cycling test, measurements from Anatech Event Detectors show opens in many TVs. Hand probes are then used for each size of micro-vias, and show that electrical contact exists in 50 µm, 75 µm and 100 µm micro-vias and the same is not true for 25 µm micro-vias, which result in the electrical opens measured by Anatech Event Detectors. After the completion of 1000 thermal cycles, no additional electrical open is measured by Anatech Event Detectors. The hand probes are also followed and no additional electrical failure is observed.

Failure Analysis

Visual inspection of the micro-vias is limited since the micro-vias are embedded inside of PWB. Therefore, a DPA is required to further isolate the failure locations and determine the failure mechanisms of the solder joints. Typically, the micro-vias that show electrical opens are selected for sectioning. The micro-via fields are first cut out from the boards and then encapsulated in clear epoxy. In general, the sections are taken first through the outermost row of micro-vias that are indicated as having electrical opens by the measurements from the Anatech Event Detector. If no physical evidence of the opens is found in the first level of sectioning, then additional sectional levels are taken. Evidence of opens is taken to be cracking that completely traverses the micro-via.

Figures 1 and 5 through 7 are micro-sections of the micro-vias corresponding to the diameters of 100 µm (or 0.004”), 75 µm (or 0.003”), 50 µm (or 0.002”), and 25 µm (or 0.001”), respectively. These figures show glass fiber intrusion into the copper barrier. However, electrical contact exists in 50 µm, 75 µm and 100 µm micro-vias. A discontinuity of the barrier in 25 µm micro-vias, shown in Figure 7, is observed. This figure shows thinning and gaps in micro-via walls near first metal layer below RDL. This condition is resulted in an electrical opening and is most likely due to a manufacturing defect. Micro-vias of 25 µm, 50 µm, and some of 75 µm, shown in Figures 5 through 7, are blind and appeared to be inverted. This observation is also shown in Ramakrishna et al. (2002b) and is due to an inadequate aspect ratio of the micro-via, which leads to the difficulty of depositing the thin layer of copper during the plating process and would result in the incomplete metallization. Note that the electrical opens, which were measured by the Anatech event detector, are consistent with hand probes, and the DPA results confirm electrical openings measured from testing equipment and hand-probing.

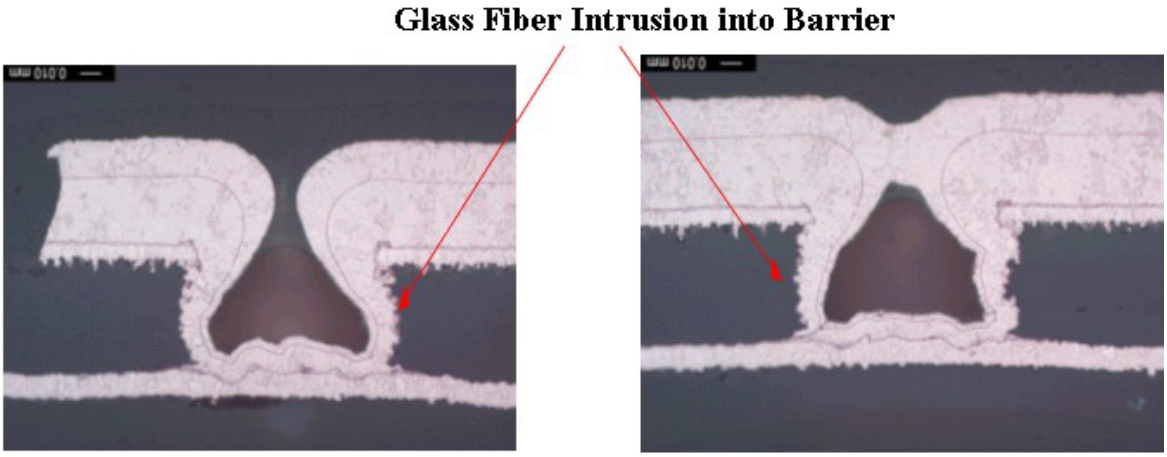


Figure 5 - Micro-section of 75 µm (or 0.003") Micro-via

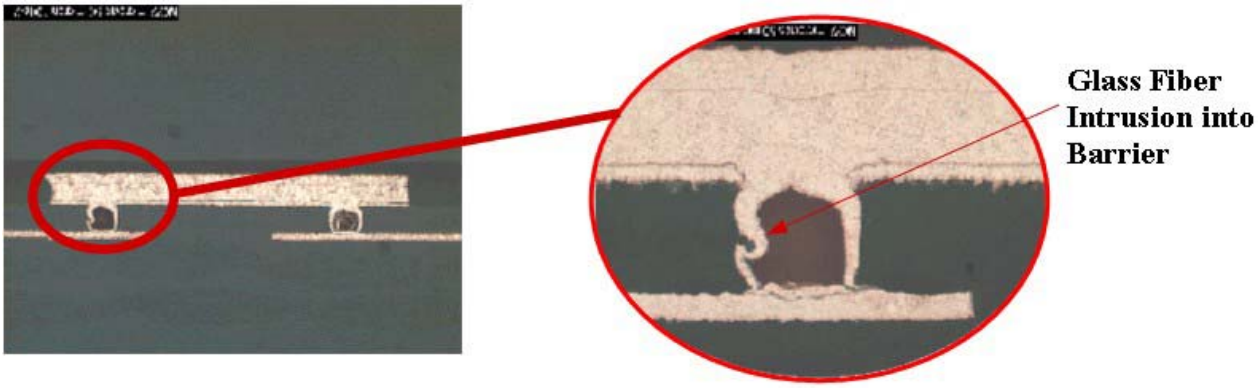


Figure 6 - Micro-section of 50 µm (or 0.002") Micro-via

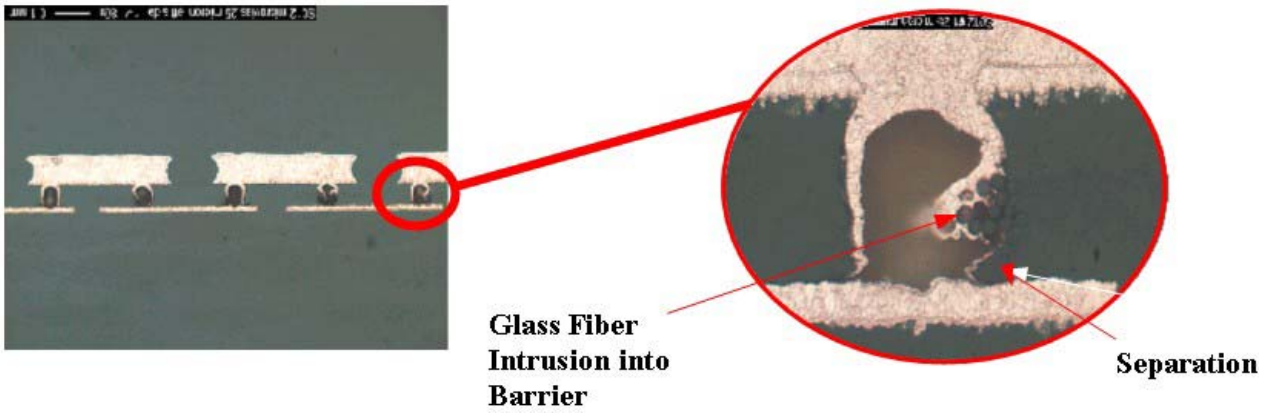


Figure 7 - Micro-section of 25 µm (or 0.001") Micro-via

Thermo-mechanical Analysis

A nonlinear finite element analysis (FEA) with ABAQUS computer code (HKS, 2002) is conducted to estimate the effective strain of the micro-via copper barrier during the temperature cycling. This derived strain is then used in Engelmaier's modified Coffin-Manson approach (Engelmaier, 1987) to predict the barrier fatigue life. The ABAQUS code is a general purpose FEA program with special emphasis on advanced nonlinear structural engineering applications.

Table 2 lists the material properties of copper and FR-4 PWB (Ramakrishna et al., 2002a/b). The plastic behavior of copper is represented by a bilinear kinematics hardening stress-strain curve. FR4 is modeled with elastic, transversely isotropic properties.

Table 2 - Material Properties

Material	Orientation	Elastic Modules, GPa	Poisson's Ratio	Thermal Expansion, ppm/°C
FR-4 PWB	**In-plane**	**24.4**	**0.14**	**16.2**
	Out-of-plane	**1.52**	**0.136**	**60.0**
*** Copper**	**Isotropic**	**103.4**	**0.34**	**17.0**

Note: All properties are between –55ºC and 125ºC
*** Yield strength = 172 MPa; Ultimate strength = 248 MPa; Elongation = 7%**

Figure 8 is the cut-through configuration of PWB stackup with the micro-via (116 μm diameter), which is the up-side-down of Figure 1. The idealized axisymmetric finite element model (FEM), generated using the MSC/PATRAN program, is shown in Figure 9. This model consists of 1333 elements and 1413 nodes. In the FEA, the effective strain of the copper barrier is calculated using an isothermal model, which starts at 25°C (strain free temperature) and cycled from –55°C to 125°C. The contour plots of the effective strains at –55°C and 125°C are shown in Figures 10 and 11. Fatigue life prediction model described in Eq. (1) from Engelmaier (1987), which relates the amount of copper strain range developed to the number of cycles needed to induce copper failure, N_f, is then used to estimate the micro-via fatigue life.

$$N_f^{-0.6} \times \varepsilon_f^{0.75} + \frac{0.9}{E}\sigma\left[\frac{e^{\varepsilon_f}}{0.36}\right]^{0.1785\log_{10}\left[\frac{10^5}{N_f}\right]} = \Delta\varepsilon_R \qquad (1)$$

where

ε_f	Fatigue ductility coefficient (0.15-0.25)
σ	Ultimate tensile strength
E	Elastic modulus
$\Delta\varepsilon_R$	Total strain range

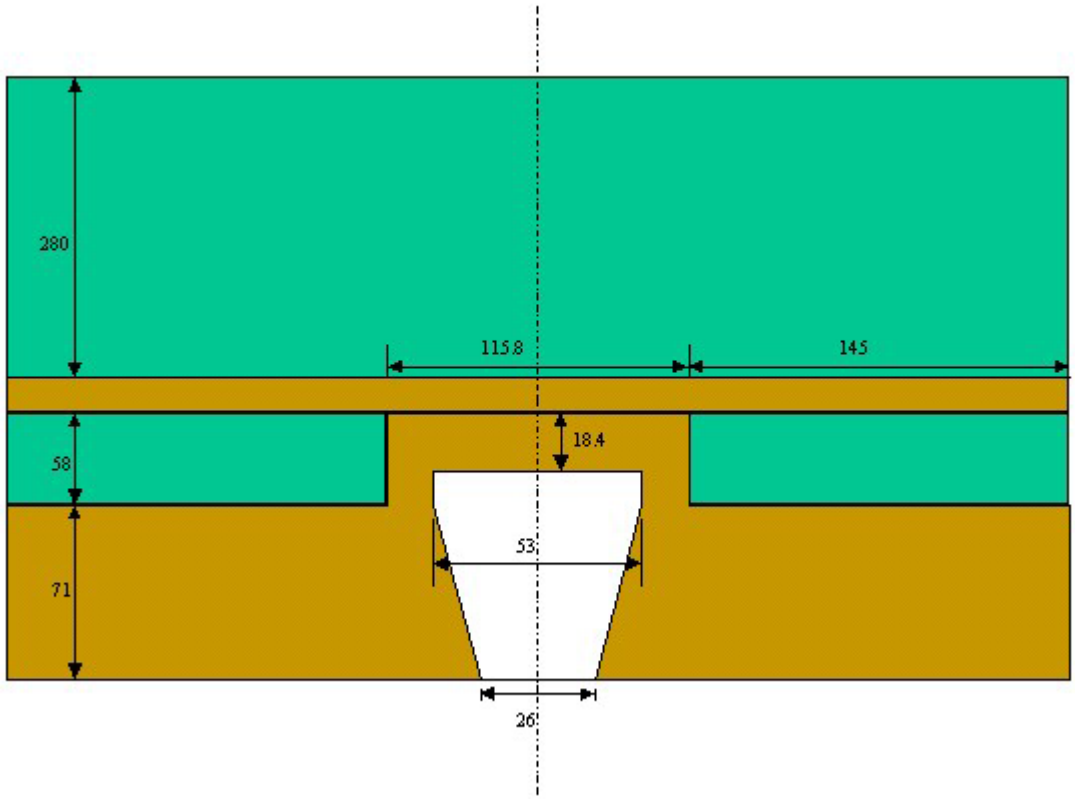


Figure 8 - Cut-through View of Micro-via (Up-side-down of Figure 1)

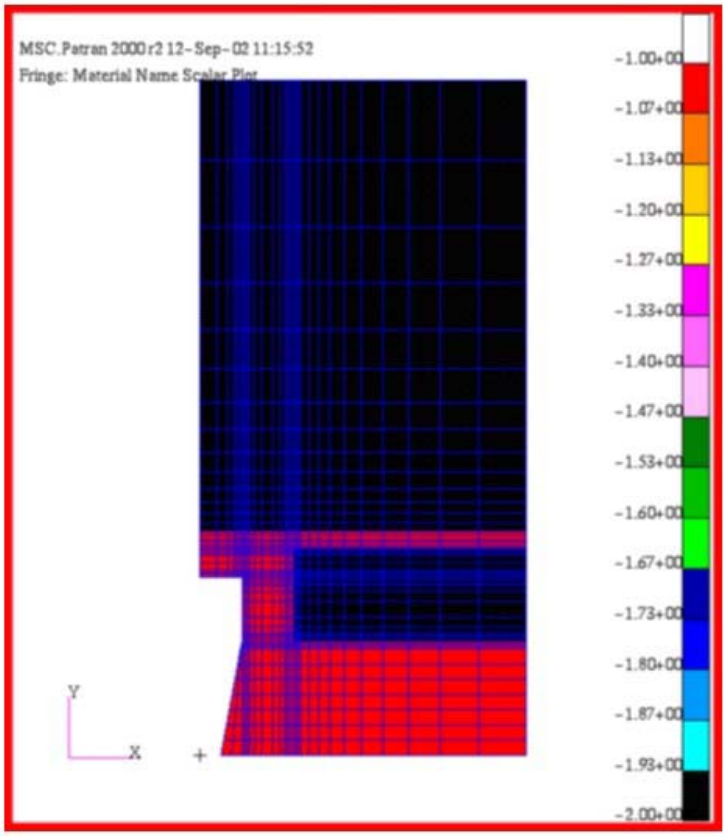
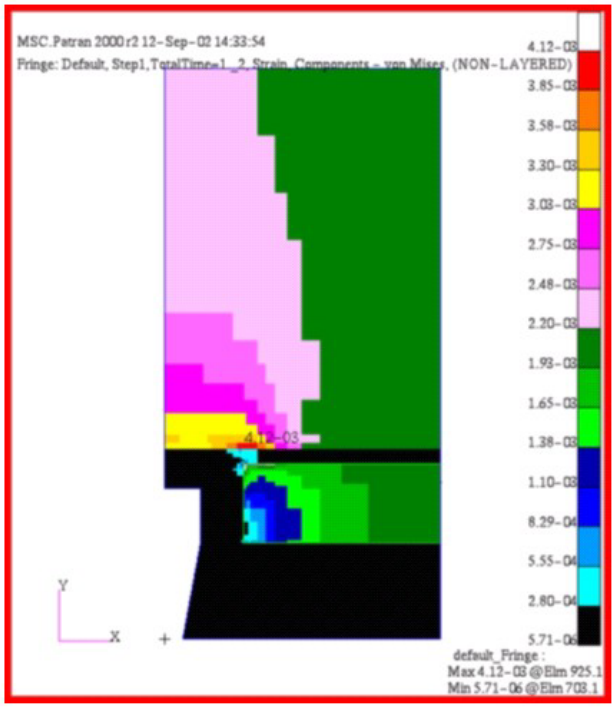
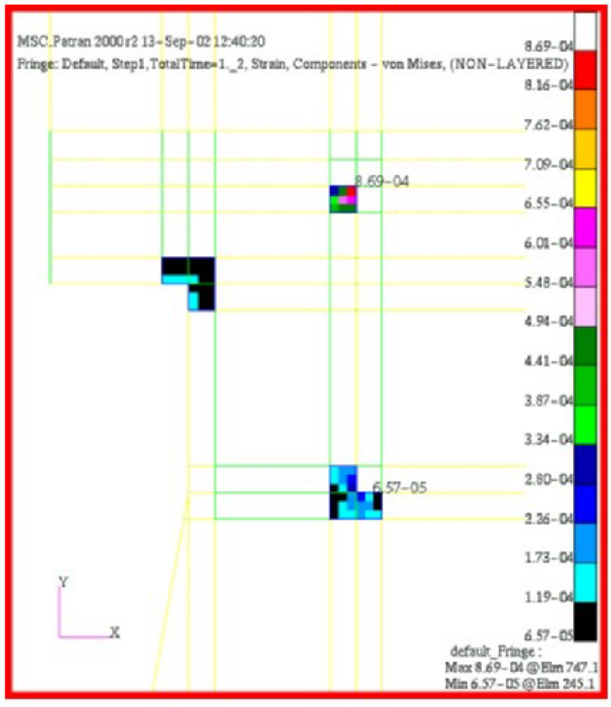


Figure 9 - Axisymmetric Finite Element Model of Micro-via

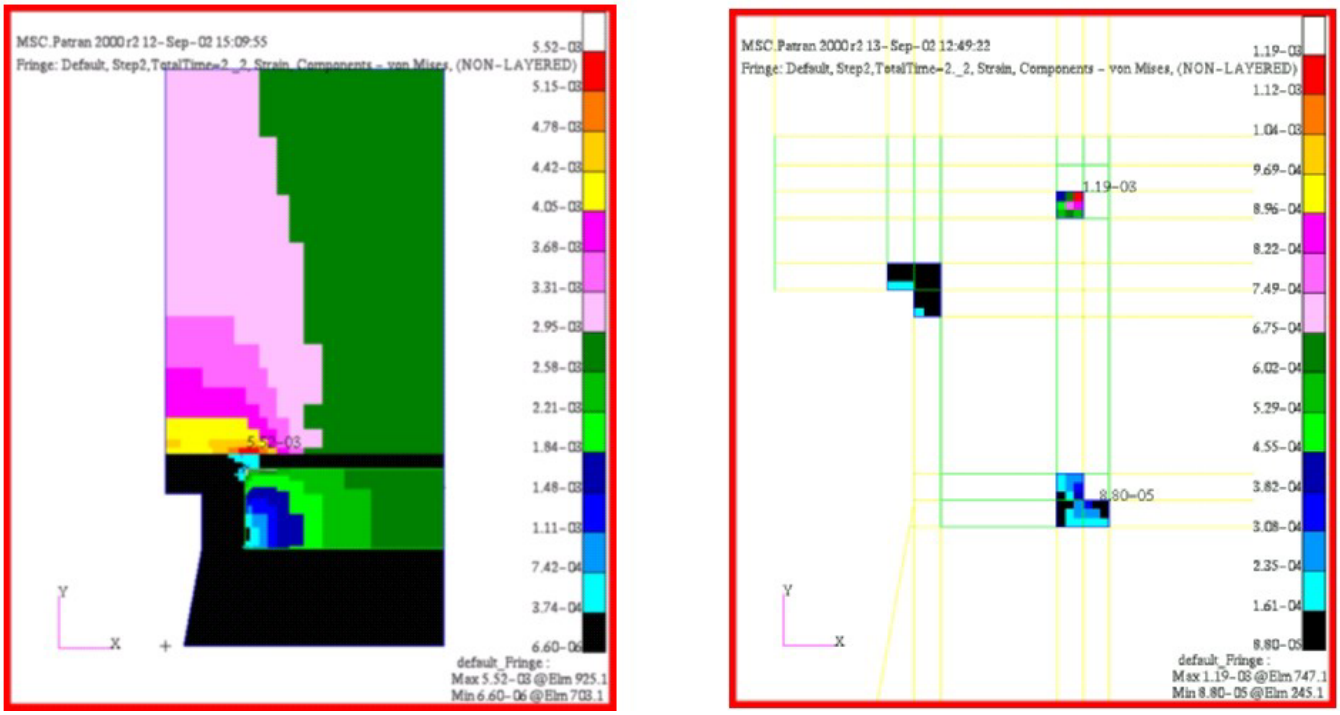


(a) Entire Model



(b) Critical Areas on Copper

Figure 10 - Effective Strain at -55°C



(a) Entire Model (b) Critical Areas on Copper

Figure 11 - Effective Strain at 125°C

It is well known that the derived values of strains are heavily dependent on finite element mesh size. The smaller the element size, the higher the resulting strain. This finite element mesh dependency is primarily due to the stress/strain singularity at the edge of a bi-material (Kuo, 1990/1997; Yin, 1992/1993). Therefore, to minimize the mesh dependence problem, a volume-weighted average method (Kuo, 1997) is used to compute an average value of the strain range per cycle over all the elements in the 5 □m by 5 □m (0.2 mil) critical corner area of the copper via. The micro-via thermal fatigue life is predicted to be 2607 cycles. This agrees with the test observation that the micro-via survives 1000 cycles without failure.

Summary and Recommendation

The TV with various configurations of micro-vias is designed, fabricated, and tested over military thermal environment. In this TV, the design/manufacturing process parameters are selected, which include solder mask on printed wiring board, micro-via pitch, and micro-via size, with each having either two or four levels of variation. After the temperature cycling test, a DPA based on monitored results is conducted to further isolate the failure locations and determine the failure mechanisms of the micro-vias. Test and DPA results indicate that: 1) the smaller sizes of micro-via are, the higher manufacture defects occur; 2) the micro-vias, having electrical continuities before the test, can survive 1000 temperature cycles; and 3) no influence or inclusive observation for the micro-via pitch variation impacting on the micro-via fatigue damage. In addition, a thermo-mechanical analysis with nonlinear finite element computer code applied in a 100 μm diameter micro-via is performed to illustrate this micro-via integrity when subjected to thermal cycling. Further evaluating the impacts of the micro-via pitch and diameter variations on the micro-via thermal fatigue damage by finite element analysis is recommended.

Acknowledgements

The authors would like to thank P.C. Chan, E. Cullens, J.M. Ickes, C.Y. Lau, M.J. Miranda, E.L. Craig, D.D. Kachuche, H.M. Cohen, D.R. Nelson, S.H. Mills, B.E. Oliver, and A.L. Truong from Raytheon Company for their contribution to this work.

References

1. Engelmaier, W. “Results of the IPC Copper Foil Ductility Round-Robin Study,” IPC Publication No. 947, 1987.
2. H.S. Fenger and T.E. Wong, “COTS BGA Thermal Fatigue Test for Avionics Applications,” Proceedings of InterPack’03, IPACK2003-35017, Maui, Hawaii, 6-11 July 2003.
3. Kuo, A.Y., “Thermal Stresses at the Edge of a Bi-Metallic Thermostate,” ASME J. of Applied Mechanics, Vol. 57, 1990, pp. 585-589.
4. Kuo, A.Y., W.L. Yin, D. Newport and M.Y. Chiang, “Generalized Stress Intensity Factor Concept for Fatigue and Fracture Evaluations of IC Package Solder Joints,” EEP-Vol. 19-2, Advances in Electronic Packaging, ed. by Suhir et al., 1997, pp. 1451-1460.

5. Lau, J.H., S.H. Pan, and C. Chang, "A New Thermal-Fatigue Life Prediction Model for Wafer Level Chip Scale Package (WLCSP) Solder Joints," Trans. of the ASME, Vol. 124, pp. 212-220, 9/2002.
6. Lau, J.H and S.W. Lee, Microvias for Low Cost, High Density Interconnects, McGraw-Hill, New York, NY, 2001.
7. Hegde, S., R.V. Pucha, and S.K. Sitaraman, "Enhanced Reliability of High Density Wiring (HDW) Substrates through New Dielectric and Base Substrate Materials," Proc. of IMECE 2002, the 2002 ASME Winter Annual Meeting, New Orleans, LA, 17-22 Nov. 2002.
8. HKS, Inc., ABAQUS Theory and User's Manuals, Version 6.3, 2002.
9. Paulus, J. and M. Petti, "Microvia Materials: Enablers for High Density Interconnects," International Symposium of Advanced Packaging Materials, pp. 31-38, 1997.
10. Ramakrishna, G., F. Liu, and S.K. Sitaraman, "Role of Dielectric Material and Geometry on the Thermo-Mechanical Reliability of Microvias," 52nd Electronic Components and Technology Conference, San Diego, CA, 28-31 May 2002a.
11. Ramakrishna G., F. Liu, and S.K. Sitaraman, "Experimental and Numerical Investigation of Microvia Reliability," 2002 Inter Society Conference on Thermal Phenomena, San Diego, CA, 5/2002b.
12. Rasul, J., W. Bratschun, and J. McGowen, "Microvia Bare Board Reliability Assessment," IPC EXPO 1997, pp. S17-5-1 to S17-5-6, 1997.
13. Wong, T.E., C.Y. Lau, L.A. Kachatorian, H.S. Fenger and I.C. Chen, "Design of Experiments in Ball Grid Array Thermal Fatigue Life Tests," Proc. of IMECE 2002, the 2002 ASME Winter Annual Meeting, New Orleans, LA, 17-22 Nov. 2002.
14. Wong, T.E. and H.S. Fenger, "Vibration Fatigue Test of Surface Mount Electronic Components," Proceedings of InterPack'03, IPACK2003-35031, Maui, Hawaii, 6-11 July 2003.
15. Yin, W.L., "Refined Variational Solutions of the Interfacial Thermal Stresses in a Laminated Beam," ASME J. of Electronic Packaging, Vol. 114, 1992, pp. 125-140.
16. Yin, W.L., "The Effects if Inclined Free Edges on the Thermal Stresses in a Layered Beam," ASME J. of Electronic Packaging, Vol. 115, 1993, pp. 208-213.

Design of Experiment in Micro-Via Thermal Fatigue Test

T. E. Wong*, H. S. Fenger, and I. C. Chen

Raytheon Electronic Systems
El Segundo, California

***310-334-5668 (O)**
tse_e_wong@raytheon.com

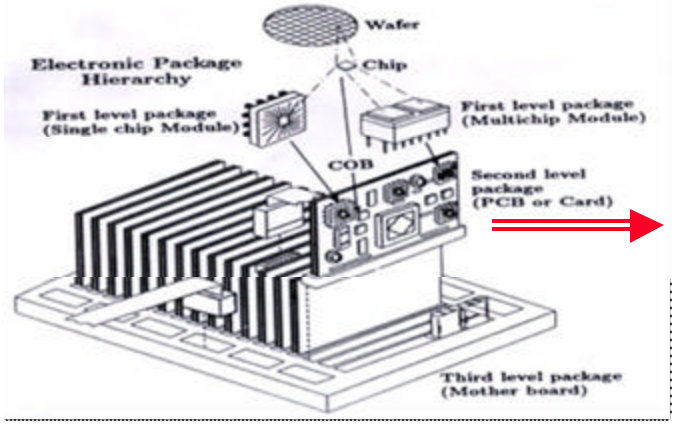
February 24-26, 2004

Outline

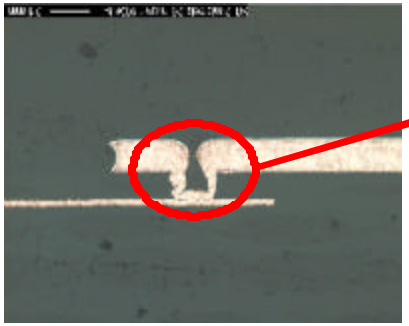
- Background
- Objective & Approach
- Test Vehicle
- Experiment
- Failure Analysis
- Thermo-mechanical Analysis
- Summary & Recommendation

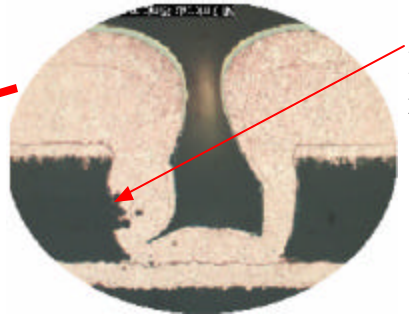
Background

- There is a need to use micro-via in printed wiring board (PWB) to achieve a finer pitch of the substrate's solder pad
  - Direct chip attach (DCA) or wafer-level chip scale package (WL-CSP) is directly soldered onto PWB
- The micro-via barrier cracking is a great concern during temperature cycling
  - Thermal fatigue damage is induced by coefficient of thermal expansion (CTE) mismatch



Micro-section of 0.004" (or 100 µm) Micro-via





Glass Fiber Intrusion into Barrier

Objective & Approach

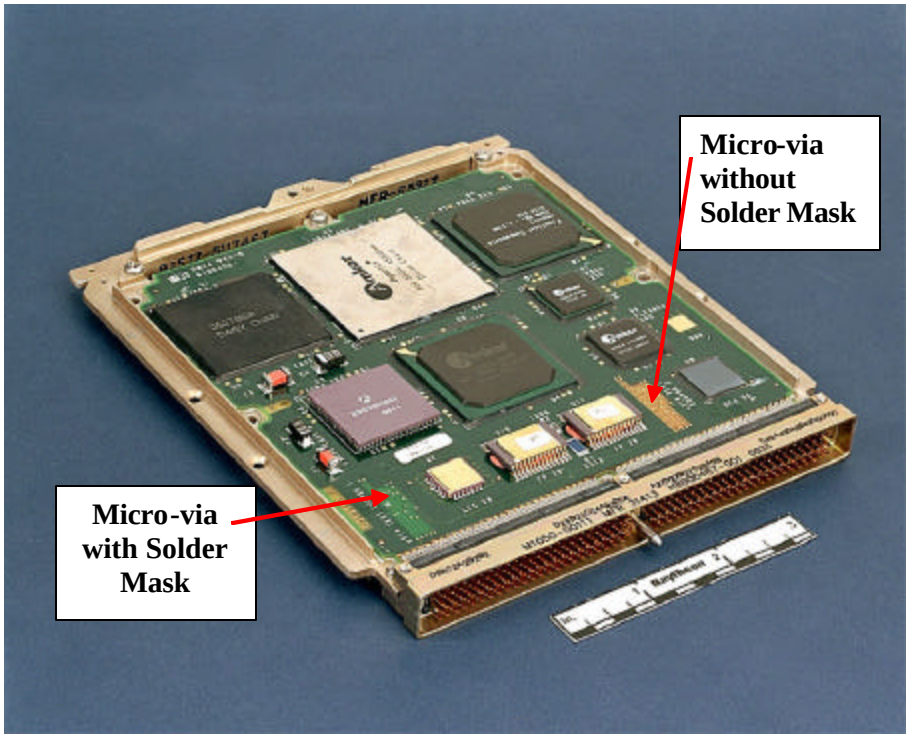
- **Objective**
  - **Evaluate the impacts of micro-via design/manufacturing process variables on the thermal fatigue damage of the micro-vias**
- **Approach**
  - **Design and fabricate an electrical daisy-chain patterned PWB assembly test vehicle (TV) with various configurations of micro-vias**
    - » **Including four different diameters in micro-via (each with a different micro-via pitch) and two solder mask types (including no solder mask).**
    - » **Total of 26 TVs**
  - **Conduct temperature cycling test with continuously monitoring the micro-via electrical continuity**
  - **Perform destructive physical analysis (DPA) to further isolate the failure locations and determine the failure mechanisms of the micro-vias**
  - **Conduct a thermo-mechanical analysis with nonlinear finite element code to illustrate the micro-via integrity when subjected to thermal cycling**

Test Vehicle

- **Design/manufacturing process parameters and their variation levels**

Para-meter	Description	Level			
		1	2	3	4
A	Micro-via Diameter / Pitch (in.)	0.004/ 0.05	0.003/ 0.035	0.002/ 0.02	0.001/ 0.01
B	Solder Mask	No	Yes	-	-

- **Each side of aluminum heat sink bonded with a high Tg FR-4 single-side circuit card assemblies (CCAs)**

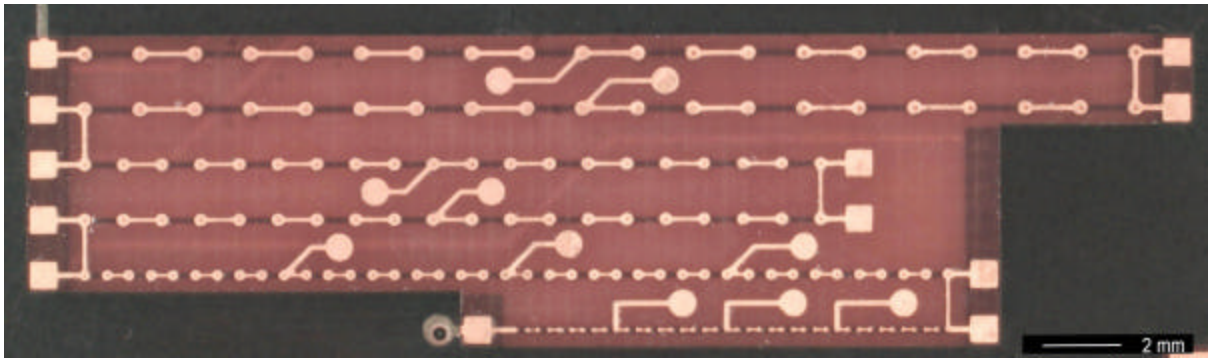


035-4005180

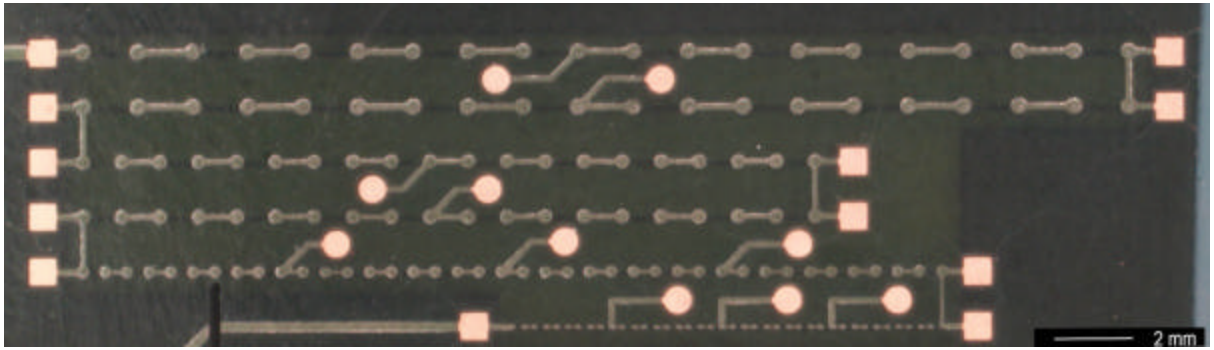
Test Vehicle

Raytheon

- Micro-via lay-out configurations
  - Measurement pads are available for hand probes
  - Only one net is used for each CCA
  - Micro-via without solder mask



  - Micro-via with solder mask



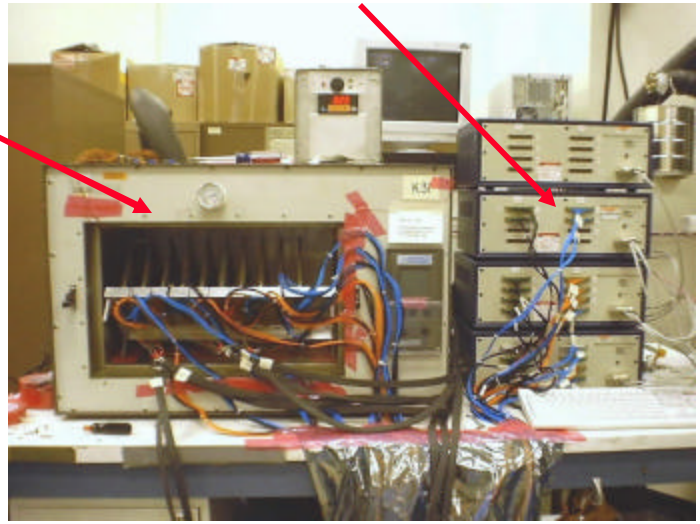
Diameter	Pitch
0.004”	0.05”
0.003”	0.035”
0.002”	0.02”
0.001”	0.01”
0.004”	0.05”
0.003”	0.035”
0.002”	0.02”
0.001”	0.01”

Experiment

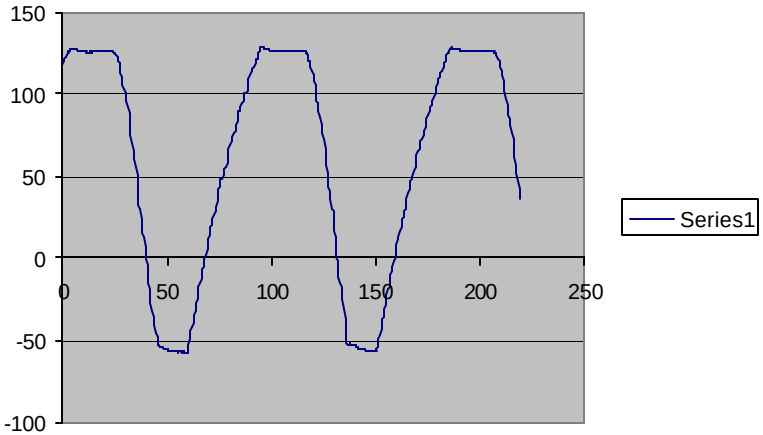
- Temperature cycling profile is 20-minute dwell at hot and a 10-minute dwell at cold, and ramp rates of 5.5±1°C/minute going hot and 10±1°C/minute going cold
- The total number of thermal cycles is 1000
- Visual inspection of the micro-vias is performed at 327, 701 and 1000 cycles
- Four Anatech Event Detectors are used to continuously monitor the electrical openings
- The electrical failure is defined as a resistance change of 500 ohm within 0.2 microsecond
  - The higher resistance change is selected for overcoming the noise effects during test

Anatech Event Detector

Thermal Chamber



Temperature Cycling Profile



Experiment

- Prior to the thermal cycling test
  - Measurements from Anatech Event Detectors show opens in many TVs
  - Hand probes are conducted for each size of micro-vias and show that
    - » Electrical contact exists in 0.002”, 0.003” and 0.004” micro-vias
    - » Electrical opens in 0.001” micro-via
- After the completion of 1000 thermal cycles
  - No additional electrical open is measured by Anatech Event Detectors
  - Hand probes are also performed and no additional electrical failure is observed
- The electrical opens, which are measured by Anatech Event Detectors, are consistent with hand probes

Failure Analysis

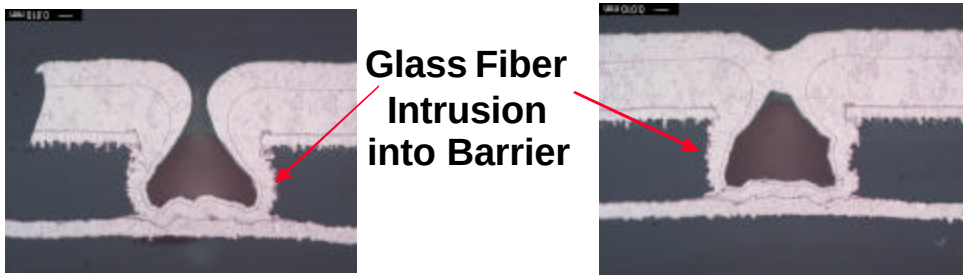
Raytheon

- **Post-thermal cycling failure analysis methodology**
  - **The micro-vias that show electrical opens are selected for sectioning**
  - **The sections are taken first through the outermost row of micro-vias that are indicated as having electrical opens**
  - **Evidence of opens is taken to be cracking that completely traverses the micro-via**
  - **If no physical evidence of the opens is found in the first level of sectioning, then additional sectional levels are taken**
- **DPA results confirm electrical openings measured from Anatech Event Detectors and hand-probing**

Failure Analysis

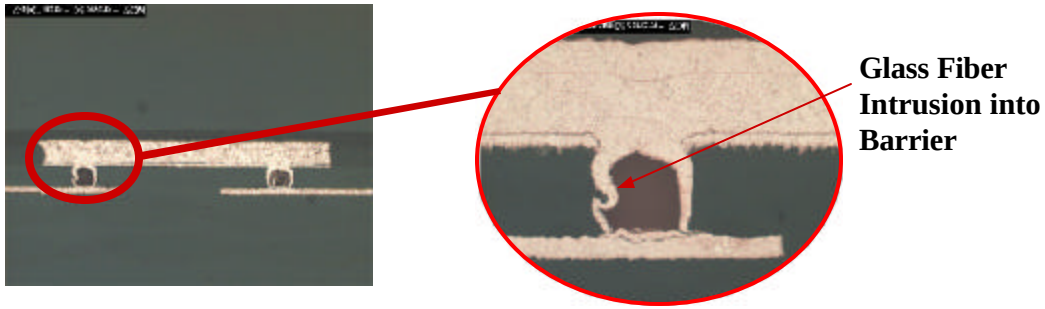
Raytheon

Micro-section of 0.003” (or 75 µm) micro-via

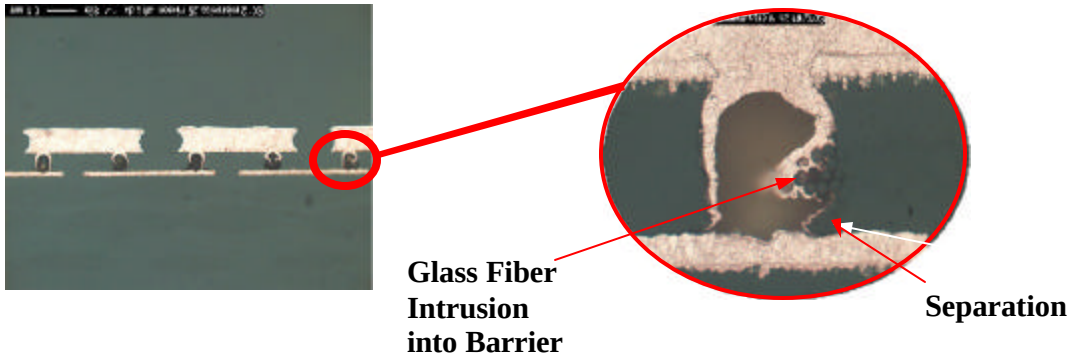


- Blind vias are observed in 0.001”, 0.002”, and some of 0.003” micro-vias
- Electrical opens are measured in most of 0.001” micro-via and also confirmed by DPA

Micro-section of 0.002” (or 50 µm) micro-via



Micro-section of 0.001” (or 25 µm) micro-via



Thermo-mechanical Analysis

Raytheon

- Analysis characteristics
  - Axisymmetric finite element model
  - Nonlinear analysis
    - » Material plasticity
  - Loading & boundary conditions

- Material properties

Material	Orientation	Elastic Modules, GPa	Poisson's Ratio	Thermal Expansion, ppm/°C
FR-4 PWB	In-plane Out-of-plane	24.4 1.52	0.14 0.136	16.2 60.0
* Copper	Isotropic	103.4	0.34	17.0

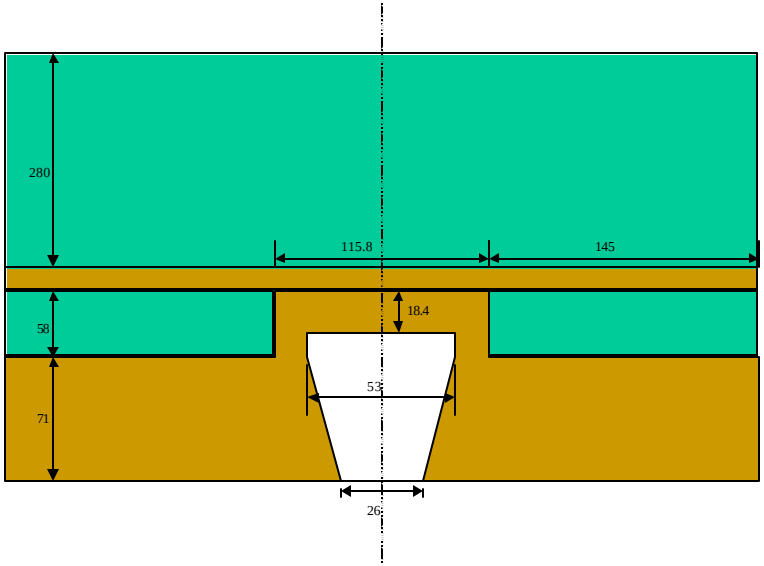
Note: All properties are between –55ºC and 125ºC

*Yield strength = 172 MPa; Ultimate strength = 248 MPa; Elongation = 7%

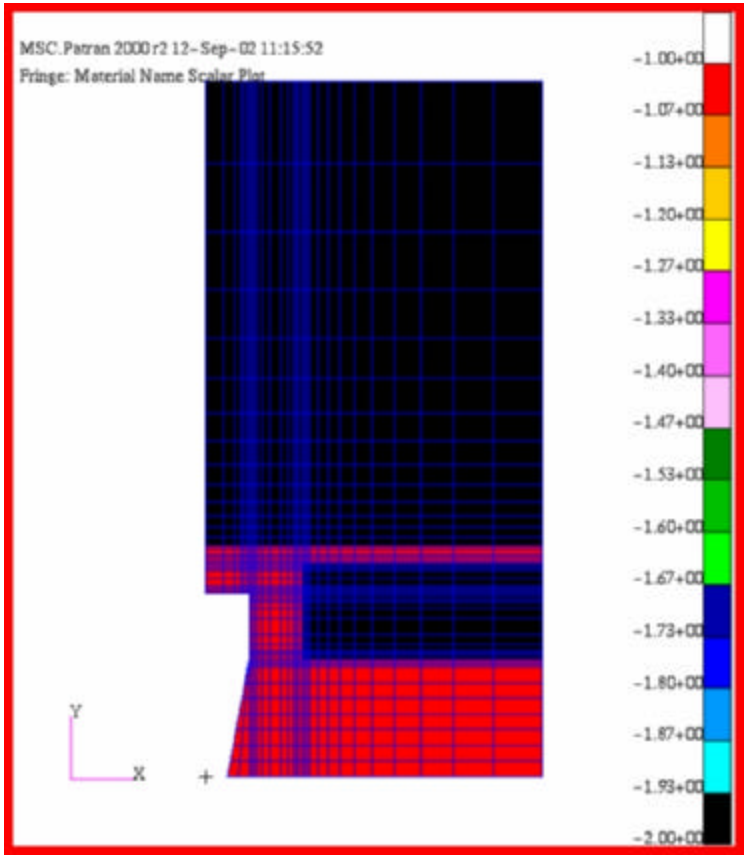
Thermo-mechanical Analysis

Raytheon

Cut-through view of 0.004” micro-via (Up-side-down of micro-section)



Axisymmetric finite element model

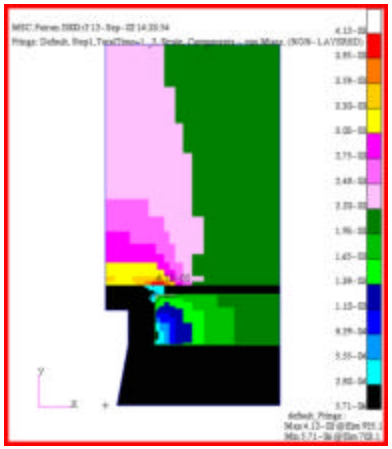


Thermo-mechanical Analysis

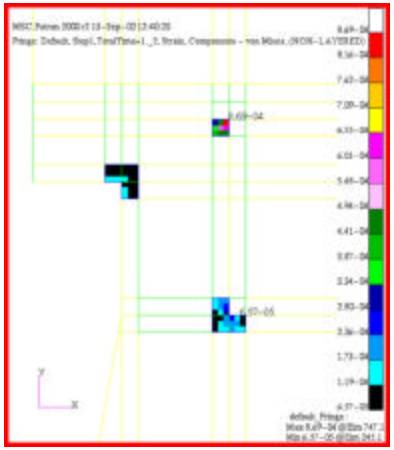
Raytheon

- **Effective strain at -55°C**

Entire Model

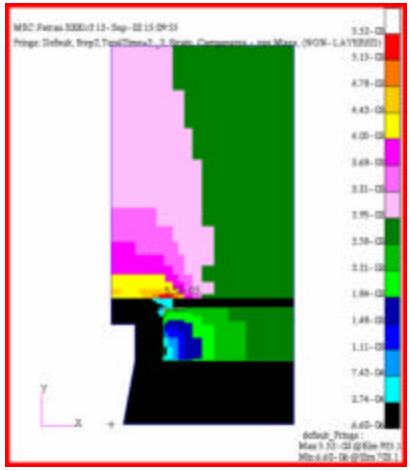


Critical Areas on Copper

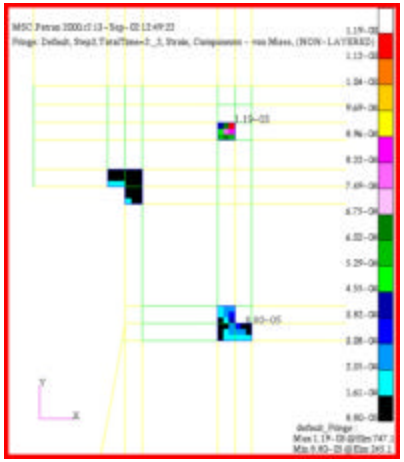


- **Effective strain at 125°C**

Entire Model



Critical Areas on Copper



Thermo-mechanical Analysis

Raytheon

- **Thermal fatigue life prediction model of copper (based on modified Coffin-Manson approach)**
  - **Volumetric average of strain per cycle over all the elements in 0.2 mil by 0.2 mil critical corner area of the copper via is used for fatigue life prediction**

$$N_f^{-0.6} \times e_f^{0.75} + \frac{0.9}{E} s \left[\frac{e^{e_f}}{0.36} \right]^{0.1785 \log_{10}\left[\frac{10^5}{N_f}\right]} = \Delta e_R$$

e_f: Fatigue ductility coefficient (0.15-0.25); **s: Ultimate tensile strength**

E: Elastic modulus; **? e_R: Total strain range**

- **The predicted micro-via thermal fatigue life is 2607 cycles, which agrees with the test observation that the micro-via survives 1000 cycles without failure**

Summary & Recommendation

- TV with various configurations of micro-vias is successfully designed, fabricated, and tested over military thermal environment
  - Design/manufacturing process parameters are
    - » Four different diameters in micro-via (each with a different micro-via pitch)
    - » Two solder mask types (including no solder mask)

- Test, DPA, and finite element analysis results indicate that
  - The smaller the micro-via sizes, the higher the occurrence of manufacturing defects
  - The micro-vias, having electrical continuities before the test, can survive 1000 temperature cycles
  - There is no influence or inclusive observation of the micro-via pitch variation on the micro-via fatigue damage
  - Predicted micro-via thermal fatigue life is consistent of test observation

- Further evaluating the impacts of the micro-via pitch and diameter variations on the micro-via thermal fatigue damage by finite element analysis is recommended