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Novel Polyimide Build-up Material for Fine-line Fabrication

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Abstract
We have developed a new thermosetting polyimide build-up material for high performance build-up PWBs, which can mount high speed CPUs with high I/O numbers. These PWBs meet the following requirements; good processability for the fine-pitched circuits, the low dielectric characteristics, and the excellent mechanical properties.

Our proposed polyimide build-up material shows a dielectric constant (Dk) of 3.1 and a dielectric loss (Df) of 0.01 (at 1GHz). Moreover the material shows following mechanical properties; a low coefficient of thermal expansion (CTE) of 45ppm and a tensile strength of 100MPa. Even though the material has a low surface roughness Ra of less than 200n meters, we have successfully deposited an electro-less plated copper layer with very high peel strength. This means that the material is suitable for fabricating fine-pitched circuits, even when using a conventional semi-additive process. Actually, we could make a fine-pitched circuit of less than 10micron L/S (Line and Space).

Introduction
In recent years electronic equipment has been required to have many functions and a high processing speed. To meet these requirements, IC chips, like high performance CPUs have evolved to have high clock frequencies and high I/O numbers. To mount the CPUs to the substrate, the flip chip attachment method is usually adopted to exhibit the maximum performance of CPUs and it is necessary for the substrates to a have high wiring density. Build-up PWBs whose circuits are formed by the semi-additive method have been used for these substrates.

Next generation build-up PWBs for next generation CPUs, which are expected to have higher I/O numbers, are required to have fine-pitched circuits of less than 20 micron L/S (Line and Space). For the fabrication of the fine-pitched circuits, it is important for the build-up material on which the fine-pitched circuits are formed to have as a small amount of surface roughness as possible and an ability to adhere the circuits without peeling off.

Epoxy resin has been mainly used for build-up material. The epoxy type build-up material is processed to make the material's surface rough and to firmly adhere the circuit by an anchor effect. For the fabrication of next generation fine-pitched circuits of less than 20 micron L/S, a new build-up material is desired which has a smaller amount of surface roughness than the existing material and good adhesion with the circuit. Furthermore the new build-up material must have a low CTE (Coefficient of Thermal Expansion) and low dielectric properties, which will improve the electrical reliability or electrical properties of the build-up PWBs.

For the development of next generation build-up material, we started to develop a new polyimide build-up material expecting superior properties based on the properties of polyimide resin that has been used for electric insulation material. As a result of this investigation, we developed a novel thermosetting polyimide build-up material that meets the requirement mentioned above. In this paper, the thermal properties, the dielectric properties around gigahertz (GHz), the peel strength of electro-less plated copper layer on the materials, the processability of fine-pitched circuit by semi-additive process and LASER via processability are evaluated.

Target Properties of the New Build-Up Material
First in the development, the target properties for new build-up material were designed.
- -A coefficient of thermal expansion (CTE) less than 50 ppm
- -A dielectric loss (Df) of less than 0.010 at 1GHz
- -A mechanical strength over 100MPa
- -Flame resistance without a halogenated compound
- -The processability of a fine-pitched circuit less than 20 micron L/S by semi-additive process

Evaluation of the New Build-Up Material
Formation of Finely Roughened Build-Up Material's Surface
To fabricate the fine-pitched circuit by semi-additive process, the build-up material needs to have a surface with a small amount of surface roughness and a high peel strength with an electro-less plated copper layer. In this investigation the replica

method is used to make a finely roughened surface of the material. In the replica method, finely roughened copper foil surface is transcribed to the surface of the build-up material, i.e. the copper foil is laminated to the build-up material using vacuum press machine and then the copper foil is removed from the build-up material by an etching process. The copper foil used in this investigation has a very small surface roughness of Rz less than 1.5 microns. Figure1 shows a SEM image of the material's surface after removing the copper foil and applying de-smear treatment, consisting of sodium permanganate. Figure2 shows a surface roughness measurement chart of the same surface measured by New View 5000 3-D Surface Profilers (Zygo corporation product). A finely roughened surface is observed in figure 1 and the surface roughness was evaluated to have an Rz of 1.1 micron and an Ra of 0.17 micron.

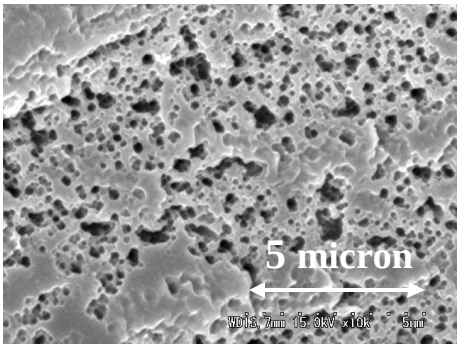

Figure 1 - SEM Image of the Build-Up Material's Surface Made by the Replica Method

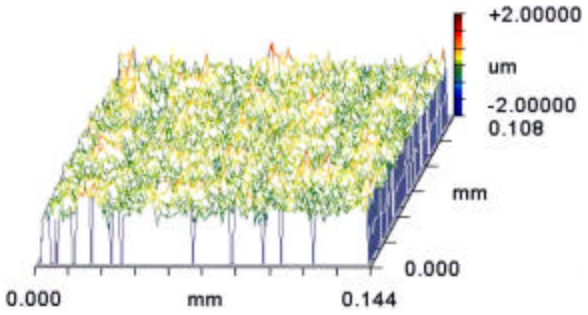

Figure 2 - 3D Surface Profile of the Build-Up Material's Surface (Rz=1.1micron and Ra=0.17micron)

Measurement of Peel Strength

Electro-less copper was plated on the surface of the build-up material on which the replica was formed. After electrolytic copper was deposited on up to 18 micron, peel strength was measured according to JIS C6471. The result is shown in Table1. Despite a small amount of surface roughness, the peel strength is high enough for practical use even after the conditioning of PCT or aging. We suppose that this high peel strength is caused not only by the anchor effect but also by the chemical interaction between the polyimide resin and the electro-less copper.

Table 1 - Results of Peel Strength

Conditions	Peel strength
As received	9N/cm
After PCT (96hr/121dC/100%RH)	6N/cm
After aging (240hr/150dC)	7N/cm

Processability of Fine-Pitched Circuit

The processability of fine-pitched circuit is evaluated according to the process shown in Figure 3. Copper foil, build-up material and core BT substrate were stacked and laminated using a vacuum press machine under the condition of 1hr/3MPa/180dC. The copper foil is then removed by an etching process from the laminate, and then desmear and electro-less copper plating is applied onto the surface of the build-up material. Dry film resist (DFR) used in the resist development process, was Sunfort (TM), which was supplied by Asahi Kasei Electronics Materials & Device. The DFR is processed to make the pattern of resist materials, and then pattern electrolytic copper plating is applied. After removing the resist pattern the flash etching process consisting of sulfuric acid-hydrogen peroxide is applied.

The SEM image of 20 micron and 10 micron pitched copper circuit are shown in Figures 4 and 5 respectively. The circuits are observed to have a good rectangular shape; therefore the build-up material is proven to have a good compatibility for the fine-line fabrication with the replica method. Furthermore the space area between two copper lines was analyzed by EDX and it was confirmed that no residue of Cu element was observed. Superior insulation property between the lines can be expected.

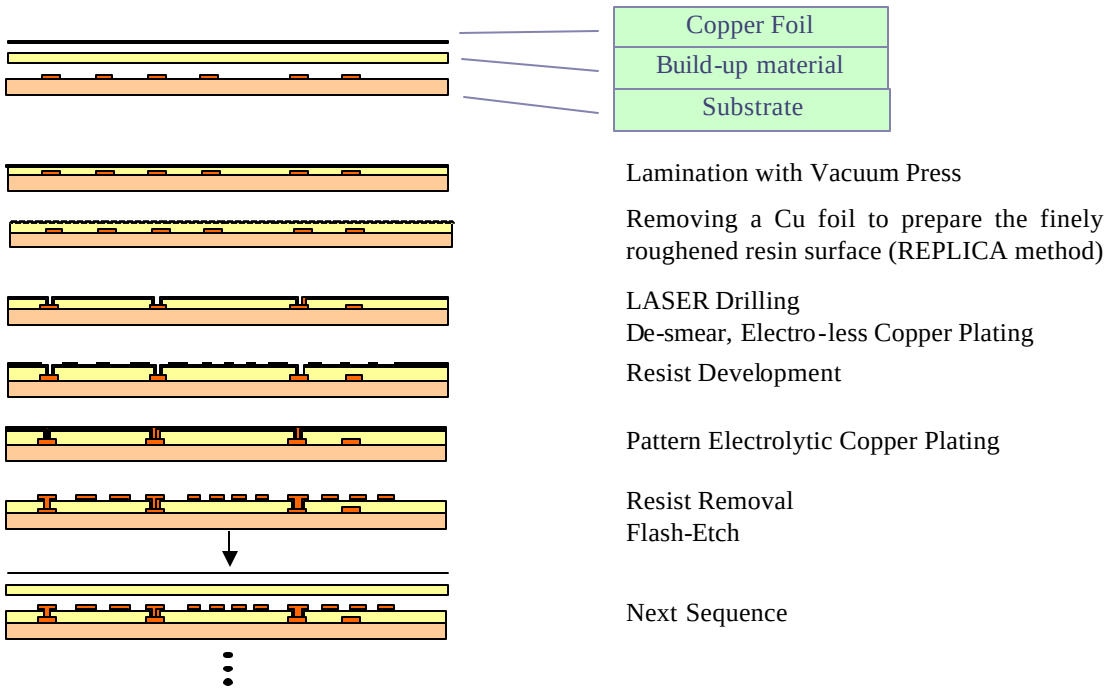

Figure 3 – Typical Manufacturing Process of Build-Up PWB

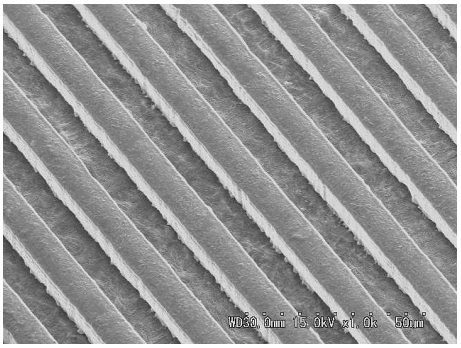

Figure 4 - SEM Image of 20 Micron (L/S=10/10) Pitched Circuit

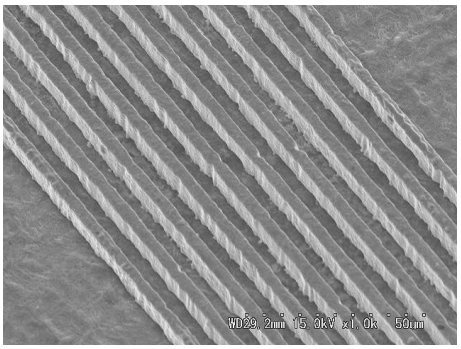

Figure 5 - SEM Image of 10 Micron (L/S=5/5) Pitched Circuit

Laminate Property

Figure 6 and 7 show the cross sections of laminating build-up material 2 to the copper circuit fabricated on the build-up material 1. The laminating process was carried out under the condition of 1hr/3MPa/180dC using a vacuum press. No voids can be observed near the bottom of the circuit; the build-up material is found to fill well into the space area between the circuits and to have a good laminate properties.

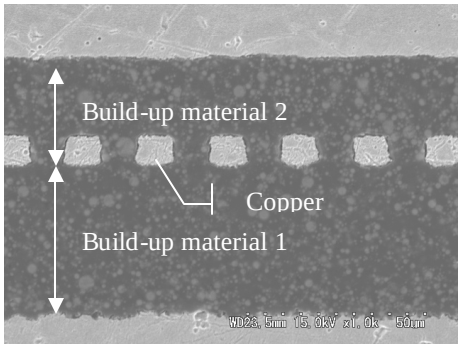

Figure 6 - Cross Section of Laminate (20 Micron Pitched Circuit)

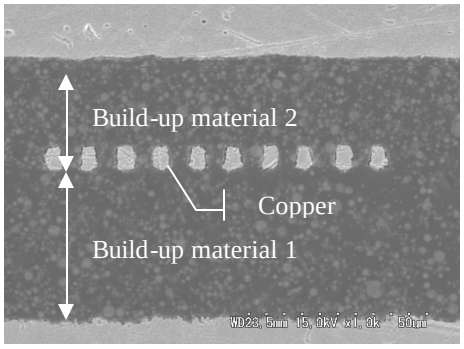

Figure 7 - Cross Section of Laminate (10 Micron Pitched Circuit)

LASER Via Formation

Figure 8 shows a SEM image of 50 micron via drilled by UV-YAG LASER and Figure 9 shows a cross section after plating. Fine shape of the via is observed from the picture, it was found that the material is supposed to be suitable for LASER via formation.

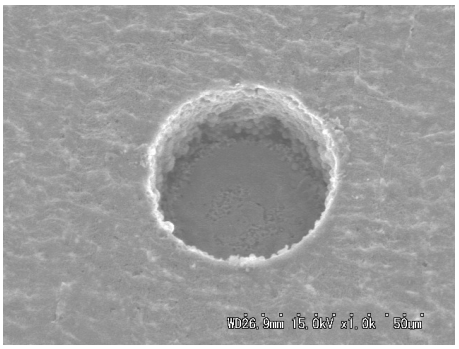

Figure 8 - SEM Image Of Via Formed By UV-YAG LASER (Before Plating)

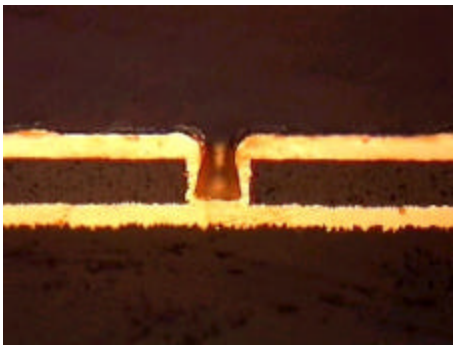

Figure 9 - Cross Section Of Via Formed By UV-YAG LASER (50 Micron Diameter, After Plating)

Properties for the New Build-Up Material

The properties for the new build-up material are summarized in table 2. Remarkable electrical properties such as low dielectric loss of 0.010 and high insulation resistance after HAST are realized. High volume resistance of over 1.0E+16ohm*cm is realized even in high temperature of 125ºC, which is the temperature expected as the junction temperature of next generation semiconductors and over 5.0E+12ohm*cm of volume resistance is required for the next generation build-up material.[1]

Excellent thermal and mechanical properties are recognized, i.e. low coefficient of thermal expansion as less as 45ppm, high thermal decomposition temperature over 400ºC, tensile strength as high as 100MPa, and V0 equivalent without halogenated compound. The origin of these properties is supposed to be based on the properties of polyimide.

Table 2 - Properties for the New Build-Up Material

	Conditions	Measured values
Material type	---	Film
Water absorption	D24/23	0.7%
Glass transition temperature	TMA DMA	150ºC 167ºC
Coefficient of thermal expansion	-55-125ºC	45ppm
Thermal decomposition temperature	TGA	>400ºC
Tensile modulus	RT	4.1GPa
Tensile strength		100MPa
Elongation to break		6%
Dielectric constant	1GHz Resonance cavity method	3.0
Dielectric loss		0.010
Insulation resistance	HAST, 3.3V biased, thickness of dielectric is 20 micron	>200 hr > 1.0E+9 ohm
Volume resistance	RT 125ºC	>1.0E+16 ohm*cm >1.0E+16 ohm*cm
Peel strength with electro-less copper (Replica method)	Thickness 18 micron As received After PCT (96hr/121ºC/100%RH) After aging (240hr/150ºC)	 9N/cm 6N/cm 7N/cm
Solder heat resistance	JEDEC LV3	Pass
Flammability rating	UL-94	V0 equivalent Halogen free

Conclusions

We have developed a new thermosetting polyimide build-up material, which shows superior electrical and mechanical properties, and we believe that this material has a potential for next generation build-up material.

Reference

1. K. Kobayashi, K.Yamanaka, H.Mori, Y.Tsukada, Micro Electronics Symposium 2001, p355