Presented in the ECWC 10 Conference at IPC Printed Circuits
Expo®, SMEMA Council APEX® and
Designers Summit 05

Use of Novel Adhesive-lined CCL Material in Single-pressed Multi-layer Circuit Boards with Inner Via-Holes in all Layers

Daisuke Kanaya, Shuji Maeda, Keiko Kashihara and Kenji Ogasawara
Matsushita Electric Works, Ltd.
Osaka, Japan

Abstract
This newly developed material and process enable the manufacturing, using a single pressing process, of multi-layer circuit boards with inner via-holes in every layer. Because this material utilizes conventional circuit board materials for its structural components, it not only provides proven high reliability and ease of circuit assembly, but also offers a short lead-time and high production yield due to adoption of the following processes used during the manufacture of conventional printed circuit boards.

- Use of a multi-layer substrate consisting of copper foil, glass-cloth-based insulation layer, adhesive layer, and cover film
- Application of an etching process to the copper foil to produce a fine-patterned circuit
- Generation of blind via-holes using laser processing and hole cleaning
- Formation of via-bumps by filling metal-based paste and removing the cover film
- A multi-layer circuit board with inner via-holes in all layers can be produced by aligning the insulation layers and pressing them together in a single operation.

The materials used in this process require a variety of key technologies that enable laser processing, dimensional control, conductive paste filling etc. This paper describes these techniques and includes an example of the production of a multi-layer circuit board in a single pressing operation, followed by reliability evaluation results for the whole circuit board.

Introduction
Electronic equipment manufacturers are under pressure to create ever smaller but increasingly feature-packed designs. Densely packaged build-up type printed wiring boards (PWBs) have been proposed since the 1990s as a potential strategy for reconciling these two conflicting demands.[1, 2] Build-up type PWBs are increasingly used in electronic equipment due to their greater suitability for fine-pattern wiring than conventional PWBs, but the demand for increased functionality requires more and thinner layers plus smaller through-holes in the core board. To meet these requirements, the focus is now on the all-layer IVH (interstitial via-holes) structure board, which allows increased freedom of wiring design and the faster signal transmission speeds needed for performance improvement, as well as the mass multi-layer process that is suited to short product lifecycles. Although a variety of all-layer IVH structure boards and mass-pressed multi-layer process have been proposed[3], the need for special materials and their complex manufacturing process has restricted their broader application. Thus, improvements in both material and process are urgently needed for expanding their application. Our newly developed technology is capable of easily and simultaneously realizing an all-layer IVH structure board and mass-pressed multi-layer process by applying the new materials and related processes. The new material is based on thermosetting resin, which has a long history of use as PWB material. The manufacturing process adopts conventional PWB process technology and infrastructure, which means that a slight extension of the conventional multilayer board manufacturing process can enable production of all-layer IVH boards with high via positional accuracy.

Newly Developed Materials
Shown in Figure 1 are the newly developed material configurations and the function/feature of each layer. The developed material consists of four layers of copper foil, a glass-based thermosetting resin layer (hereafter referred to as the thermosetting layer), a B-stage adhesive layer and cover film. The adhesive layer and its protective cover film are attached to the thermosetting layer with copper foil. The most important task we faced in material development was controlling dimensions during pressing by separating the function of the insulation layer and adhesive layer. The key point in manufacturing all-IVH boards is to maintain the positional accuracy of each layer with more precision than that required for a normal multi-layer board, since all boards feature a 'stacked via' structure, in which via-holes are positioned above other via-holes. The currently proposed materials, by utilizing a fully cured insulation layer as the lamination material, are capable of maintaining far better dimensional accuracy than would a lamination process using non-cured materials such as pre-preg.

The four-layer structure with the cover film protecting the adhesive layer from the beginning of the process facilitates the use of a wet etching process, enabling the application of unique and entirely novel circuit configurations. In addition, even the thinnest gauge of single-sided CCL (Copper-clad Laminate) board responds to conventional handling methods in the manufacturing process.

Table 1 shows the typical characteristics of the material. The adhesive layer has been newly designed based on the thermosetting resin proven in PWB applications, but the melting viscosity is fine-tuned to the manufacturing process discussed below. The material type for the thermosetting layer and copper foil may be selected from a wide array of copper-lined laminated board materials.

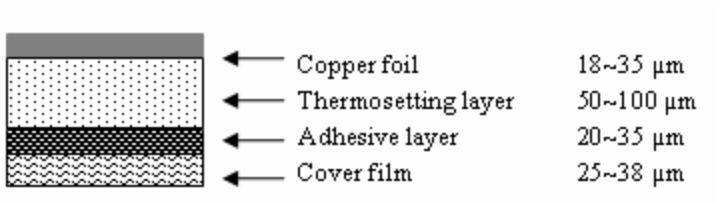


Figure 1 - New Material Structure

Table 1 - General Characteristics of the Board Material

Items	Conditions	Unit	Insulation	Adhesion
Tg	A	°C	140 (DSC)	140 (DSC)
Insulation resistance	C-96/20/65	Ω	1×E14	3×E13
	C-96/20/65 +C-96/40/90		5×E13	1×E13
Dielectric constant	C-96/20/65	-	4.4	4.2
	C-96/20/65 +C-96/40/90		4.4	4.2
Dielectric loss tangent	C-96/20/65	-	0.017	0.03
	C-96/20/65 +C-96/40/90		0.018	0.03
Inner peel strength	A	KN/m	-	0.7-1.0
Copper peel strength	A	KN/m	1.3	-

The Manufacturing Process

An example of the manufacturing process of all-layer IVH mass-pressed multi-layer circuit board is shown in Figure 2, utilizing laser-based via-hole processing and conductive paste printing.

The 4-layer material includes the B-stage adhesive layer protected with the cover film, allowing a standard etching process to be used for circuit pattern formation. Via-holes are processed from the cover film side with a CO_2 laser until reaching the copper surface, thereby leaving blind via-holes, the floors of which are cleaned using a UV laser. The processed blind IVHs are then injected with conductive paste containing metal powder. A normal printing mask can be used for paste injection but may also be omitted because the cover film itself works as a mask as well as adjusting paste height control to the film thickness. The metal paste for printing consists primarily of silver powder or silver-coated copper powder and binder resin, the viscosity of which can be adjusted for printing purposes while providing the electrical characteristics described below.

PWBs made from this material and after press-forming allow normal drilling and through-hole plating as applied to conventional multi-layer boards, thereby enabling a variety of applications. The photographic views of the major parts are shown in Figure 3.

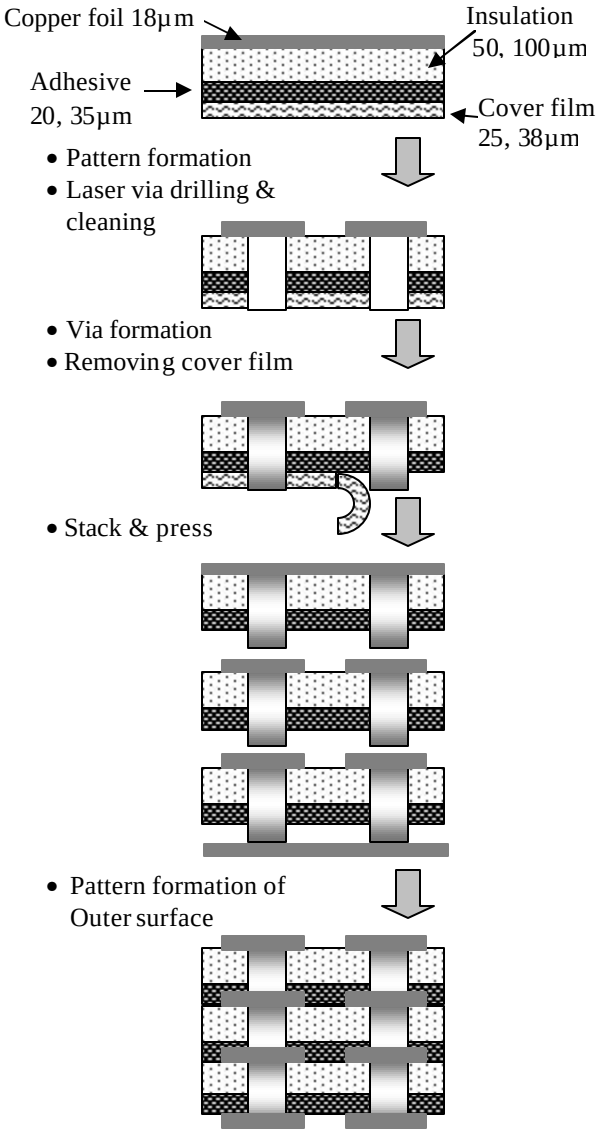
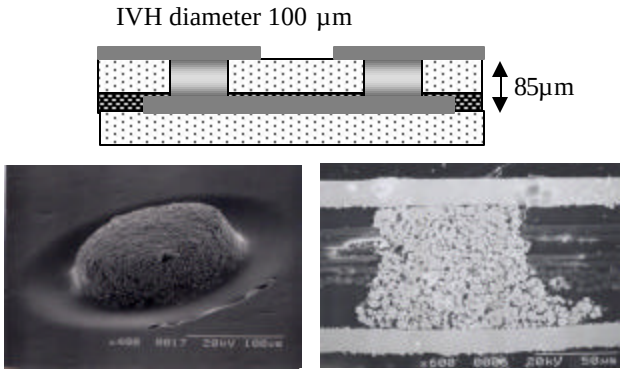


Figure 2 - Manufacturing Process Flow



An IVH filled with paste Cross-section of a formed IVH

Figure 3 - Illustration of an Evaluation Board Used For General Assessment, and SEM Photos of the Major Parts

The next process is to laminate a number of these sheets, each with protruding metal bumps, align them using the pin-laminate method, then press them together to produce a multi-layer printed wiring board with metal-filled via-holes in all layers to ensure conductivity. For the purpose of selecting a matching combination of the developed material and corresponding manufacturing process, a reliability evaluation was performed on a basic structure board to obtain the result shown in Table 2. The result showed that the developed material and the manufacturing process satisfied the required reliability at a level that caused no practical problems. The minimum value of initial continuity resistance was 2.0~3.0 mΩ/via.

Table 2 - Reliability Evaluation Result

Test Item	Test Condition	Target	Judge
TC (Condition B)	-55⇔RT⇔125°C	1000cycle	Pass
High Temp. Storage test	150°C	1000Hr	Pass
Temperature Humidity	85°C 85%	1000Hr	Pass
Oil Dipping Test	RT⇔260°C	100cycle	Pass
THB (Via pitch 300μm)	85°C/85%/50V	1000Hr	Pass

Multi-layer Board Samples

While maintaining the basic board structure, two types of 6-layer board were fabricated by following the process shown in Figure 2. The cross-section photo of an IVH structure is shown in Figure 4. The IVH board gave a resistance value of 2.0~3.0 mΩ/via, similar to the value shown by the evaluation board. It was confirmed that an IVH could easily be made in any number of layers, as shown in the Figure, by using this material. To obtain constant resistance in high multi-layer boards of different types in the future, further efforts are needed to fine-tune the material characteristics to match the conductive paste and the press-forming conditions.

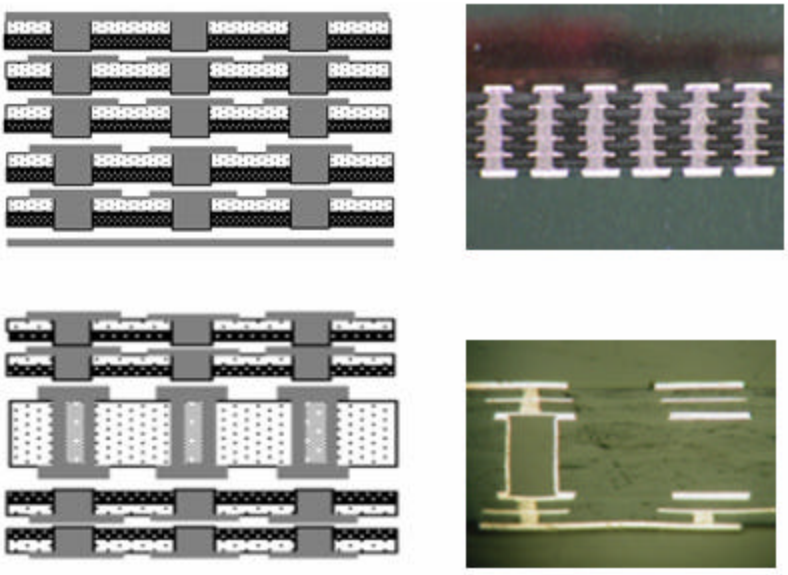


Figure 4 - Cross-Section of a 6-Layer Mass-Pressed Multi-Layer Board

Applications

As one potential application of this material, a 5-layer structure material with double-sided adhesive layers and its process flow are shown in Figure 5, along with its application example in Figure 6. Since this material is based on through-hole IVHs, a conventional drilling process is usable, delivering productivity and cost advantages. In addition, this material does not require a grinding process before circuit-forming, and the dimensional stability of the IVH-equipped double-sided PWB is substantially better than that of previous versions. In contrast to the conventional manufacturing process of IVH-equipped double-sided PWBs, the new process can easily produce a thickness of 100 μm or smaller, very effective in making build-up boards thinner when applied to the core board. The IVH-equipped double-sided PWB is also ideal for CSPs (Chip-Scale Packages), which require a thin substrate for pad-on-hole design to facilitate fine-pattern circuit forming through etching on copper foil.

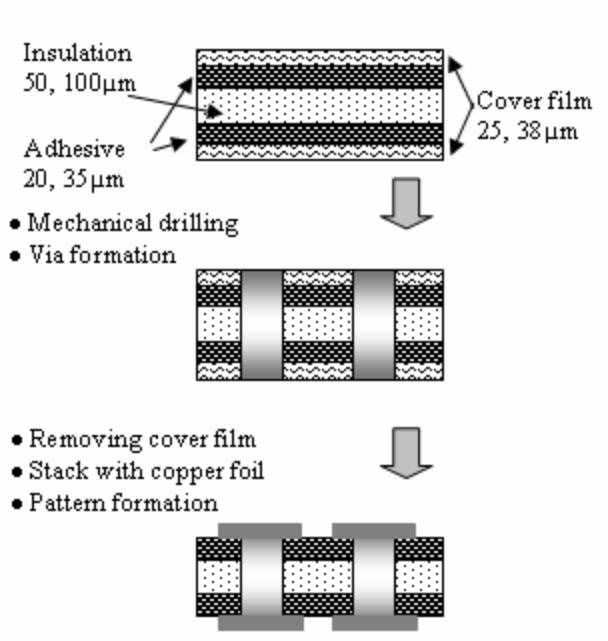


Figure 5 - Unclad Board with Double-Sided Adhesive Layer and Cover Film

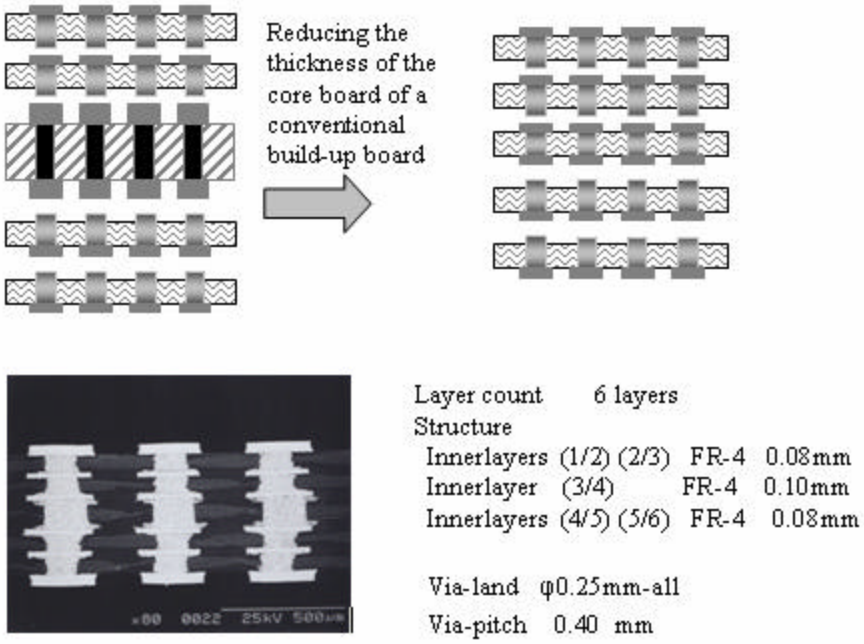


Figure 6 - Example of a Thin Build-Up Board Made By Combining the Two Newly Developed Materials

Summary

The developed all-layer IVH structure and mass-laminated multi-layer board coupled with the corresponding process provide the following advantages over conventional mass-laminated boards.

- A general-purpose four-layer structure and process design are compatible with the conventional PWB processing technology and manufacturing infrastructure.
- The material provides high rigidity and dimensional stability.
- With a minor extension of this technology, IVH-equipped thin-gauge double-sided PWBs can easily be manufactured.

The developed material is expected to provide great benefits to PWB design, manufacturing, packaging and assembly by utilizing the described features. Planned future tasks include accumulation of reliability data and upgrading of multi-layer boards along with research on possible applications.

References

1. Ishihara *et al*.: Build-up Boards for Flip-chip Loading, Electronic Materials, pp35-39, 1996
2. H. Tsukada: Present State and Future Outlook of Build-up Boards – General Theory, Japan Institute of Electronics Packaging, Vol.2, No. 6, pp426-429, 1999
3. Enomoto *et al*.: Mass-lamination High-density Wiring Boards for Achieving Low Cost and High Lamination, PWB-10, The 4th PWB Expo, 2003

Use of Novel Adhesive-lined CCL Material in Single-pressed Multi-layer Circuit Boards with Inner Via-holes in all Layers

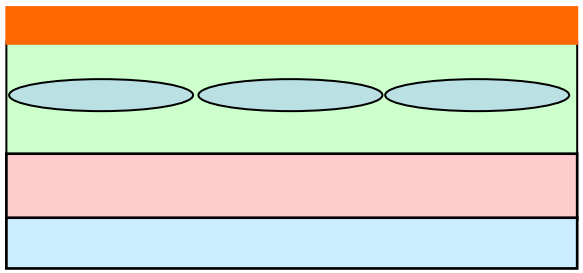
Electronic＆Plastic Materials R&D Center

Daisuke Kanaya

Overview

1. Composition of New CCL
2. Process Flow Chart
3. Technical Concept of New Build-Up PWB
4. General Properties of New CCL
5. Mock-up samples
6. Reliability Data
7. Applications
8. Conclusion

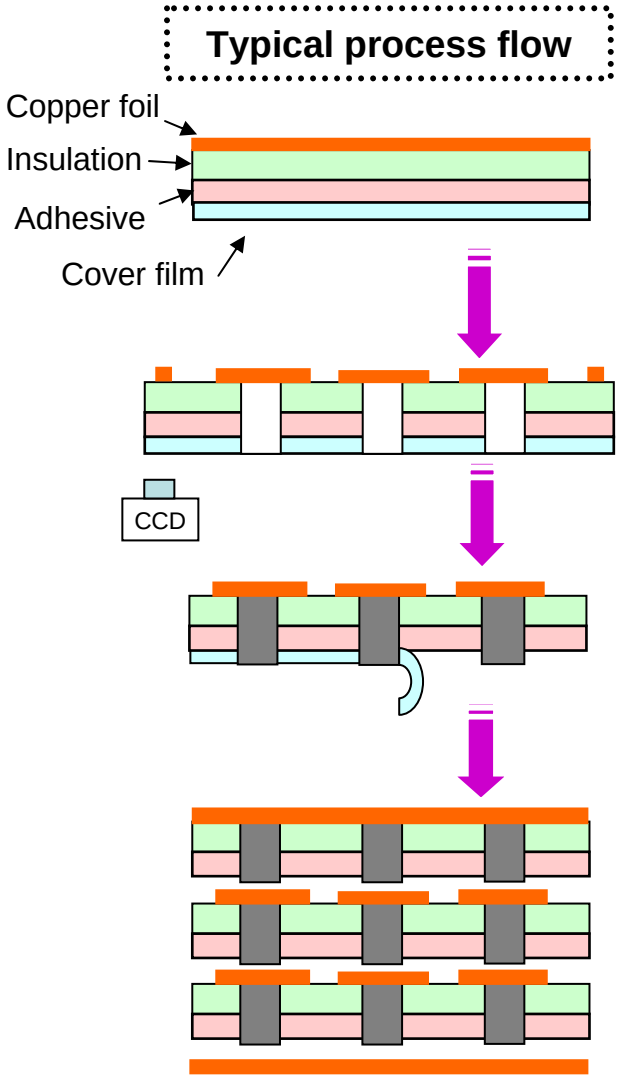
Composition of New CCL



▪ Copper foil	12 to 35μm
▪ Insulation	50 to 100μm
▪ Adhesive	Up to 45μm
▪ Cover film	20 to 40μm

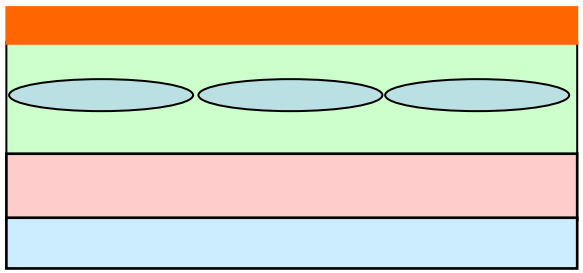
- Copper foil — The copper foil used depends on the application.
- Insulating layer — Can support various requirements for rigidity, thickness, Tg, dielectric constants, etc.
  Laminated substrates **with GC** are basically used.
- Adhesive layer — Can be adjusted to a viscosity that allows the adhesive layer to be **laminated simultaneously** with a conductive paste, etc.
- Cover film — **Protects** the adhesive layer when processed for etching, etc.
  Contributes to securing **an even bump height**.

Process Flow Chart



Process	Functions and features
Copper foil surface roughening	**Roughening to improve the adhesiveness**
Circuit forming	The cover film protects the adhesive layer. Can be used in the regular cupric chloride etching process.
Laser process	Can process the PWB being fitted with the protective film using carbon dioxide laser gas. The laser processed section can be identified by looking through the circuit.
Hole cleaning	A dry type (UV laser, etc.) can be used.
Paste printing	Select from various metallic pastes.
Cover peeling	Even-height bumps can be provided.
Mounting capability	Lamination The dimensional changes are at the same level as conventional laminates with GC. GC helps stabilize mounting.

Composition of New CCL



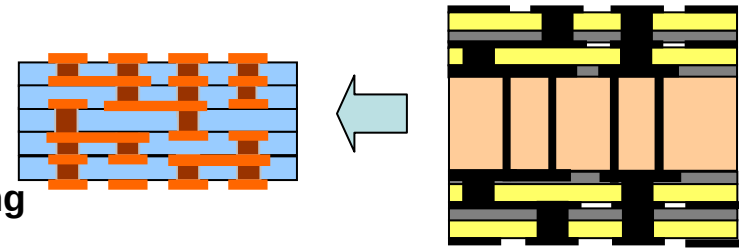
▪ Copper foil	12 to 35μm
▪ Insulation	50 to 100μm
▪ Adhesive	Up to 45μm
▪ Cover film	20 to 40μm

- Copper foil — The copper foil used depends on the application.
- Insulating layer — Can support various requirements for rigidity, thickness, Tg, dielectric constants, etc.
  Laminated substrates **with GC** are basically used.
- Adhesive layer — Can be adjusted to a viscosity that allows the adhesive layer to be **laminated simultaneously** with a conductive paste, etc.
- Cover film — **Protects** the adhesive layer when processed for etching, etc.
  Contributes to securing **an even bump height**.

Development concept for new materials and corresponding process (Solμv)

Trend requirements

- All-layer small-diameter IVH structure board
- Stacked via structure
- Realization of both thin-film insulating layer and mounting capability



Solution for micro Via substrate material

Development concept

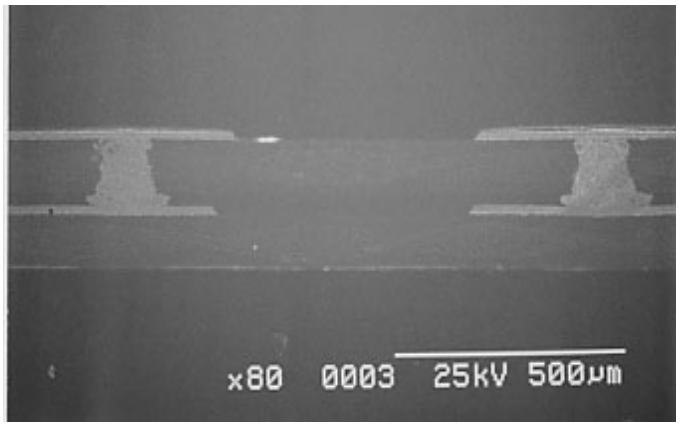
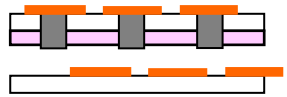
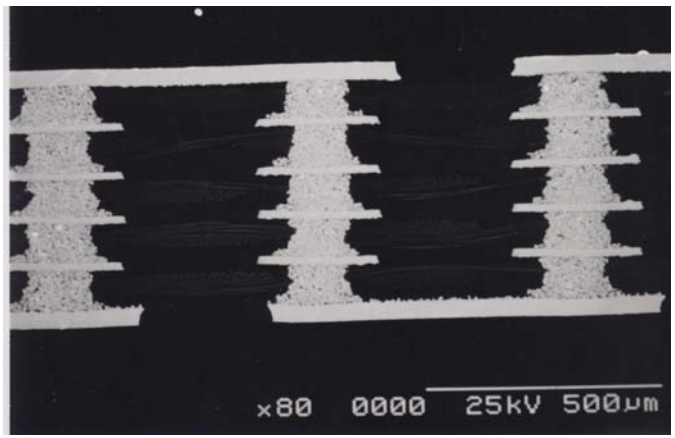
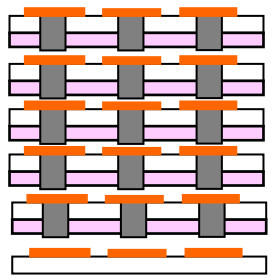
New materials and related processes have been developed.

- Contribute to the design through all-layer IVH/stacked via hole boards
- Have a positional accuracy advantage through direct via hole processing on boards.
- Have advantages for circuit miniaturization.
- Improvement of the yield and the reduction of the lead time through mass-pressed multi-layer processes

Performance example of mass-pressed multi-layer wiring board materials

Item	Process condition	Unit	Insulating layer	Adhesive layer (35 μm)
Tg	A	°C	140 (DMA)	140 (DMA)
Insulation resistance	C-96/20/65	Ω	1 ×E13	1×E12
	C-96/20/65 +C-96/40/90		5×E12	1×E12
Dielectric constant	C-96/20/65	—	4.4 (at.1GHz)	4.4 (at.1GHz)
	C-96/20/65 +D-24/23		4.4	4.4
Dielectric dissipation factor	C-96/20/65	—	0.017	0.03
	C-96/20/65 +D-24/23		0.018	0.03
Inner layer peel strength	A	KN/m	——	0.7～1.0
Copper foil peel strength	A 18 μm	KN/m	1.3	——

Sample model of buildup board

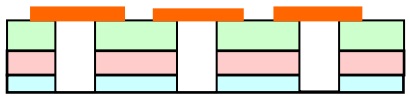
Layer	Cross section	Construction	Remarks
2 layers		 Copper foil 18 µm Insulating layer 80 µm Adhesive layer 25 µm	Via resistance **3.2mΩ/via**
6 layers		 Copper foil 18 µm Insulating layer 60 µm Adhesive layer 25 µm	Via resistance **3.0mΩ/via**

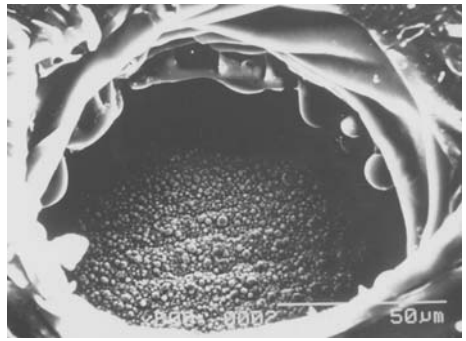
Photos of the Sample in each Process

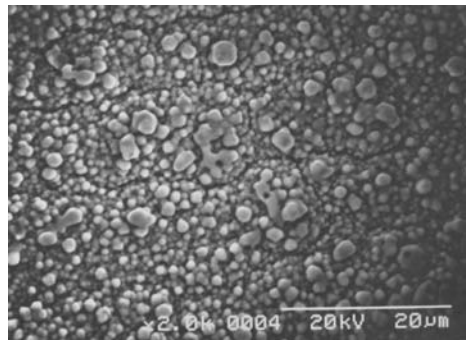
[Via hole laser processing]

CO_2 2.30mj/S 4 shots 100Hz

UV 0.12mj/S 30 shots5000Hz



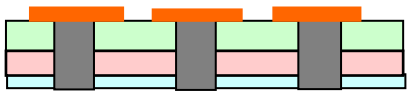


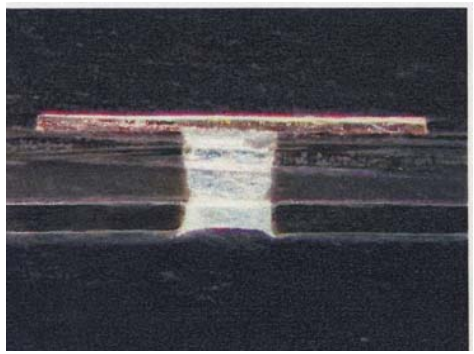


[Printing of conductive paste]

Vacuum printing

about 2 to 3 shots



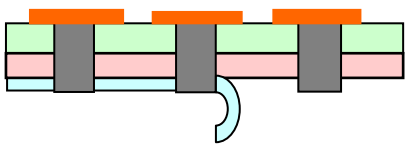


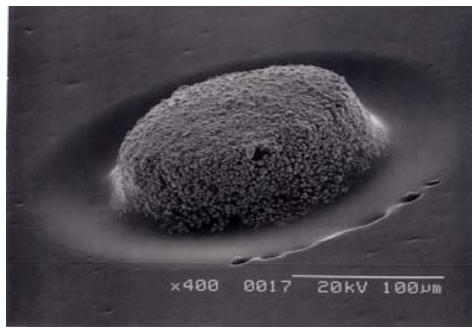
Types of conductive pastes

Paste consisting of silver-coated copper powder and epoxy resin

[Peeling of cover film]

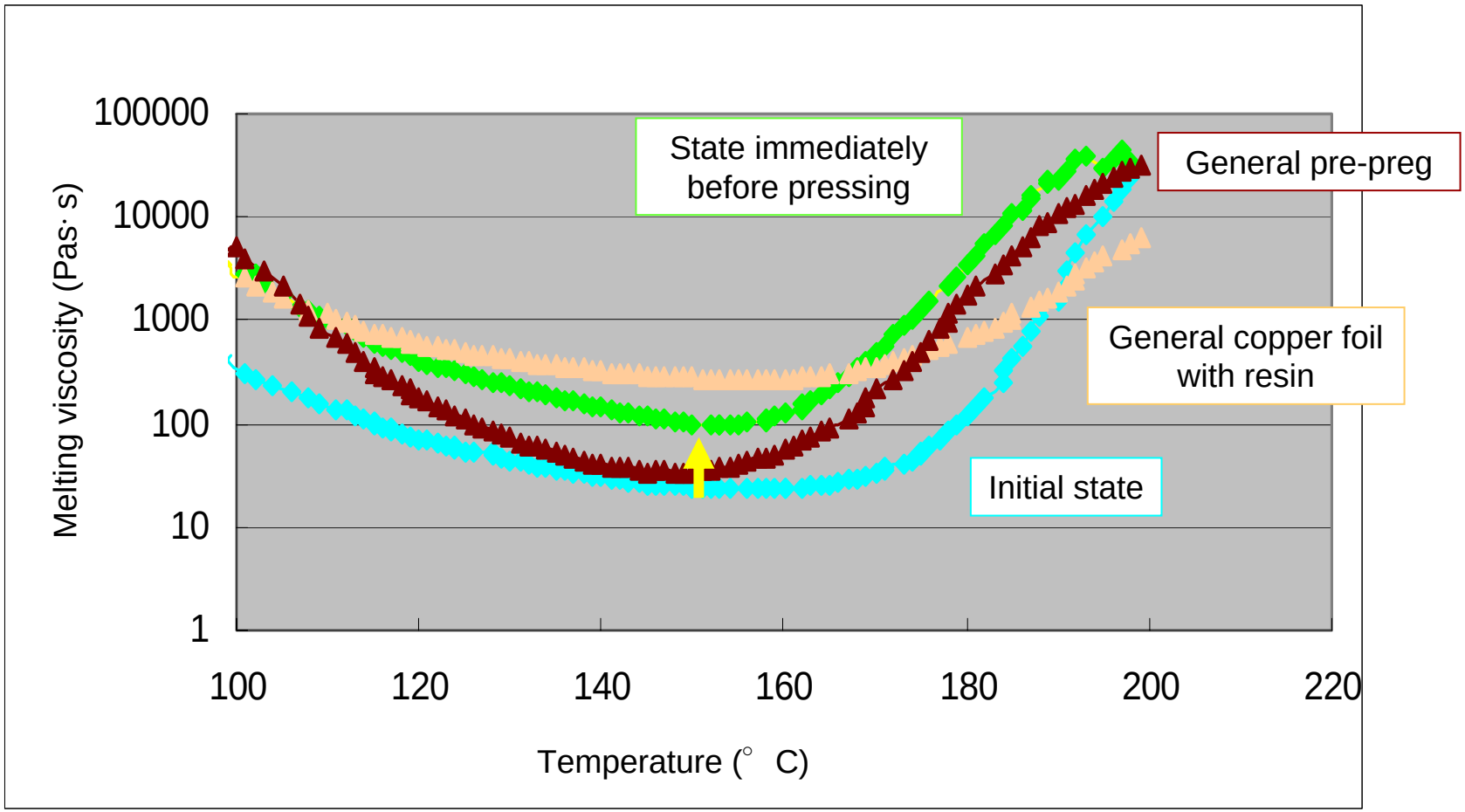
Heating for provisional curing of bumps





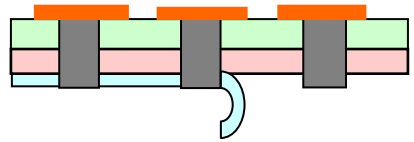
Pre-drying process for hardening the paste head

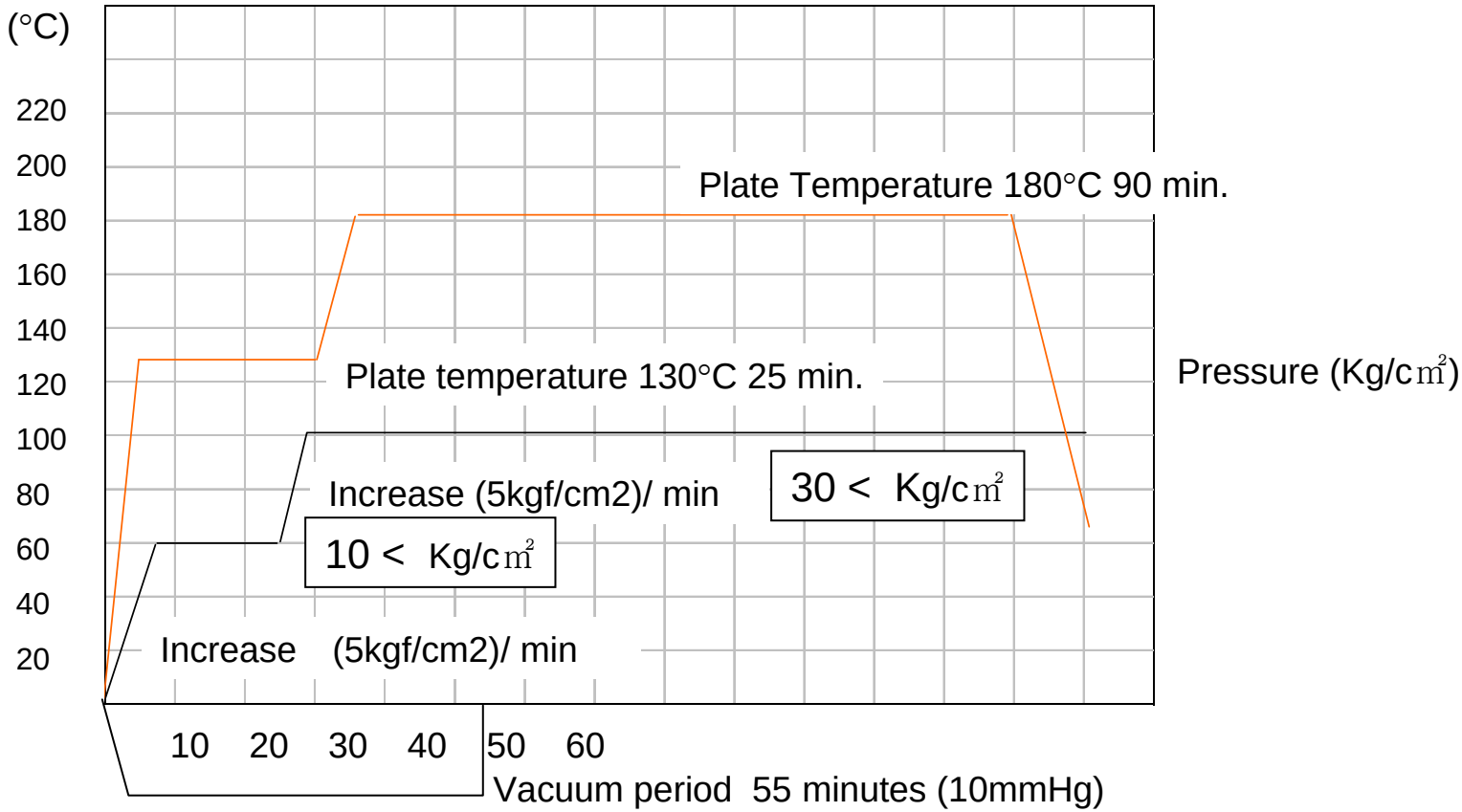
Melting viscosity behavior of the adhesive layer



Vacuum Press Process Condition

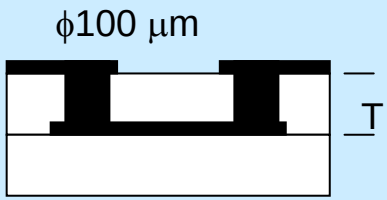
- Pre-heathing 100°C /30 to 60 minutes
  Selective curing of paste head section
- After the layers are laminated,
  the mass-press process is carried out.





Results of the continuous operation reliability evaluation of a two-layer board

Evaluated model **Type A**



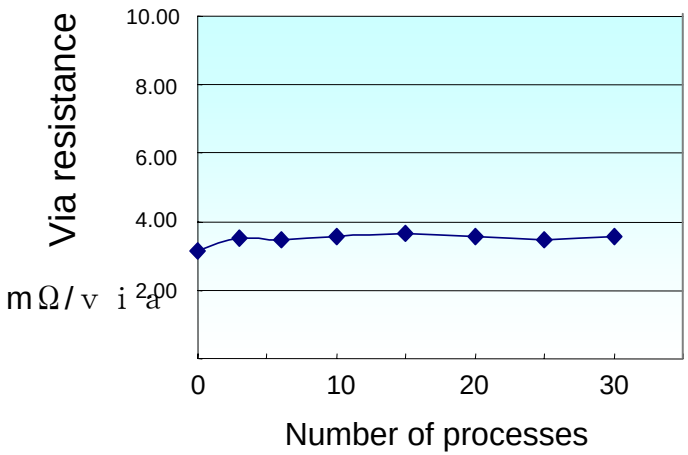
Initial resistance

3.24 mΩ/via
（3136via/chain）

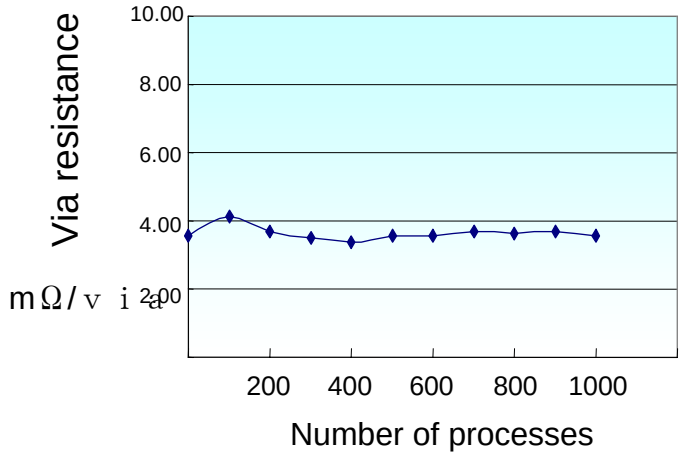
2 layers PWB

Test Item	Test Condition	Target	Result
Oil dip test	RT⇔260°C	30 cycle	Pass
Temperature cycle test	-55⇔RT⇔125°C	1000 cycle	Pass

Results of oil dip test

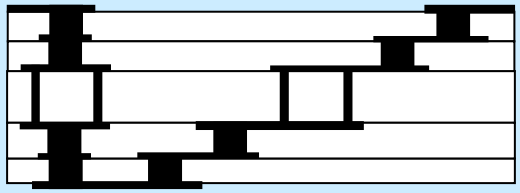


Results of temperature cycle test



Results of the continuous operation reliability evaluation of a six-layer board

Type B



Layer thickness (1/2)(2/3) 0.08 mm

Layer thickness (3/4) 0.60mm

Layer thickness (4/5)(5/6) 0.08 mm

Initial resistance

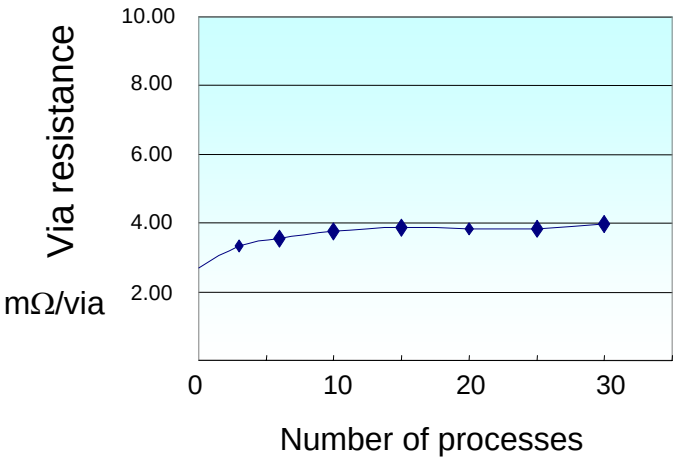
2.00～2.50 mΩ/via

6 layers PW B

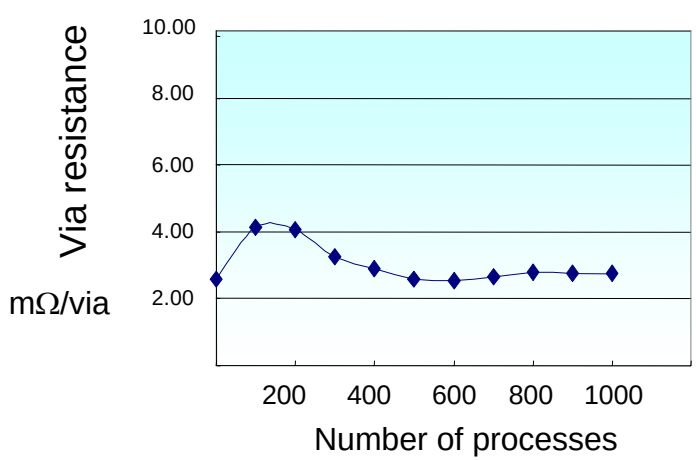
(240via/chain)

Test Item	Test Condition	Target	Evaluation
Oil dip test	RT⇔260°C	30 cycle	Pass
Temperature cycle test	-55⇔RT⇔125°C	1000 cycle	Pass

Results of oil dip test

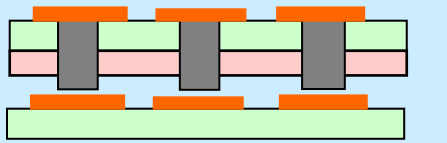


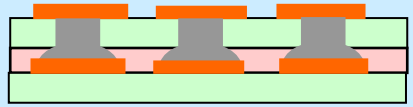
Results of temperature cycle test



Sample structure for insulation test

Via wall to via wall insulation evaluation





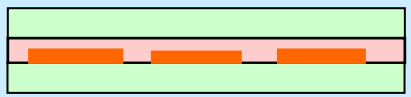
200μm

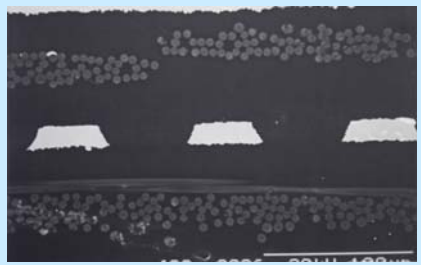
Evaluated specifications

Via pitch
250 300 350μm

Via land: 200μm
Via diameter: 100 to 150μm

Circuit to circuit insulation evaluation





100μm

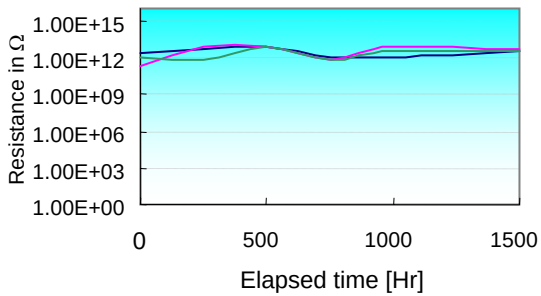
Evaluated specifications
L/S 50/50 65/65
75/75μm

Results of insulation test

Test conditions: 85° C, 85%, 50 V DC

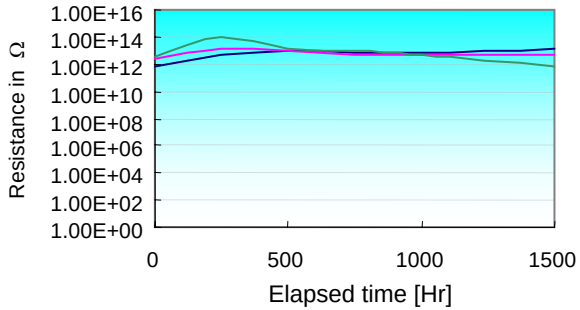
L1-2 Via-Via

-- 250 -- 300 -- 350μm



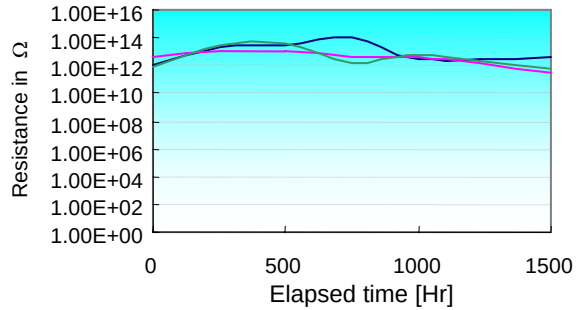
L2-3 Via-Via

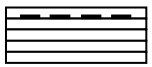
-- 250 -- 300 -- 350μm



L3-4 Via-Via

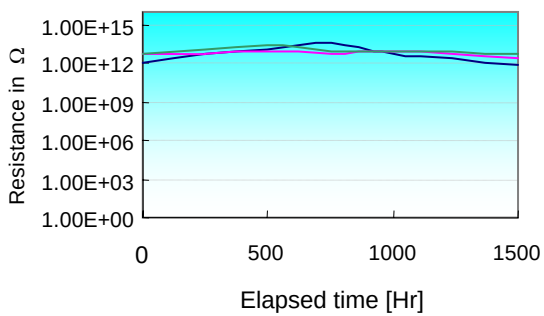
-- 250 -- 300 -- 350μm

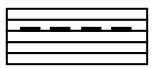




L1-2 L/S

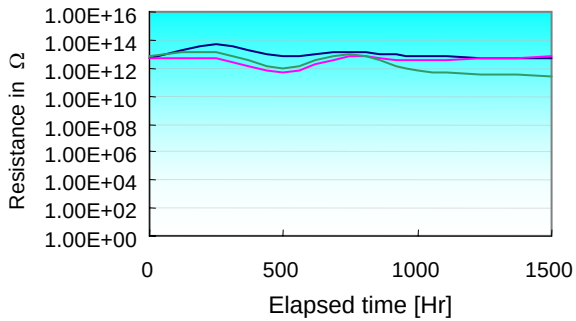
-- 50/50 -- 65/65 -- 75/75





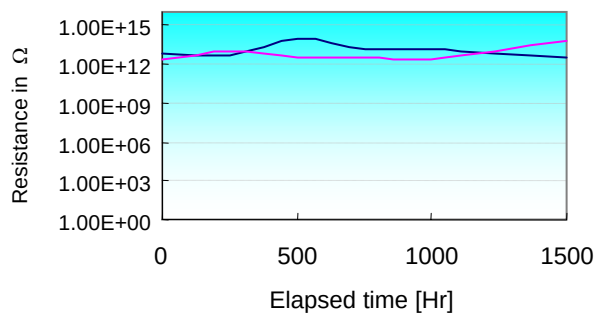
L2-3 L/S

-- 50/50 -- 65/65 -- 75/75



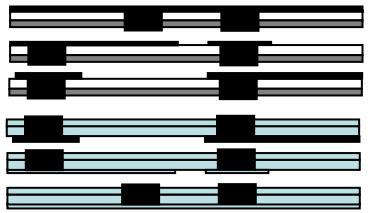
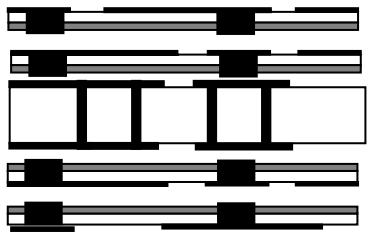
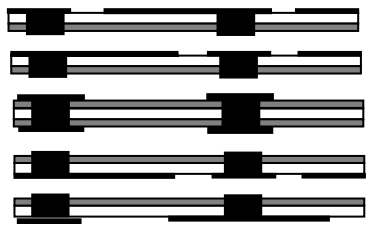
Inter-layer resistance 100 mm

-- L1/L2 -- L2/3



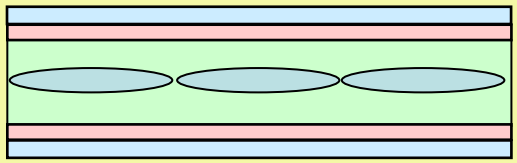
Criteria : Insulation reliability R>1.0E8

Examples of applications for build-up printed wiring boards

Type of boards facing each other 	***Thin core board type*** 
Type of build-up onto core boards 	***Type of build-up onto thin core boards*** 

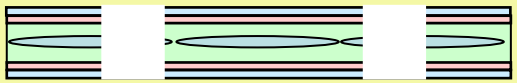
Proposal for thin core boards

Materials with a double-sided adhesive layer

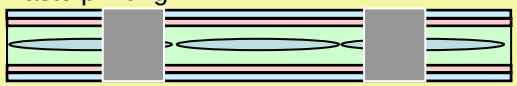


Cover film
Adhesive layer
Insulating layer
Adhesive layer
Cover film

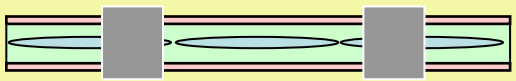
Drilling



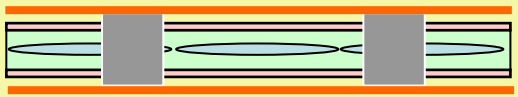
Paste printing

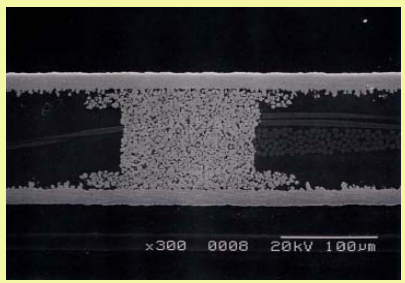


Cover peeling

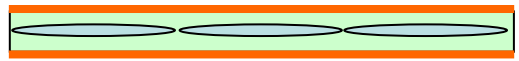


Press (copper foil is used.)





Engineering method using conventional CCL



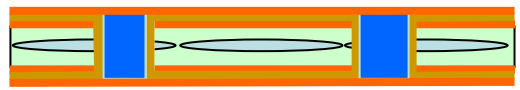
Drilling

Through-hole plating

Ink hole filling (non-conductive ink)

Ink projection grinding

Cover plating

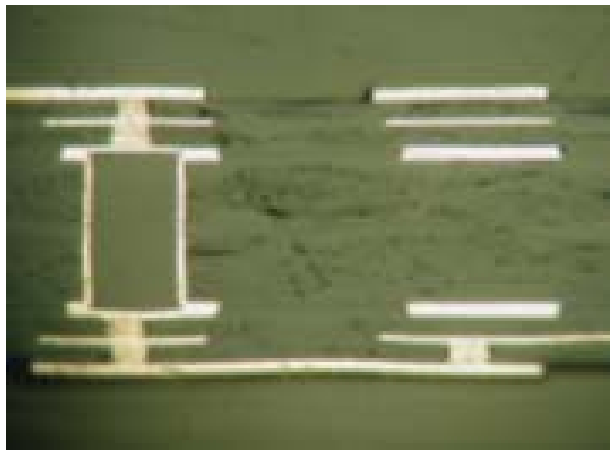
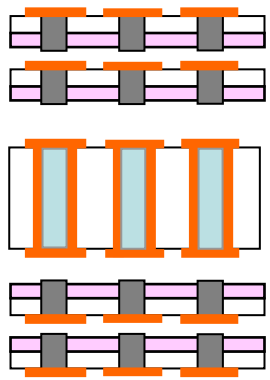
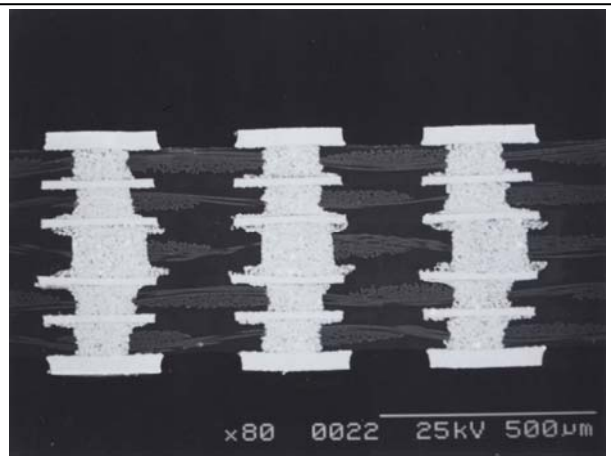
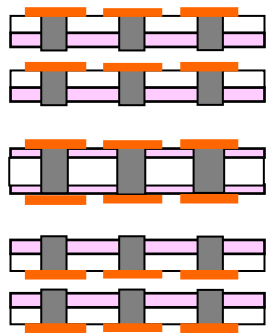


↓Circuit forming

1.Several plating operations are necessary and it is difficult to form fine patterns.

2.Due to the ink projection grinding for removal, thin boards cannot be processed. (It is difficult to eliminate dimensional changes.)

Examples of build-up boards using thin core boards

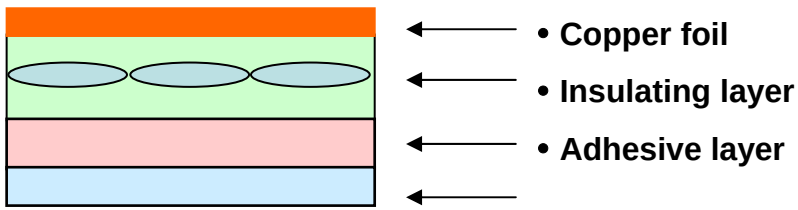
Layer	Cross section	Construction	Remarks
6 layers			Via resistance **3.2mΩ/via**
6 layers			Via resistance **3.0mΩ/via.**

Summary

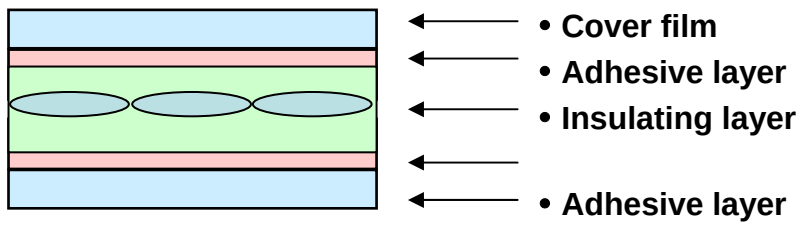
1. New mass-pressed multi-layer printed wiring board materials supporting the all-layer IVH structure and related process (Sol μ V) have been developed.
2. The advantages of using these materials are as follows:
   - Offers solutions with micro-via holes for greater via hole processing accuracy, fine circuits, etc.
   - General-purpose manufacturing processes using conventional manufacturing technologies and infrastructure can be applied.
   - The insulating layer containing glass cloth provides rigidity surpassing that of the RCC and the conventional mountability.
3. Proposal of insulating materials fitted with an adhesive layer on both sides for application deployment
   - It is possible to study the deployment into double-sided boards with IVH, build-up core boards, etc.

"New mass-pressed multi-layer printed wiring board materials" supporting all-layer IVH structure

Specifications supporting build-up sections



Specifications supporting core sections



Thank you very much.

dkanaya@den.mew.co.jp

END