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Next Generation High Density Build-Up PKG Substrate

Takashi Shuto, Kenji Takano, Kazuya Arai, Munekazu Shibata
Junichi Kanai and Kaoru Sugimoto
Fujitsu Interconnect Technologies Limited
Kitaowaribe, Nagano, Japan

Abstract
In recent years, along with the further progress of network systems, mobile communication systems and high performance servers printed wiring boards (PWBs), which are key components in these products, are increasing in importance, and are required for technology innovation.

Especially, the substrates in the field of high-end ASICs require more high density and high performance, and CSP and Module substrates in the field of mobile application require more high density and downsizing. The demands for the substrate have been steadily becoming more and more stringent.

This paper introduces a new multi-layer PKG substrate that has been developed to meet these market trends, and has better features than the conventional build-up substrate. This new multi layer PKG substrate has no core material and is a so-called coreless structure composed of only high-density build-up layers. This substrate is produced with our original manufacturing process and has the following features: 1) Light weight (70% reduction), Thin-thickness (less than half), and High density 2) High reliability 3) Good productivity 4) Green material.

Introduction

Device Road Map

As shown in Figure 1, the clock frequency and the number of pins per package keeps increasing every year. The pin counts per a package will increase by about 15% per year, and it will exceed 3,000 pins in 2005 and 4,000 in 2007 in the field of high performance. Also the bump pitch will become finer by about 6% per year with the increasing pin count. In 2004 the required bump pitch is less than 150 um and will be less than 130 um in 2005 in the field of high performance.

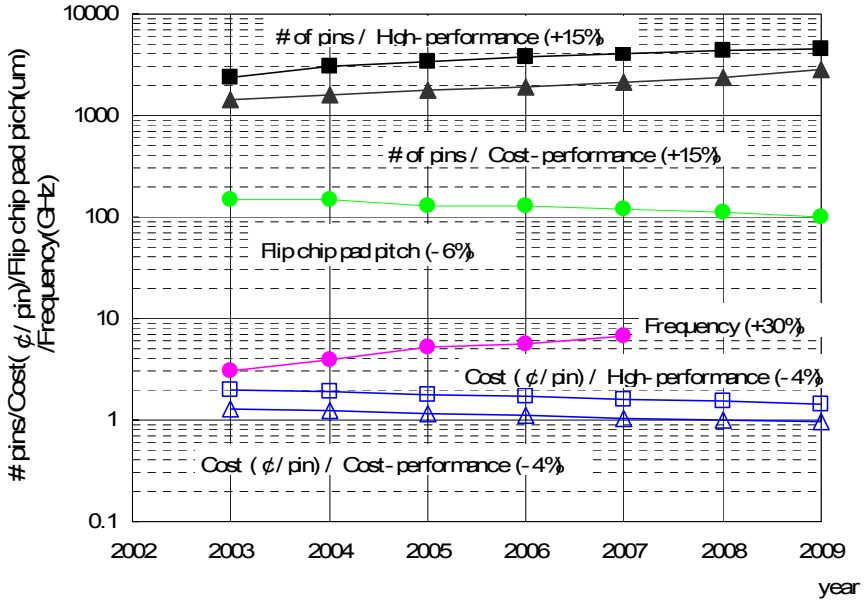


Figure 1 - Packaging Road Map by ITRS 2003 Process Flow

Needless to say, packaging cost reduction is required. In 2004 the required packaging cost is less than 1.9cents/pin in the field of high performance. Moreover, the electrical characteristics requirements for packages for GHz devices will become higher such as: tighter Z0 control, lower cross-talk noise, lower DC/AC resistance, and especially lower Power-Ground (hereafter: VG) impedance for high power chips.

Requirements for PKG Substrate

As above-mentioned, high-performance and cost-performance field have common two trends, high density interconnection and high speed. For Semiconductor PKG substrate high density and thin substrate becomes a common requirement for both the high-performance and cost-performance area. For the high-performance area, a thin substrate is required in addition to high density in order to reduce VG inductance for high frequency. The cost-performance area requires high density and thin substrates for downsizing purposes, e.g. stacked CSP for an example. In addition to these functional improvements, improving materials to meet environmental concerns is necessary. Nowadays many companies have big concerns about environment issues. So electronics the equipment industry has to use green materials. The industry needs to use Pb free and halogen free materials for the PKG substrate.

The next generation high-density build-up PKG substrate, which is manufactured by our newly developed process, can meet these requirements. Figure 2 shows the advantages of the next generation high-density build-up PKG substrate. This new multi layer PKG substrate has no core material and is a so-called coreless structure composed of only high-density build-up layers. And this substrate has the following features: 1) Light weight, Thin-thickness, and High density 2) High reliability 3) Good productivity 4) Green material. This paper introduces the features of the next generation high-density build-up PKG substrate and the new manufacturing process.

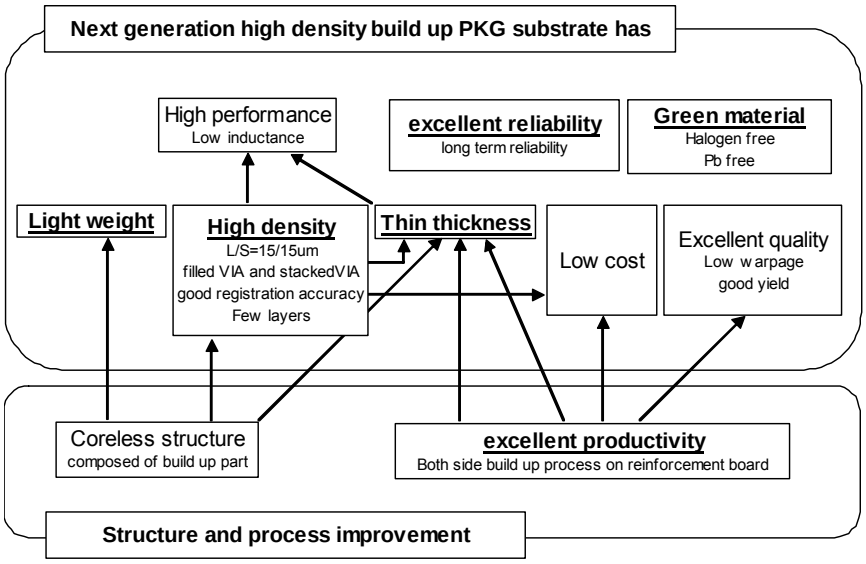


Figure 2 - Advantage of Next Generation High Density Build up PKG Substrate

Advantages of New Substrate and Manufacturing Process

Conventional Manufacturing Process

Current PKG substrate is mainly divided into two parts: core layer and build-up layer. As you can see in Figure 3, core layer is thick and its volume is more than half of a substrate. On the other hand, the build-up layer is thin and high density. Generally the core layer is 2 to 4 layer, 400um to 800um thickness of reinforced epoxy which has 120um to 300um diameters via hole made by mechanical drilling. Patterning is made by the subtractive process. On the other hand the build-up layers are structured by a 30 to 50um thickness dielectric layer and 50 to 100um diameter micro via by laser drilling for layer connection. Patterning is made by the subtractive process or semi-additive process.

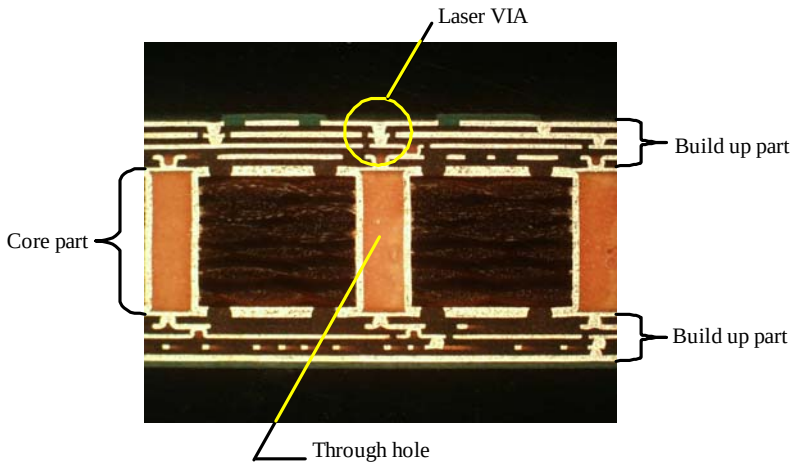


Figure 3 - Cross Sectional Micrograph of Conventional PKG Substrate

The New Manufacturing Process

The new developed process can manufacture the high density and thin thickness substrate efficiently. As in Figure 4 it starts from a reinforced board and then A) patterning on both sides of the reinforcement board B) build-up C) removal D) surface finish.

The new process has a feature that can make an odd number of layer substrate such as 3L, 5L, and 7L. Manufacturing efficiency of the new process improved 2 times compared with the current process since it has put products on both sides of the reinforcement board. And because of the high-density substrate the number of layer can be reduced. Therefore, this new process is more applicable for low cost production.

Start and the First Patterning

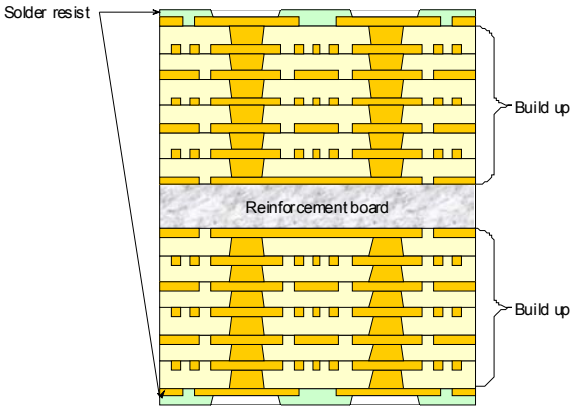
Form a first pattern on both sides of stiff reinforcement board whose thickness is approximately 0.4mm. The patterning shall be done by a subtractive process or semi-additive process.

Build Up and Solder Resist

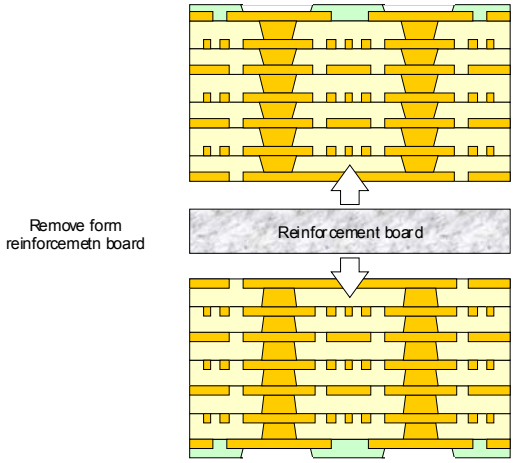
Form a dielectric layer on both sides of patterned reinforcement board and make vias for interlayer connection by CO2 laser or UV-YAG laser. After making the vias, make patterning by a semi-additive process (electro-less Cu plating, plating resist and electrolytic pattern Cu plating) on the reinforcement board. Repeat these steps until getting the desired structure (layers) then put solder resist on it. In this process it was confirmed that a much smaller diameter via by using UV-YAG laser, L/S=15/15um and multi stacking by fill plating can be made with the same condition/ yield as current process. Glass-cross impregnated prepreg is usual for an insulating material. Also the application of other low dissipation factor materials such as PPE, PTFE, and liquid crystal polymer, for further improvement of electric performance is expected.

A) Start and the first patterning.

B) Build up and Solder resist.



C) Remove form reinforcement board.



D) Back side solder resist and Ni/Au plating, pre-solder.

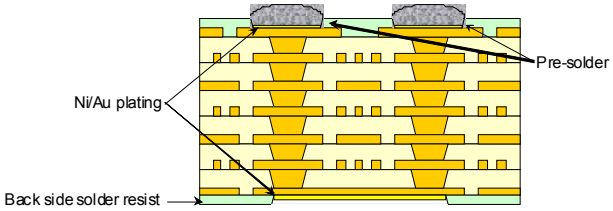


Figure 4 - Fabrication Process Flow

Remove Form Reinforcement Board
The build-up parts are detached from both sides of the reinforcement board after build-up and solder resist process.

Back Side Solder Resist and Ni/Au Plating, Pre-Solder
Form solder resist on backside of build-up part and then put surface finish on the surface of the board. Surface finish can be electroless Ni/Au plating or direct Au plating, solder coat with eutectic or lead-free solder and so on.

Advantage of the New PKG Substrate
High Density Interconnection
Build-up layer has an advantage of high density over the core layer, e.g. L/S=15/15um level, 30 to 50um diameter via made

by UV-YAG laser, 2 or 3 stacked via realized by filled via technology. For the core layer, on the other hand, the trend of getting high density is much slower compared to build-up layer. Also there are couple of additional issues such as the necessity for special equipment for smaller drill holes, manufacturability changes due to materials and difficulty in through hole plating/ plugging.

Our new PKG substrate is a coreless structure which is composed of only high-density build-up layers and these features are available for high-density specification

Thin Thickness

The key to make thin thickness substrate is how to make core, which occupies more than half the volume, thinner. Currently, very thin core material with 30~50um thickness has been developed. However, special equipment is necessary to make build-up structure on such thin base material. In addition, there are a lot of problems needing to be solved in quality and manufacturability such as dimensional stability and distortion of substrate due to heat treatment processes. These are challenges that seem very difficult to solve.

Therefore, this manufacturing technology was developed: repeat multiple build-up process by the conventional method on top and back side of the reinforcement board and after removing the reinforcement board, conduct the surface treatment. This technology has excellent manufacturability, and can fabricate higher density substrates without changing current mass production equipment

For High Speed and High Frequency

For higher-speed and higher-frequency application, the existence of core has been an obstacle to shorter wiring distances and to reducing inductance. In build-up layers, multiple stack-up with filled via-holes is preferable since it can give a shortened wiring distance. This stack-up method contributes to high-density (see Figure 5, “a” can be narrower) and is also known for having effect on low VIA inductance.

The next-generation high-density PKG substrate is the optimum structure to solve these issues for high-speed and high frequency. In addition, this thin substrate fabricated with coreless and full-stacked technology is effective on low inductance.

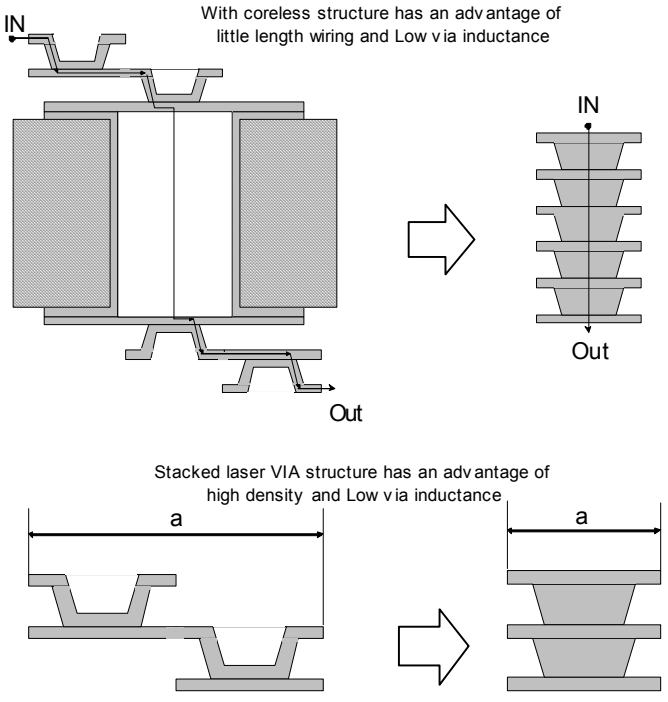


Figure 5 - Desirable Structure for High Speed and High Frequency

Others
The coreless structure and full-stacked via formation technology provides the same design rules in all layers, which has advantages of simplifying wiring in the design phase. And this also provides effective alternatives to “Thermal vias” to radiate heat by increasing copper volume which has a good thermal conductivity.

Proto Type Result of Reliability Test
We fabricated the following 3 types of proto type substrates based on above-mentioned manufacturing process, and verified each effect. These proto type substrates have epoxy-based dielectric material which features halogen-free materials and low thermal expansion. Material properties are shown in Table 1. Dielectric resin was laminated by a vacuum-laminating machine. The patterning was conducted through a semi-additive process, and a CO_2 laser was used for via formation of interlayer connection.

Table 1 - Mechanical Properties of Dielectric Resin

	Conventional	Halogen free material
CTE	70ppm	46ppm
Young's Modulus	3.0GPa	4.0GPa
Tg (TMA)	170deg.C	156deg.C
note	-	Halogen free

Proto Type-1 (CSP & Module Type)
For mobile device applications such as mobile phones and digital cameras, substrates are strongly encouraged to use green material in addition to high-density and thin thickness requirements. Halogen-free dielectric material is used to fabricate 4 and 6 layers substrates.

The reliability is evaluated through long-term reliability tests. This proto type substrate features fine lines with a minimum of L/S=25/22.5um made by a semi-additive process, small via-holes of 60-80um made by CO_2 laser, 20um pattern thickness, and 30um dielectric thickness. Figure 6 shows that thin thickness substrates such as 4 layered 220um and 6 layered 320um can be fabricated. Reliability of this proto type substrate was confirmed by the following long-term reliability tests; Reflow stress, T/C, Oil dip, HTS and USPCBT. Results are shown in Table 2.

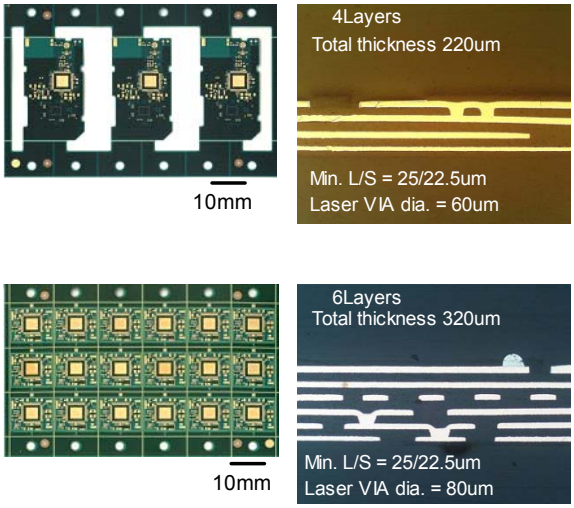


Figure 6 - Sample of Our New LSI PKG Substrate (CSP & Module Type)

Table 2 - Results of Long-Term Reliability Tests (CSP & Module Type)

	Condition	Result		Comments
Reflow stress	260degC	7times Pass	n = 15	–
T/C	-65degC ~ 125degC	1000cyc. Pass	n = 15	JEDEC Level-3
Oil dip	260degC/5sec ~ 20degC/20sec 20cyc.	80cyc. Pass	n = 10	JEDEC Level-3
USPCBT	120degC/85% DC3V	264hrs. Pass	n = 15	JEDEC Level-3
HTS	150degC	1000cyc. Pass	n = 15	JEDEC Level-3

Proto Type-2-1 (Flip-Chip Type)
High density is a common requirement for flip-chip type substrates. We took a design for our current production part (fabricated by conventional process) and converted to this newly developed manufacturing process to see how it can be improved. (See Figure 7)

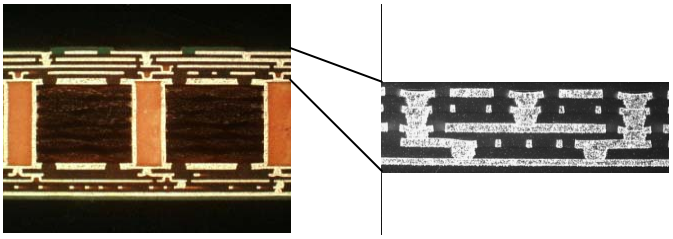


Figure 7 - Sample of Our New LSI PKG Substrate (GigaModule-4)

Halogen-free materials are used for solder resist and dielectric, and Sn/Pb as the pre-solder to fabricate this proto type.

This proto type has fine lines with a minimum of L/S=20/20um made by a semi-additive process. It was fabricated by the specification which contains 3 stacked small via-holes made by a CO2 laser, 20um pattern thickness, and 30um dielectric thickness. With this process, getting rid of core layers makes it possible to reduce the numbers of the layer from 10 to 5, the thickness of PWB reduced to 20%, from 1300um to 270um and the weight is reduced to approximately 36%. (Table 3)

Table 3 - Specification of Each Sample

		Conventional PKG substrate	Proto type
Core layer	Core thickness	600um	—
	Drill diameter	200um	—
	Line/Space	50/50um	—
	Pattern thickness	30um	30um
Build up layer	Laser VIA diameter	60um	60um
	Dielectric thickness	30um	30um
	Line/Space	25/25um	20/20um
	Pattern thickness	20um	20um
	Numbers of stacked VIA	2 max	3 max
Substrate	Numbers of layer	10(4-2-4)	5
	Total thickness	1300um	270um
	Weight	6.4g	1.8g

Proto Type-2-2 (Flip-Chip Type)
Flip-chip type has the key requirement for high speed in addition to high-density, as already stated, to reduce VG inductance. In order to achieve this, an effective solution is to make a thinner thickness with fine-pitch and full-stacked via-holes. With a 7 layer proto type which is structured with full-stacked via-holes on every VG layers (see Figure 8); reliability was tested and the results were checked on a following list as well as the connectivity of full-stacked via-holes. Halogen-free materials are applied as solder resist and insulation of build-up material, and lead-free solder (Sn/Ag) as pre-solder to fabricate this proto type.

The substrate also features of: 20um pattern thickness, 30um dielectric thickness, total thickness of 370um, L/S=20/20um, small via-holes of 60um to make 6 full-stacked via-holes on VG layers, 3 stacked via-holes on signal layers. High reliability of this proto type substrate made of halogen-free materials was confirmed in long-term reliability tests shown in Table 4.

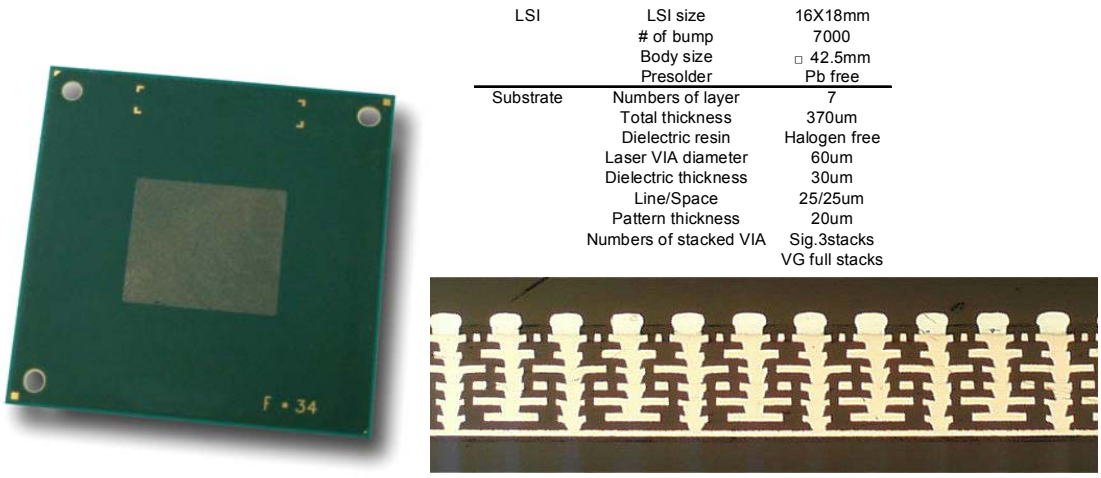


Figure 8 - Sample of Our New LSI PKG Substrate (GigaModule-4)

Table 4 - Results of Long-Term Reliability Tests (Flip-chip type)

	Condition	Result		Comments
Reflow stress	260degC	7times Pass	n = 15	_
T/C	-65degC ~ 125degC	1000cyc. Pass	n = 15	JEDEC Level-3
USPCBT	120degC/85% DC3V	264hrs. Pass	n = 15	JEDEC Level-3
HTS	150degC	1000cyc. Pass	n = 15	JEDEC Level-3

Figure 9 shows a flip-chip connection which is mounted on the substrate (Figure 8). It's the results of connection reliability are shown in Table 5.

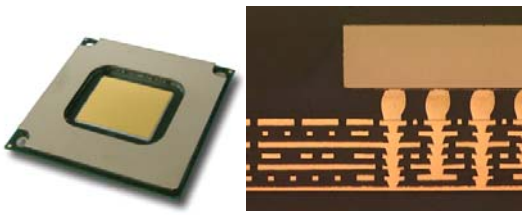


Figure 9 - Sample of LSI Assembled PKG

Table 5 - Results of Long-Term Reliability Test with LSI Assembled Sample

	Condition	Result	
Reflow stress	218degC	4times Pass	n = 18
T/S	-40degC ~ 125degC	250cyc. Pass	n = 18

Future Work

It will be necessary to verify the electrical characteristics of this PKG substrate and review its application with low-k [low dielectric constant] material to make it suitable for further speeding up. It will also be necessary to investigate making it a low-thermal expansion product and a low-stress product for low-k chip and large die.

Summary

LSI PKG substrate is used for high-performance ASIC, CSP and SIP. It is required that the material be high-density, thin and a green material for application with LSI where higher-pin-count and high speed are needed. We have developed a high-density build-up substrate as the next-generation technology. It has the following advantages: 1) the full-stacked via hole structure without core layers, makes substrates light, with thin thickness, and high-density 2) high reliability when testing with long-term reliability tests 3) fabricating is efficient for thin thickness and high-density when using only build-up layers 4) in addition, is uses halogen-free dielectric materials and Pb free pre-solder that are suitable for environmental issues.

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