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The European Roadmap

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Abstract
A unified European roadmap for PWBs does not exist today. It is also most unlikely that a unified roadmap will available in a foreseeable future time. However, the EIPC has worked together with many European companies and association to define trends in technology based on the future needs of the industry. This paper will report on some of the trends that are included in European company roadmaps and the HotCar project. More details have been documented in the European Technology and Trend Report that has been put together by the German GMM VDE/VDI, the DGO, FED, ZVEI, the EITI as well as the European Institute of Printed Circuit Boards. Leading companies involved in design of electronic equipment supported this report. Also PCB fabricators, PCB assemblers as well as materials suppliers for PWBs and companies that develop latest fabrication methods used to manufacture state-of-the-art electronic equipment. This paper will provide a snap shot on developments that will impact the European Roadmap for PCBs and will help to guide electronic engineers to select the new PCB technologies for advanced electronic devices.

Overview
The paper will contain the following elements:
- Objective of the paper
- Introduction
- Hot Car Project
- Trend to Higher Data Transmission Rates
- Materials
- Additional Materials Options
- Summary
- Acknowledgement

Objective
The aim of this presentation is to describe some of the issues when trying to influence the road map of the leading PWB fabricators (Figure 1).

Roadmap of Package Material Technology :
Substrate Materials for Printed Wiring Board

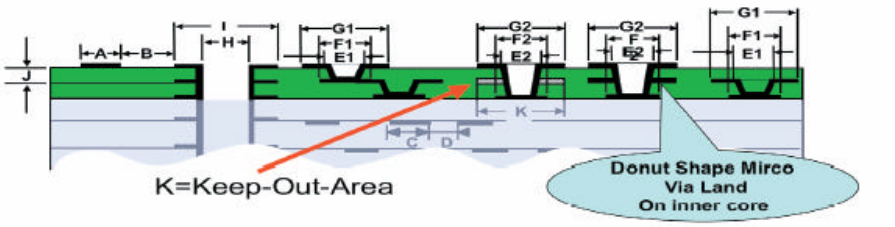
European Mobile Phones:	2001	2004

Year	1998	2005	2010
Tg (TMA) (°C)	120 ~ 130	140 ~160	160 ~180
CTE (ppm/°C)	14 ~15	12 ~13	10 ~12
Dielectricconst (1MHz)	4.4 ~4.6	3.0 ~4.0	<3.5
Dielectric loss (1MHz)	0.02 ~ 0.025	0.013 ~ 0.015	<0.01
Conductor thickness (µm)	12, 18	12, 18	12, 18
Insulator thickness (µm)	60 ~ 100	60 ~ 100	40 ~ 60
Peel strenght (kN/m)	1.0 ~1.2	1.0 ~1.2	1.0 ~1.2
Via diameter (µm)	150 ~250	100 ~150	80 ~100
Lines and Spaces (µm)	50 ~100	30 ~70	25 ~50
Flame retardancy	V-0	V-0	V-0

Source : Conference International Packaging Forum, Tokyo September 1999

Figure 1 – Roadmap for material/Technology needed for Electronic Equipment

Putting a roadmap together is very much an issue of input information. Based on this and the knowledge base of the person or the group of people working on such a roadmap will very much define the output and the usefulness of such documents. Changes in environmental regulation or component developments can make a strong impact on the influence that a roadmap will have on future manufacturing technologies and devices that are produced. Designers of different fields shall be aware of the changes that will take place in technology. (See Figure 2: PCB Requirements for Future Electronics.) An updated roadmap is a good source of information that will help to make the right recession for selecting comments, materials and manufacturing technology. Also managers that have to invest in new technology shall be aware of the technologies that are coming and have to decide if such new technologies will result in new business and could help to improve the profitability of their company in future.



			Cost-Effective	Leading Edge (Mobile Phones)
A	Line width outer layer	-	125 µm	100 µm
B	Spacing outer layer	-	125 µm	100 µm
C	Line width inner layer		100 µm	75 µm
D	Spacing inner layer	-	100 µm	75 µm
E1	Micro via hole size	-	125 µm	100 µm
E2	Micro via hole size	-	200 µm	175 µm
F1	Micro via landing pad	-	300 µm	250 µm
F2	Micro via landing pad	-	400 µm	350 µm
G1	Micro via pad	-	300 µm	250 µm
G2	Micro via pad	-	400 µm	350 µm
H	Drill size through hole	-	250 µm	200 µm
I1	Pad size through hole, outer layer		450 µm	400 µm
I2	Pad size through hole inner layer		470 µm	420 µm
J	E1 / J (aspect ratio)	-	1: 0.8	1: 1
K	Keep-Out-Area	-	Hole size +250 µm	Hole size +150 µm

Figure 2 – PCB Technology Requirements for Future Electronics

Introduction

Europe has a strong position in developing professional Industrial Electronics as well as Automotive, Medical, Mobile Phone, Base station and avionic, space / military systems. Large market segments are like mobile phones and base station have its Original Equipment Manufacturing (OEM) base in Europe. However, for cost reason, large quantities are manufactured in low cost countries like China and other mainly Asian countries. As a result of this, the designs made by OEMs and ODMs have to take into consideration the manufacturing capabilities in the prototype stage as well as the large quantity production. As Europe also is very strong export oriented, and many European companies have their factories also in Asia, the "local content" rules that have been established by some countries have to be considered. As a result of this, a new technology can only be implemented if second sources are available in such countries. Any fancy solution, that needs a lot of know how in fabrication, will therefore not being adopted.

Roadmap by market segments

The European Car industry (Table 1 and Table 2) is a key driver for new technology. However, at the same time, high performance and low cost are major requirements. Also multiple sources for the electronic devices in Europe, USA and Asia are major needs for adopting new technology. (See tables 1 and 2 of the paper "Automotive engine control and dash board") Permanent design changes to place the electronics where it is needed are challenging the component fabricators as well as the material suppliers and the PWB fabricators to meet future needs. In the automotive industry, 3 to 5 years are normal times for the introduction of new technologies. Often long-term Multi Company projects are conducted to find the most cost-effective way that meets the future technology requirements. The "HotCar" was such a project that teamed up with experts from multi companies. The goal of this work group was to define the requirements for PWBs used in different places of the car. As a major part was also related to design new functionality on silicon a close cooperation with the "HotCar" work group was needed.

Table 1 – Airbag Control Electronics

Product	Airbag control unit (high end)			
Technical Details	**Measure**	**Today 2001 – 2002**	**Near Term 2003 – 2005**	**Long Term 2006 - 2010**
Thermal Dissipation :				
Average	Watts	2	2	3
Maximum	Watts			
Electrical Values :				
Maximum	Volts	35	70	70
Number of Supply Voltages	Aver. number	3	3	3
High Currents (Powerparts)	A	10/10msec	10/10msec	10/10msec
Collected Currents	A	20	20	20
Printed Board Technology :				
Base Material	mainly used	Glass reinforced	Glass/ Aramid Microvia layers are reinforced	Glass / Aramid Microvia layers are reinforced
Board Size Area	cm^2	96	96	96
Typical Dimension	mm x mm	80 x 120	80 x 120	80 x 120
Board Thickness	mm	1,6	1,6	1,6
Layer Count	Aver. number	4	4	6
Minimum Line width / line space	µm	125/125	100/100	75/75
Minimum hole diameter - PTH	mm	0,3	0,3	0,3
Minimum hole diameter - Blind/buried	mm	Not used	Not used	Not used
Minimum hole diameter - Microvias	mm	Not used	0,125	0,1
Minimum land diameter – PTH	mm	-	0,3	0,25
Number of holes PTH / Microvias	Average	400 / 0	200 / 400	200 / 600
Component mounting:				
Parts per 6,5 cm^2 ($inch^2$)	Aver. number	27	40	50
Leads per component	Aver. number	3	5	8
Largest Component	Number of I/Os and Type	140 FC	280 FC	360 FC
Minimum pitch	mm	1.0	0,8	0,65
Mounting type (see 3.1.2)	Type	2XReflow	2XReflow	2XReflow
Reliability :				
Default Rate in Field	ppm	100	50	25
Temperature Cycles	Min/max °C	-40 / +85	-40 / +100	-40 / +100
Operating Temperature	°C	80	90	90
Bus Description:				
Frequency	MHz	16	32	64
Prozessor Description:				
On Chip Rise Time	ns	10	4	2
Internal Processor Frequency	MHz	16	32	64
Electromagnet.Compatibility (EMC)				
Emission	dB-µV/m	+10	+10	+10
Susceptibility	V/m	100	200	250
Environmental:				
Recycling requirements	%	95	98	98
Product Details:				
Weight of Assembled Board	max. in Grams	200	150	150

Table 2 – Typical Requirements for Engine Control Unit

Product	Engine control unit			
Technical Details	**Measure**	**Today 2001 – 2002**	**Near Term 2003 – 2005**	**Long Term 2006 - 2010**
Thermal Dissipation :				
Average	Watts	25	30	35
Maximum	Watts			
Electrical Values :				
Maximum	Volts	400	400	400
Number of Supply Voltages	Aver. number	3	4	5
High Currents (Powerparts)	A	8	8	8
Collected Currents	A	20	20	20
Printed Board Technology :				
Base Material	mainly used	Glass reinforced	Glass/ Aramid Microvia layers are reinforced	Glass / Aramid Microvia layers are reinforced
Board Size Area	cm^2	245	245	210
Typical Dimension	mm x mm	175 x 140	175 x 140	175 x 120
Board Thickness	mm	1,6	1,6	1,6
Layer Count	Aver. number	4	6	6
Minimum Line width / line space	µm	160/160	100/100	75/75
Minimum hole diameter - PTH	mm	0,3	0,25	0,25
Minimum hole diameter - Blind/buried	mm	Not used	Not used	Not used
Minimum hole diameter - Microvias	mm	Not used	0,125	0,1
Minimum land diameter – PTH	mm	-	0,3	0,25
Number of holes PTH / Microvias	Average	3000 / 0	1000 / 2000	1500 / 3000
Component mounting:				
Parts per 6,5 cm^2 ($inch^2$)	Aver. number	15	20	30
Leads per component	Aver. number	4	6	8
Largest Component	Number of I/Os and Type	388 BGA	500 BGA	800 BGA
Minimum pitch	mm	1,0	0,8	0,65
Mounting type (see 3.1.2)	Type	2XReflow	2XRflow	2XReflow
Reliability :				
Default Rate in Field	ppm	100	50	25
Temperature Cycles	Min/max °C	-40 / +85	-40 / +125	-55 / +125
Operating Temperature	°C	80	90	100
Bus Description:				
Frequency	MHz	60	100	200
Prozessor Description:				
On Chip Rise Time	ns	5	3	2
Internal Processor Frequency	MHz	65	100	130
Electromagnet.Compatibility (EMC)				
Emission	dB-µV/m	+6	+6	+6
Susceptibility	V/m	100	150	200
Environmental:				
Recycling requirements	%	95	98	98
Product Details:				
Weight of Assembled Board	max. in Grams	500	400	300

"HotCar" Project

In this HotCar project, a large number of new features have been defined for future car electronics. Parts like "Steer by wire" or " by wire" have their own reliability requirements. As such, material suppliers and technologists are forced to come up with materials and fabrication solution that will meet future requirements. The HotCar project was finished in November 2004. The final report is available also on the public domain. (See Figure 3)

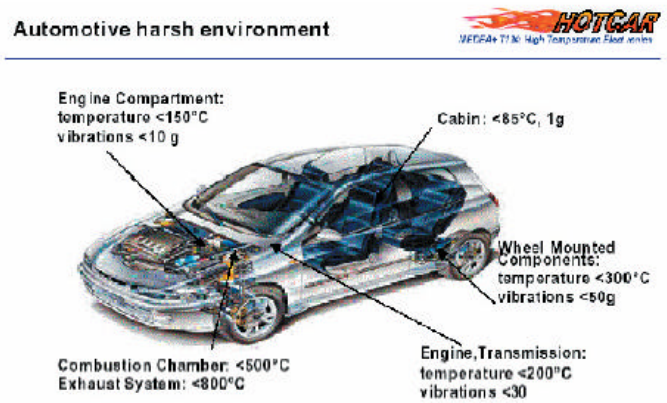


Figure 3 – "HotCar" Project for Advanced Technology and Material Developments

Trend to Higher Data Transmission Rates

The signal-processing rate increases within all fields of electronics. Examples of changes in PCBs for communications are shown in Table 3.

Table 3 – Requirements for Mobile Phone Base Station

Product	Mobile Phone Base Stations			
Technical Details	**Measure**	**Today 2001 – 2002**	**Near Term 2003 – 2005**	**Long Term 2006 - 2010**
Thermal Dissipation :				
Average	Watts	30	40	40
Maximum	Watts	50	60	60
Device Voltage :				
Minimum	Volts	1.8	1.8	1.5
Number of Supply Voltages	Averag.number	4	4	4
Printed Board Technology :				
Base Material	mainly used	FR4, CE	Low dissipation factor (tan d)	Low dissipation factor (tan d)
Board Size Area	cm²	650	650	650
Typical Dimension	mm x mm	280 x 230	280 x 230	280 x 230
Board Thickness	mm	2.0	2.4	3.0
Layer Count	Aver. number	10	16	20
Minimum Line width / line space	µm	125/125	100/100	80/80
Minimum hole diameter - PTH	mm	0,3	0,25	0.2
Minimum hole diameter - Blind/buried	mm	0.3	0.2	0.15
Minimum hole diameter - Microvias	mm	0.15	0,12	0.1
Minimum land diameter – PTH	mm	0.3	0,25	0.2
Number of holes PTH / Microvias	Average	2000 /5000	3000/5000	5000/5000
Component mounting:				
Parts per 6,5 cm² (inch²)	Aver. number	12	15	18
Leads per component	Aver. number	10	15	20
Largest Component	Number of I/Os and Type	304QFP 480BGA	304QFP 1000BGA	1500BGA
Minimum pitch	mm	0.5QFP 1.0BGA	0,5QFP 0.8BGA	0.8BGA
Mounting type (see 3.1.2)	Type	2XReflow	2XReflow	2XReflow
Reliability :				
MTBF	Hours	20000	30000	40000
Temperature Cycles	Min/max °C	-55 / +125	-55 / +125	-55 / +125
Operating Temperature	°C	50	60	70
Bus Description:				
Frequency	MHz	600	1200	2400
Prozessor Description:				
On Chip Rise Time	ns	1.0	0.7	0.5
Internal Processor Frequency	MHz	600	1200	2400
Electromagnet.Compatibility (EMC)				
Emission	dB-µV/m	30 (Cispr 22)	50 (Cispr 22)	50 (Cispr 22)
Susceptibility	V/m	50	60	60
Environmental:				
Recyclability	%	20	30	50
Product Details:				
Weight of Assembled Board	max. in Grams	400	450	500

Table 4 – Trends in processor and Signal Speed

	Aktuell *(Present)* 1- 2 Jahre *(years)* 2001 - 2002	Nahe Zukunft *(Near Future* 3 - 5 Jahre *(years)* 2003 - 2005	Ausblick *(Outlook)* 6 -10 Jahre *(years)* 2006 - 2010
Chip clock	1... 2 GHz	3 ... 5 GHz	8...10 GHz
Bus clock	166 - 200 MHz	266 ... 500 MHz	600..800 MHz electrical and optical Systems
Bus transferrate	32 x 200 Mbit/s x 2 = **12 Gbit/s**	64 x 400 Mbit/s x 2 = **50 Gbit/s**	128 x 800 Mbit/s x 2 = **204 Gbit/s**
Signal risetime (bus)	3... 1 ns	1... 0.4 ns	0.3 ... 0.1 ns
RF harmonics on bus	≤ 1 GHz	≤ 2.5 GHz	≤ 10 GHz or optical
Supply Voltage	3.3 ... 2.5 V	2.5 ... 1.8 V	1.8 ... 1.2 V
Slewrate (du/dt)	1... 3 V / ns	2... 5 V / ns	6...12 V / ns or optical

(Source: FH Giessen Friedberg)

These changes also mean increasing clock frequencies in digital technique. (Table 4.) Even in consumer products such as PC, at present bus clock frequencies of approx. 500 MHz are already in use. This corresponds to a cycle time of 5 ns (nanoseconds), requiring impulse rise times (tR) of approx. 1 - 2 ns. For the undisturbed transmission of fast impulses on PCB lines the traces must be able to transfer frequencies (harmonic waves) up to 1/tR , i.e. 1/1ns = 1 GHz, indicating thus transverse electromagnetic wave characteris tics. Due to the small wavelengths of these frequencies (below 30cm, starting from 500 MHz and er = 4) radiation by the bus lines is an increasing problem. Keeping the radiation below the limit values (EMC law) becomes more and more difficult. The traces of printed circuit boards become wave conductors (transmission lines). (Remarks: Using optical transmission lines can avoid this problem. With reduced impulse rise time also undesired signal copy effects (cross talk) between different lines increase steadily. Since the crosstalk in detail is depending on the so-called Slew-rate (du/dt), which is the relation between voltage increase and impulse rise time, the copy effect (and the thermal losses as well) can be compensated by lowering the operating voltage. The necessary consequences for the conductor structures and the layer stack-up of printed circuit boards, are important and must been considered by the electronic designers at the early stage of design.

Materials

Like everything that is mass-produced also state of the art multilayer boards with micro via holes are subject to the search for the penny to spare. The standard FR4 has been ruled out several times but it has survived every attack so far. The special materials like BT and others have found their niches and wait for the wider success when FR4 fall short. A general comparison of materials is shown in Table 5.

Table 5 – Comparison of Material for PCBS

Property	Units	Aramid / high Tg Epoxy	RCF (epoxy) normal Tg Epoxy	FR-4 / LDP normal Tg Epoxy	Test Method
X-axis CTE	ppm/°C	10 - 12	55 - 75	16 - 20	IPC-TM-650; 2.4.41
Y-axis CTE	ppm/°C	10 - 12	55 - 75	16 - 20	IPC-TM-650; 2.4.41
Z-axis CTE	ppm/°C	105 - 110	55 - 75	60 - 70	IPC-TM-650; 2.4.41
Tg (by DSC)	°C	175 - 185	135 - 175	140 - 180	IPC-TM-650; 2.4.25
Peel Strength	N/mm	0.95 – 1.7	0.90 – 1.2	1.1 – 1.4	IPC-TM-650; 2.4.8
Dimensional Stability	Percent	0.02	0.10	0.05	
Solder Float	10 sec @288°C	Pass	Pass	Pass	IPC-TM-650; 2.4.23
Solder Float	60 sec @288°C	Pass	Pass	Pass	IPC-TM-650; 2.4.23
Dielectric Constant	@ 1 MHz	3.8	3.6	4.8	IPC-TM-650; 2.5.5.3
Dielectric Constant	@ 1 GHz	3.4	3.4	4.5	IPC-TM-650; 2.5.5.3
Dissipation Factor	@ 1 MHz	0.013	0.025	0.015	IPC-TM-650; 2.5.5.3
Dissipation Factor	@ 1 GHz	0.018	0.028	0.010	IPC-TM-650; 2.5.5.3
Water Absorption	percent	0.32	1.04 - 1.6	0.20	IPC-TM-650; 2.6.2.1
Electrical Strength	V/µm	59	39	42	IPC-TM-650; 2.5.6.2
Dielectric Breakdown	kV	60		50	IPC-TM-650; 2.5.6
Resistivity					
Surface (23°C; 50%RH)	Mega-ohms	$>1.0 \times 10^{3}$	$>1.0 \times 10^{8}$	$>1.0 \times 10^{7}$	IPC-TM-650; 2.5.17.1
Surface (35°C; 90%RH)	Mega-ohms	$>1.0 \times 10^{7}$	$>1.0 \times 10^{7}$	$>1.0 \times 10^{6}$	IPC-TM-650; 2.5.17.1
Volume (23°C; 50%RH)	Mega-ohms-cm	$>1.0 \times 10^{-9}$	$>1.0 \times 10^{7}$	$>1.0 \times 10^{8}$	IPC-TM-650; 2.5.17.1
Volume (35°C; 90%RH)	Mega-ohms-cm	$>1.0 \times 10^{4}$	$>1.0 \times 10^{4}$	$>1.0 \times 10^{4}$	IPC-TM-650; 2.5.17.1
M&IR (6 days @ 65°C; 98%)	Mega-ohms-cm	$>1.0 \times 10^{4}$	$>1.0 \times 10^{4}$	$>1.0 \times 10^{4}$	IPC-TM-650; 2.6.3.E
Flexural Strength	MPa	289		310	ASTM-D-790
Flexural Modulus	GPa	14.5		19	ASTM D 790
Tensile Strength	MPa	220		510	ASTM D 3031
Tensile Modulus	GPa	14.5		17.4	ASTM-D-3031
Poisson's Ratio	ratio	0.34		0.33	
Specific Gravity	g/cm3	1.34	1.45	1.80	ASTM-D-792 Method A
Laminate Smoothness	Angstroms	2200		4200	
Thermal Conductivity	W/MK	0.20		0.35	ASTM-E-1225
Flammability	UL standard	94 V-0	94 V-0	94 V-0	UL 94
Relative Thermal Index	°C	105 - 120	90 - 115	105 - 130	UL 746

One exception to the rule is the aramid fiber based laminate that has been used in large quantities in Japan (Figure 5). The advantages of aramid are mainly its dimensional stability and the fact that the fibers are easy to laser drill unlike glass.

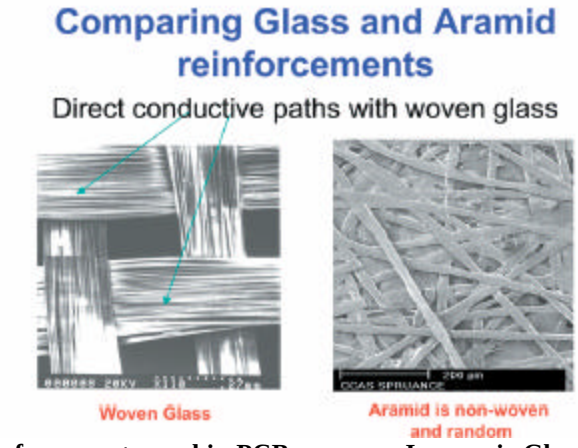


Figure 5 – Comparison of Reinforcements used in PCBs – woven Inorganic Glass Cloth in Comparison with Non-woven Aramid 100% Organic Reinforcement

One of the improvements to FR4 is LDP (Laser Drillable Prepreg) with its finer glass threads and flatter weaving. The resin rich areas of FR4 LDP are much smaller and this aids the laser drilling to a better quality. To set up the laser to drill equal in almost pure resin or glass bundles, as is the case in standard FR4, is simply not possible with current laser technology. However, this material is based on inorganic glass that has a reduced adhesion to the organic epoxy resin. Under mechanical and/or thermal stress condition, this can lead to conductive anodic filaments or metal migration shorts in PCBs.

Advanced material options

In Europe, many new designs are also manufactured locally. These types of PWBs are needed in larger quantities after its evaluation phase which is often 12 to 24 month after prototyping the electronic devices. A good knowledge about materials, processes and PWB fabrication technologies is needed to predict what technology will be used in the future. Also a good knowledge of individual roadmaps is needed as well as latest know how on materials and processes. As indicated in the earlier part of the paper, finer lines and spaces as well as smaller holes, and micro-via-holes, will be needed to meet future routing density and cost-effective design requirements. Standard FR4 laminates may reach its limits in terms of conductive anodic filament (CAF) resistance and dielectric properties. This is due to the inorganic glass materials and its capabilities to

adhere to the resin. Resin recession may result in CAF and metal migration that create shorts between narrow insulation distances in micro-via-holes or in "layer to layer" areas. The International Business Machine Corporation has developed systems with very thin dielectric materials that did not exhibit CAF or migration. This may be used for multilayer printed circuit boards and for electronic device package like ball grid array package, multi chip module, and memory chip. The INT BUSINESS MACHINES CORP filed a Patent No: US5981880 for chip packages that indicated new reinforcements. The NOVELTY was the substrate - The substrate that has prepreg comprising glass fabric impregnated with epoxy resin, is provided with power planes. The power planes are encapsulated within the non-conductive layers (156,158) made up of dielectric material free of continuous glass fibers. The use of aramid Kevlar® fiber paper is disclosed. The USE describes it as follows: - For electronic device package like BGA package, organic chip carrier package, multi chip module, and memory chip. ADVANTAGE - Prevents short circuit of power plane carried by migration of conductive material along continuous glass fibers. Eliminates conductive anodic filaments shorts in PCB. Reduces cost of package by optimizing number of conductive planes. Based on the knowledge of new materials, roadmaps describe functionality and it is up to the PWB designer to define and specify the new materials that meet the needs of future electronic devices. It has been demonstrated that organic reinforced laminates provide CAF resistance and do not exhibit resin recession even under stringent solder float test condition of 288°C for 20 seconds or several times at 288°C for 10 seconds.

New environmental requirements are putting a ban on lead for soldering as well as on halogen as a flame retardant. Although lead free is used for some time, a final answer on reliability could not being made. This is because of the thicker intermetallic layers between the solder lands of the materials at the component or the printed circuit board solder lands. (Figure 6.)

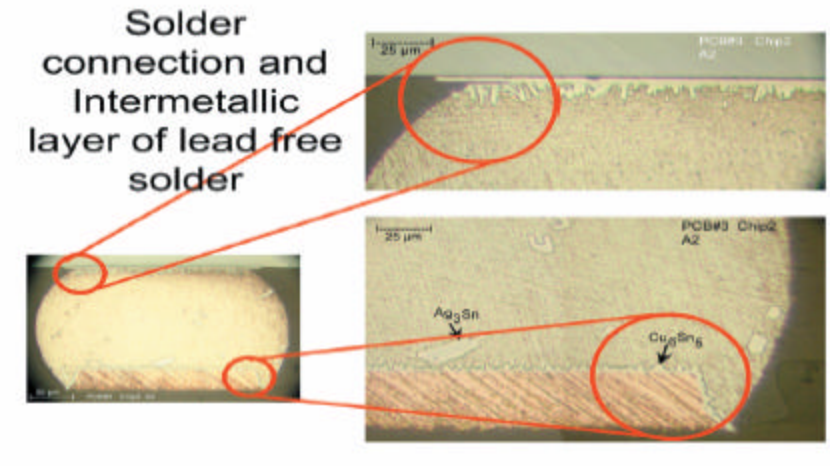


Figure 6 – Intermetallic Layer at the Interphase of the Chip and the PWB

Cost reduction through miniaturization is also one of the major challenges for the future. To apply a solderable surface to a silicon chip is not difficult anymore. Also the cost for the distribution layer on Silicon has become substantially lower compared to 3 years ago. Reliability questions, however, could not fully be answered. The major reason for this are the coefficient of thermal expansion between the individual materials that are used.

As a packaging solution, Flip Chip will become very attractive in the near future. However, before this technology can be adopted in large volume, the reliability issues must be clarified. Here, the CTE mismatch between the silicon of the component distribution layer and the PCB should be compensated. (Figure 7.) This will then reduce the stress created by the different CTE levels of materials used in PCBs as well as the stress coming from the soldering process. In addition, the lead free soldering process will provide a stronger solder filled. As lead is removed from the solder, the cold flow characteristics of the solder filled are nearly eliminated. As a result of this changes, the stress between components and PCB, which was created during the high soldering temperature of the lead free soldering process will remain in the electronics device during its lifetime. Additional thermal stress during operation of the device will continually stress and strain the solder connection at the component and the PCB. Depending on the life cycle expectation of the electronic device defects may happen earlier compared to today's electronic with standard FR4 and solder that contain lead.

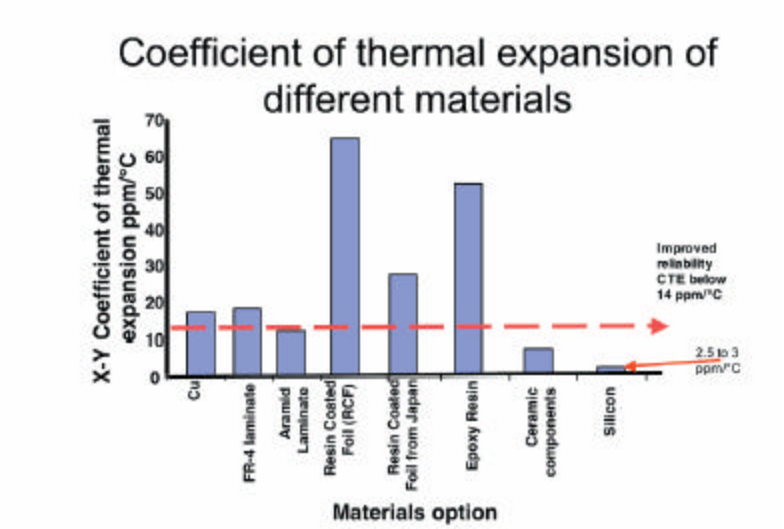


Figure 7 – A Comparison of Different CTE Levels of Materials used in PCBs

The SSD technology uses flux adhesive to assemble fine pitch BGAs without applying solder paste to the PWB lands. By controlling the level of flux, a minimum on residues is guaranteed. Figure 8.) In addition NO shorts under the fine pitch components have been observed. It is also feasible that components are pre-fluxed and allow a placement to the PCB without any additional fluxing, gluing or solder past printing process.

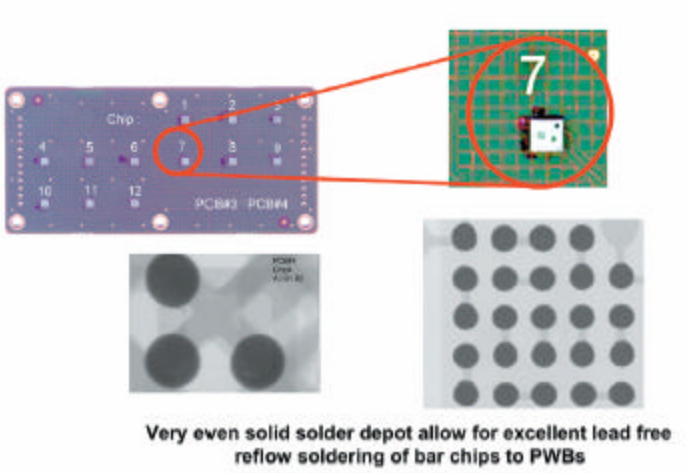


Figure 8 – Flip Chip Application soldered to the PCB using Lead Free Solder in Form of a Solid solder Depot (SSD Technology)

Summary
Smaller devices with finer lines and finer spaces are needed in future to meet the miniaturization requirements and reliability needs. Improved materials with lower tolerances will help to design and fabricate electronic interconnection that will meet the needs of the electronic designers in terms of propagation delay and signal speed. Lead free and halogen free is a must for the near future. Road maps of Printed Circuits are very much driven by the components that are used and the design techniques that are applied. This paper should draw the attention to the people that makes it best effort to predict what is needed in future based on the requirements of the electronics, the components that are used and the PWB fabrication, component and assembly technology that will be developed in the near future. (Figure 9.)

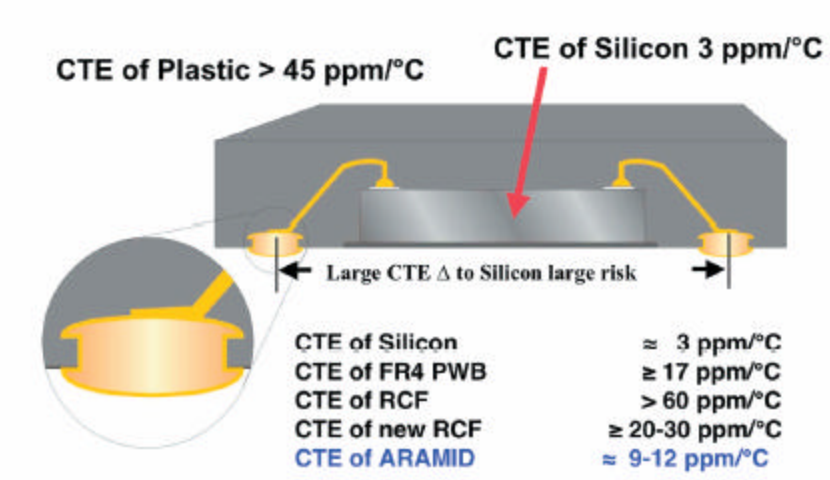


Figure 9 - Example of a Component Package
(Silicon in the package will become larger. At the same time, the package will become smaller. In the near future NO packages may be used at all.)

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