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Japan's JISSO Technology Roadmaps

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History
Japan has a long history of publishing very important technology roadmaps. Some of the Japanese roadmaps published in the past are:

JPCA Roadmaps
Report on the Technology Roadmap for Advanced Systems Integration and Packaging English version 1998, translated by IPC.What Makes Dreams Come True? A roadmap of microvia technology published in 1998

JIEP Roadmaps
The Technology Roadmap for Electronic Packaging Technology in Japan (1999 – 2010)
English version September 1998, translated by SEMI

EIAJ / (JIETA – Japan Electronics and Information Technology Industries Association)
Report on Semiconductor Packaging Technologies, December 1996
Multi Media Vision 2005, March 1997
Report on MCM / KND Packaging Technologies, October 1997

In 1999 Japanese technologists decided to go to "JISSO". JISSO is a made up word that means the total system integration. It encompasses all relevant technologies, such as semiconductor ICs and their packages, other electronic components, PWB, materials, interconnecting structures, environmental protection, and system design.

This was a major decision on the part of the Japanese technology organizations. In 1999 and again in 2001 and 2003 there has been a JISSO technology roadmap.

The first JISSO roadmap was published in 1999. The Japanese version was published in August 1999 and an English version followed in September 2000. The second JISSO roadmap was then published in April of 2001. This roadmap was also published in English. The 2003 JISSO roadmap was only published in Japanese.

Roadmap organization
JISSO roadmaps are organized in a unique layout as compared to the IPC or NEMI roadmaps. The chapter layout is in Product Type sections. There are sections on Palmtops, DVD's, Cellular phones, Notebook PC's, etc. The sections are reviewed before each publication and some are dropped and others are added as the market changes.

The Japan JISSO Technology Roadmap is an excellent document. The definition of JISSO technology is fully explained in the Foreword and in the Preface. The roadmap is developed starting with a very thorough list of survey questions administered to many, many companies throughout Japan's electronic industries. This is a process that is unique to Japan and probably would not be successful in the U.S or Europe.

The roadmap editorial board members do outstanding work analyzing the survey results and drawing conclusions, which are manifested in the technology trends reported in this roadmap. If one believes that completing a survey is difficult, think of the difficulty of analyzing all of the data in a cohesive manner.

JISSO sees itself as a system integrator encompassing a wide range of technology fields. As the technology definition of JISSO indicates, the roadmap should be considered from a macro viewpoint as "system technology encompassing areas such as function, configuration, manufacturing design, interconnect technology, and cooling technology.

Japan gained the position of an electronics leader by developing an industry characterized by volume production of standardized products -- a production style that Japan has been excellent in. Manufacturing equipment, the development of which Japan has contributed to, has evolved to a stage that allows everybody to manufacture products.

In Japan, attention is focused on cellular phones and personal digital assistants (PDAs) as mobile information equipment that

can obtain up-to-date information via the Internet. In addition, an information technology (IT) revolution as represented by the keyword "mobile" is accelerating its progress. This is closely related to the reason why the Japan Electronics & Information Technology Industries Association (JEITA) was born from the Electronics Industries Association of Japan (EIAJ). As this digital networked information society is advancing, electronic information equipment is rapidly progressing towards higher performance, more advanced functions (diversification and integration), and smaller size and higher mobility (higher density). In this circumstance, greater importance is placed on the JISSO technology that provides an interface between the semiconductor integrated circuit technology, which is the heart of the basic technology that will support this advance, and the electronic information equipment.

The environment around JISSO is diversified and harsh. Various JISSO technologies have been proposed to implement higher-density semiconductor packages providing more advanced functions. The purpose of the JISSO roadmap publication is to provide a shared viewpoint regarding future trends and forecast targets in JISSO technology. In addition, by publishing the Roadmap, JEITA expressed its desire that the Japanese JISSO technology industry should transmit information to the world and that Japan should keep a competitive advantage in JISSO technology. The primary aim of the Roadmap was to stimulate technology communication with principal industries associations and research unions in the US, Europe, Taiwan, Singapore, and other countries.

Technology Descriptions

The following table (Table 1.) has been used in all three JISSO roadmaps. It defines the different classifications of products. Class A or conventional boards are generally available and represent 80% of all PCB's. Class B products are considered leading edge and represent15% of the total and Class C products are state of the art representing 5 %.

Table 1 - Product Classification

Class	Required Production Technology	Production Ratio	Cost
Class A Conventional	General Technology	80 %	Reasonable
Class B Leading Edge	Advanced Technology	15 %	Cost up
Class C State of the Art	Most Advanced Technology	5 %	High Cost

Base Materials for Buildup layers

The following three figures (Figures 1, 2, and 3.) represent material properties and their trends as seen by the JISSO roadmap survey participants. Glass transisition temperature, dielectric constant and dielectric loss are charted. From the tables one can draw the conclusion from the Tg chart that heat resistance for Pb-free soldering is a focus of the survey participants as is lower dielectric characteristics for high speed applications. (These tables are taken from a presentation by Henry H. Utsunomiya of Interconnection Technologies, Inc.)

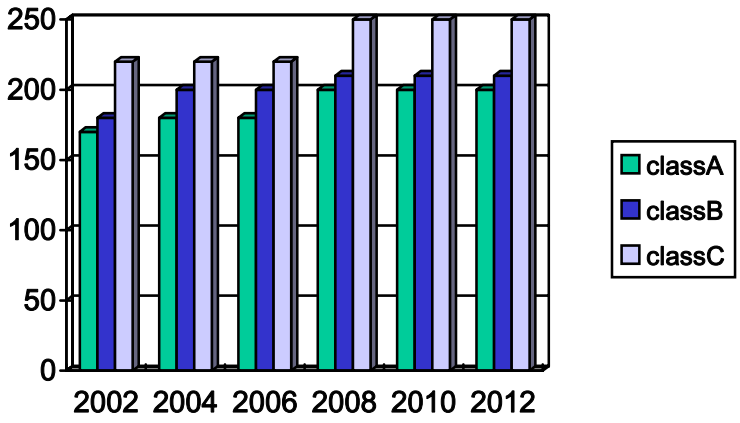

Figure 1 - Glass Transition Temperature - Tg. (oC)

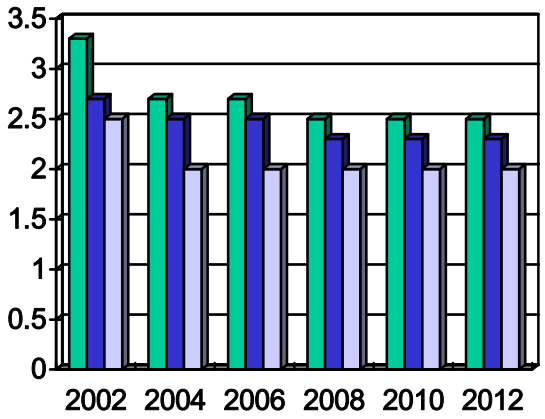

Figure 2 - Dielectric constant @ 1 GHz

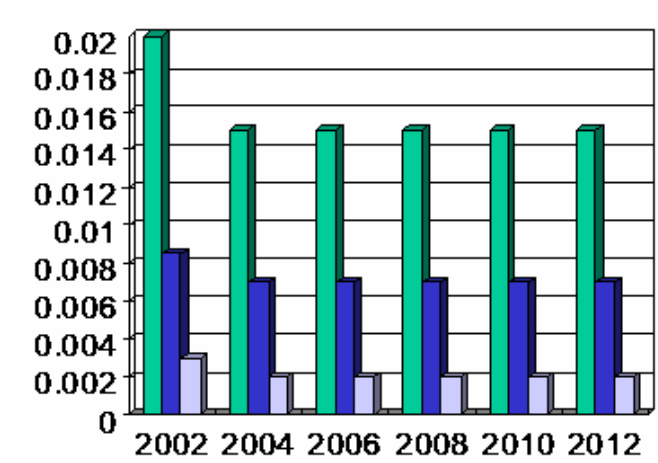

Figure 3 - Dielectric Loss @ 1 GHz

Buildup Technology Conductor Specifications

In Figures 4, 5, 6, and 7, depicting Japanese build up technology; we can see that Japan is looking for Improvement based on existing technology and novel circuit generation technology developments. Build up technology is one of the focus technologies in Japan and they continue to set the standard for development. These figures represent Japanese rigid board attributes on line width and spaces, and drilled and laser via dimensions.

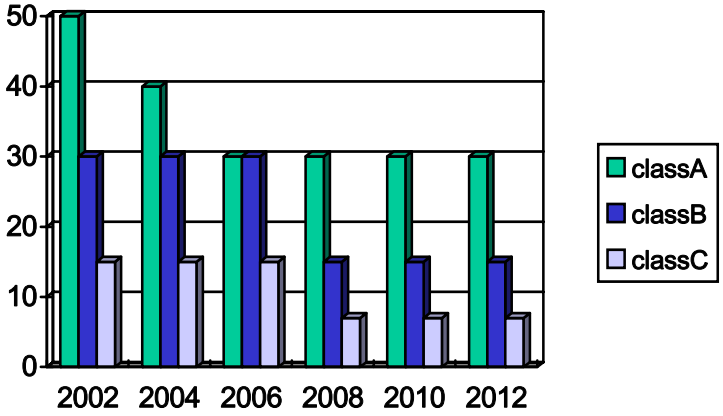

Figure 4 - Line width of conductors (um)

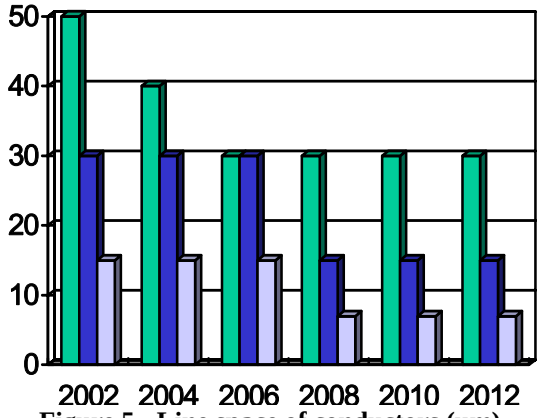

Figure 5 - Line space of conductors (um)

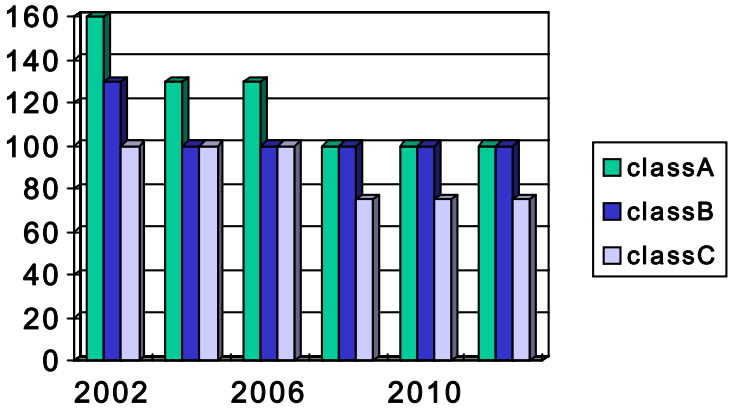

Figure 6 - Drilled Hole Size (um)

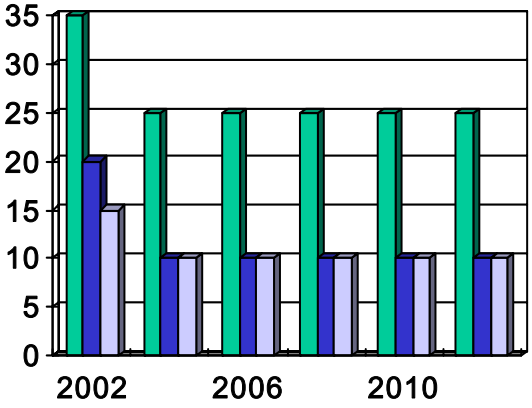

Figure 7 - Laser via size (um)

2005 Japan Jisso Technology Roadmap

February 22, 2005

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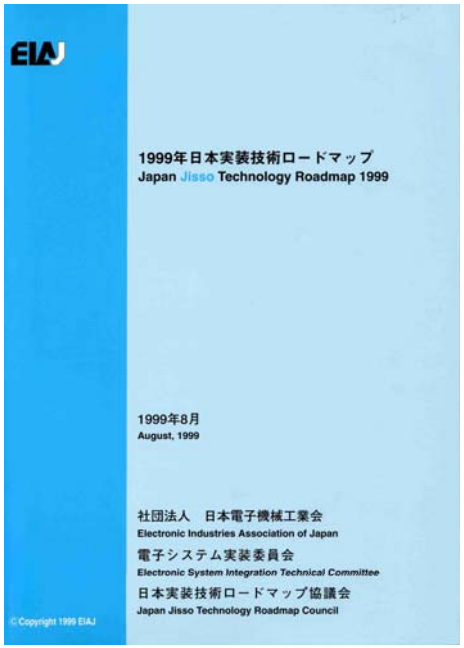
- Japan PWB Industry Status
- PWB Base Material Roadmap
- PWB Technology Roadmap
- Difficult Challenges
- Summary

Jisso Technology Roadmap



1999 Jisso Roadmap

276 Pages

2001 Jisso Roadmap

349 Pages

2003 Jisso Roadmap

598 Pages

Jisso Roadmap Committee Member

Chairman: Kunuaki Takahashi, Toshiba

Vice Chairman: Hisao Kasuga, NEC

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WG2 Leader: Absent

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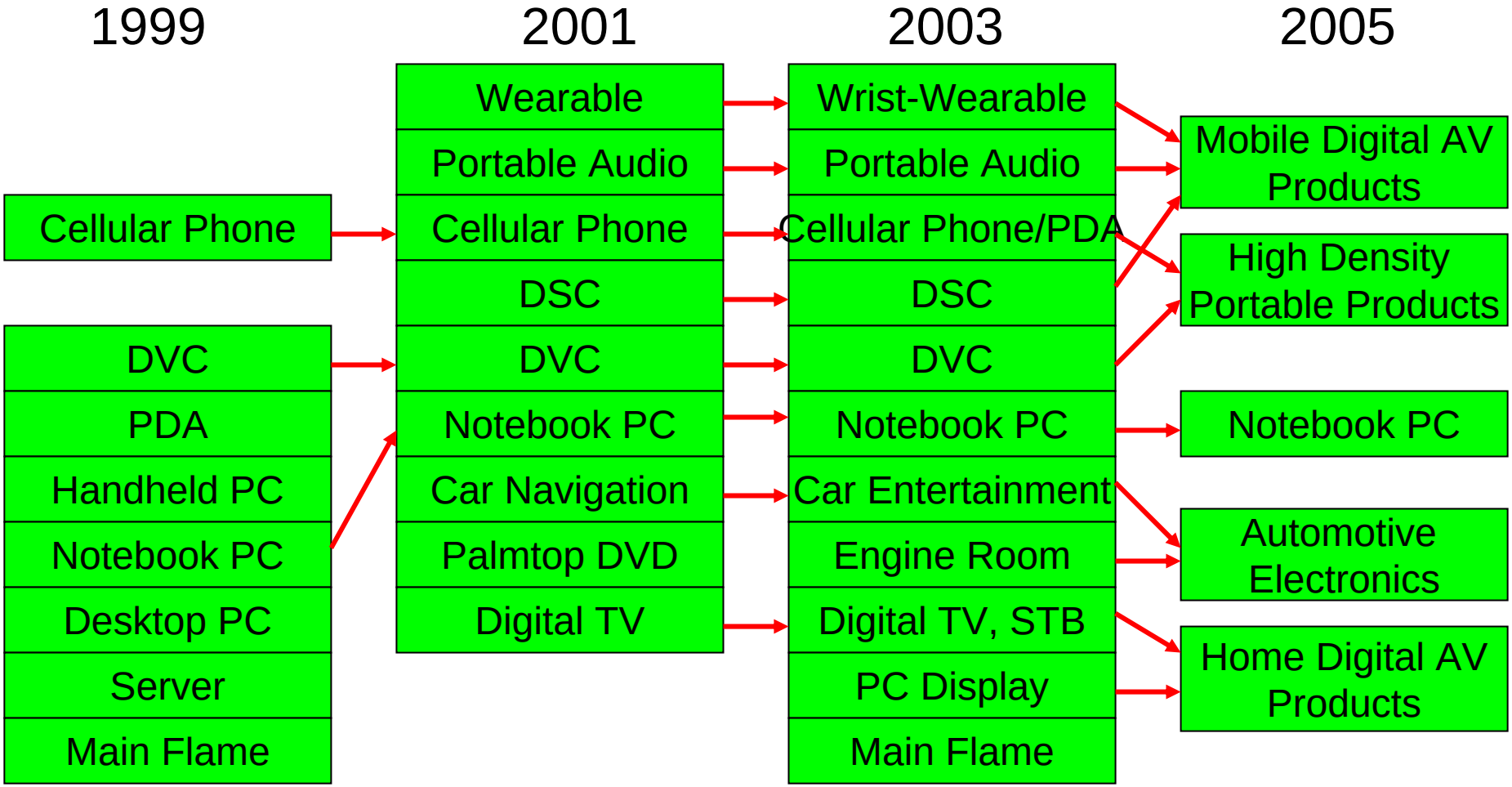
- Kiyoshi Tomita: Kyocera SLC
- Masaaki Minimi: Kyocera
- Toshiyuki Toyoshima: Mitsubishi
- Toyoo Tobe: Hitachi Chemical

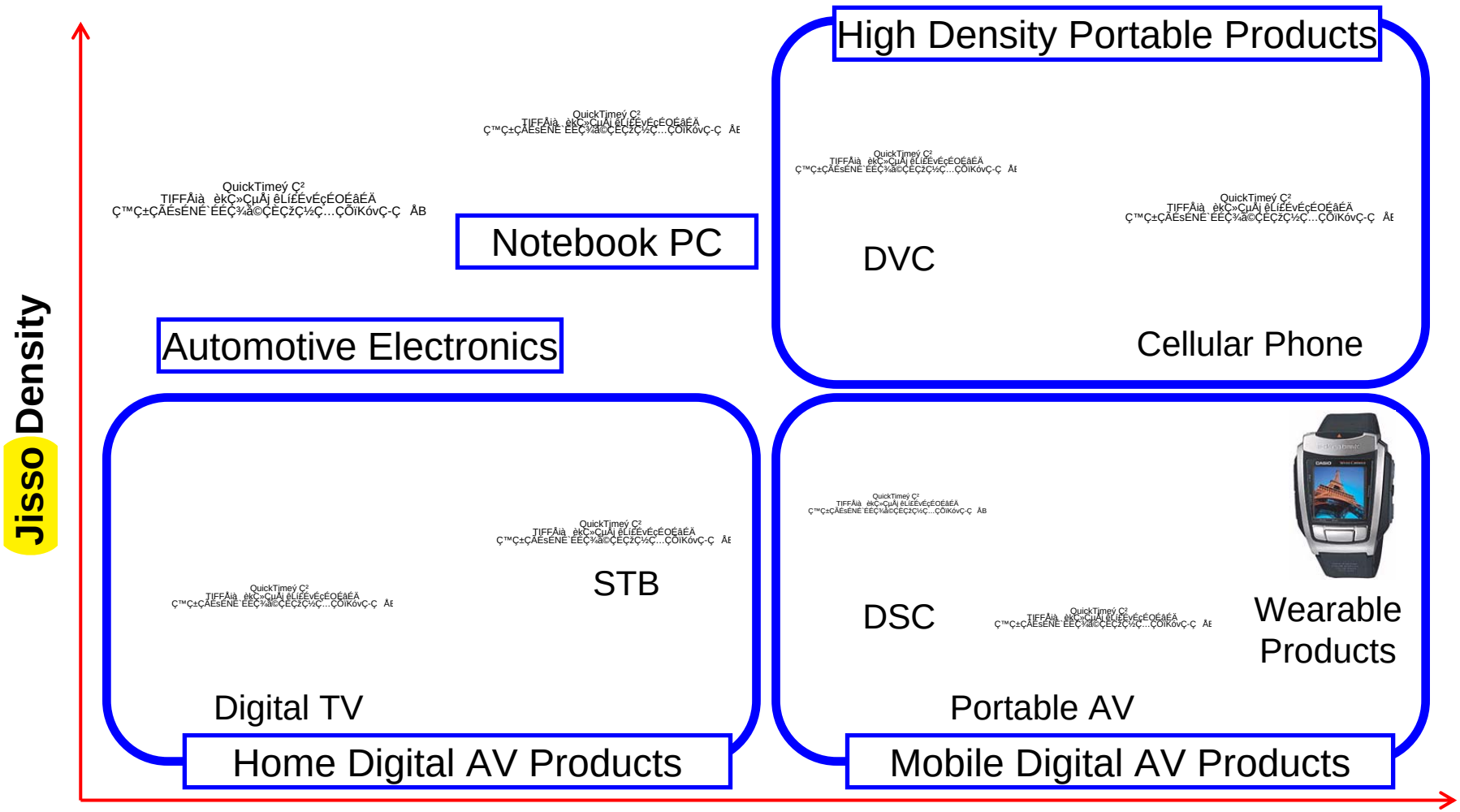
2005 Jisso Roadmap

1. Introduction
2. Electronics Products
3. Electronics Devices & Components
    1. Semiconductor Packaging
    2. Passive Components & Connectors
    3. Printed wiring Boards
    4. Assembly & Mounting Facilities
4. Topics
5. Appendix

Emulators Change in Jisso Roadmap



2005 Jisso Roadmap Emulators

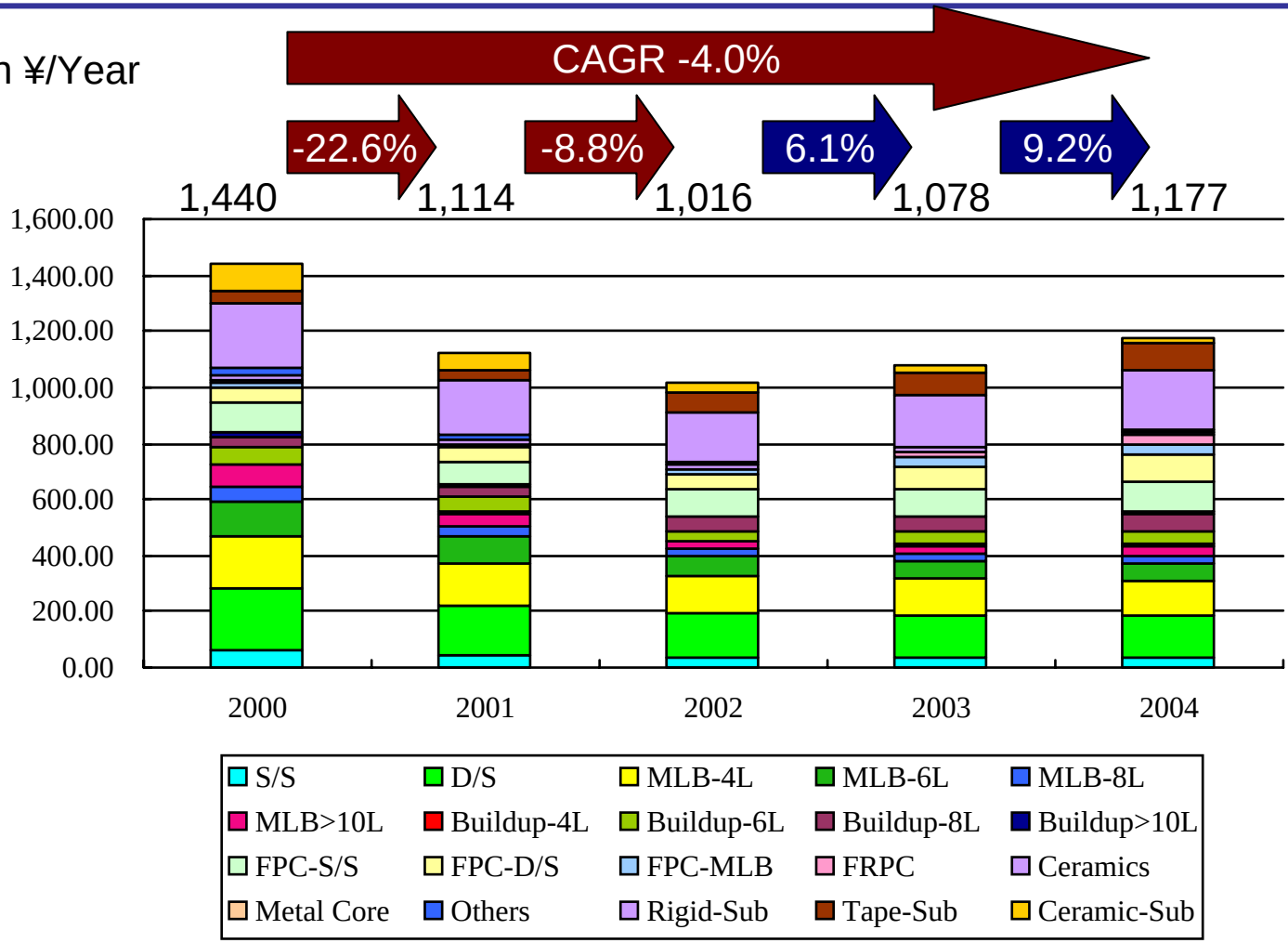


Current Japanese PWB Status

- Japanese PWB Total Sales Amount
  - Mother Board
  - FPC
  - Packaging Substrate

PWB Production Amount Progress

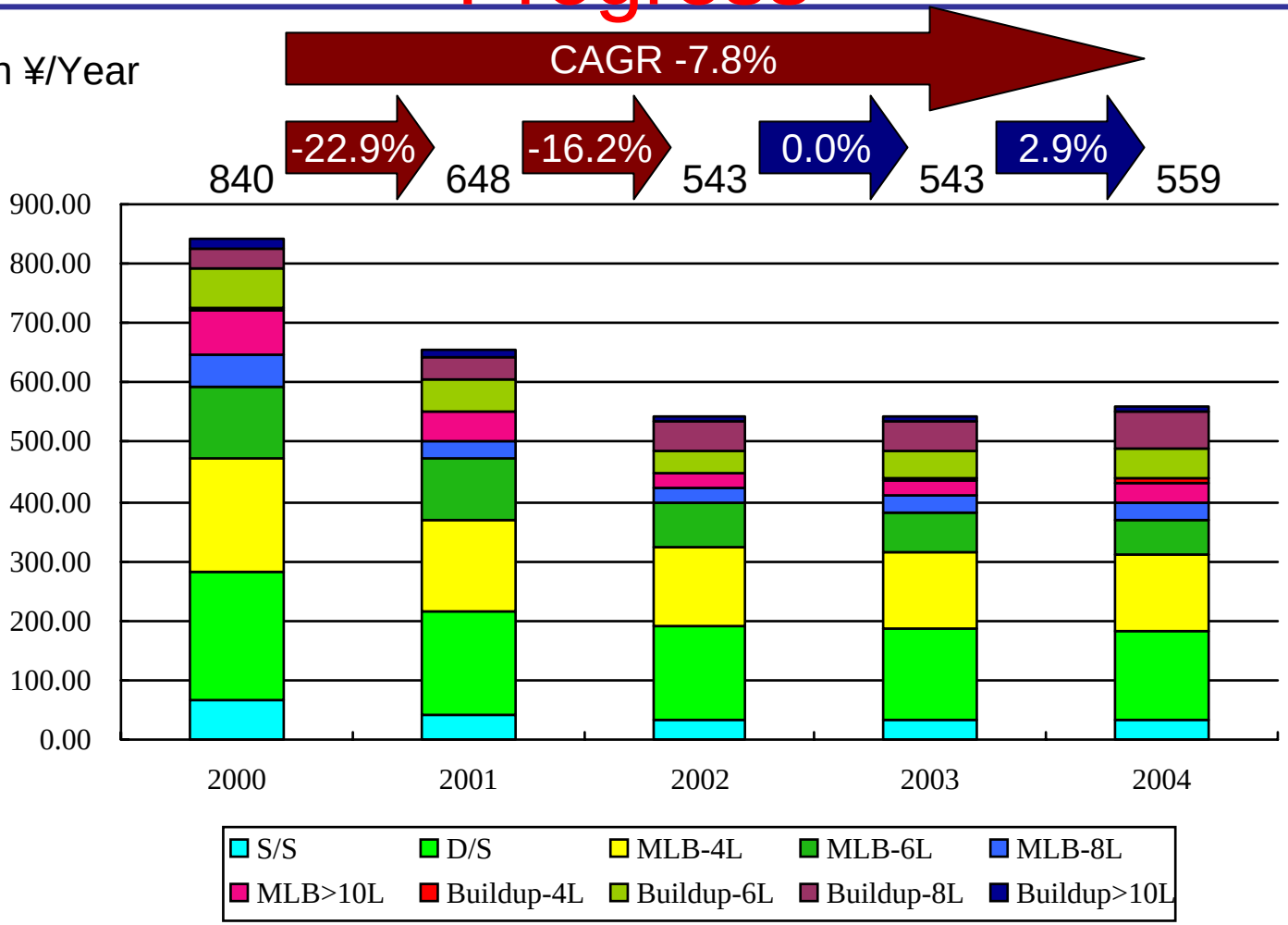
Unit: Billion ¥/Year



Source: Electronic Circuits Industry Survey Report 2004 Edition, JPCA

Mother Board Production Amount Progress

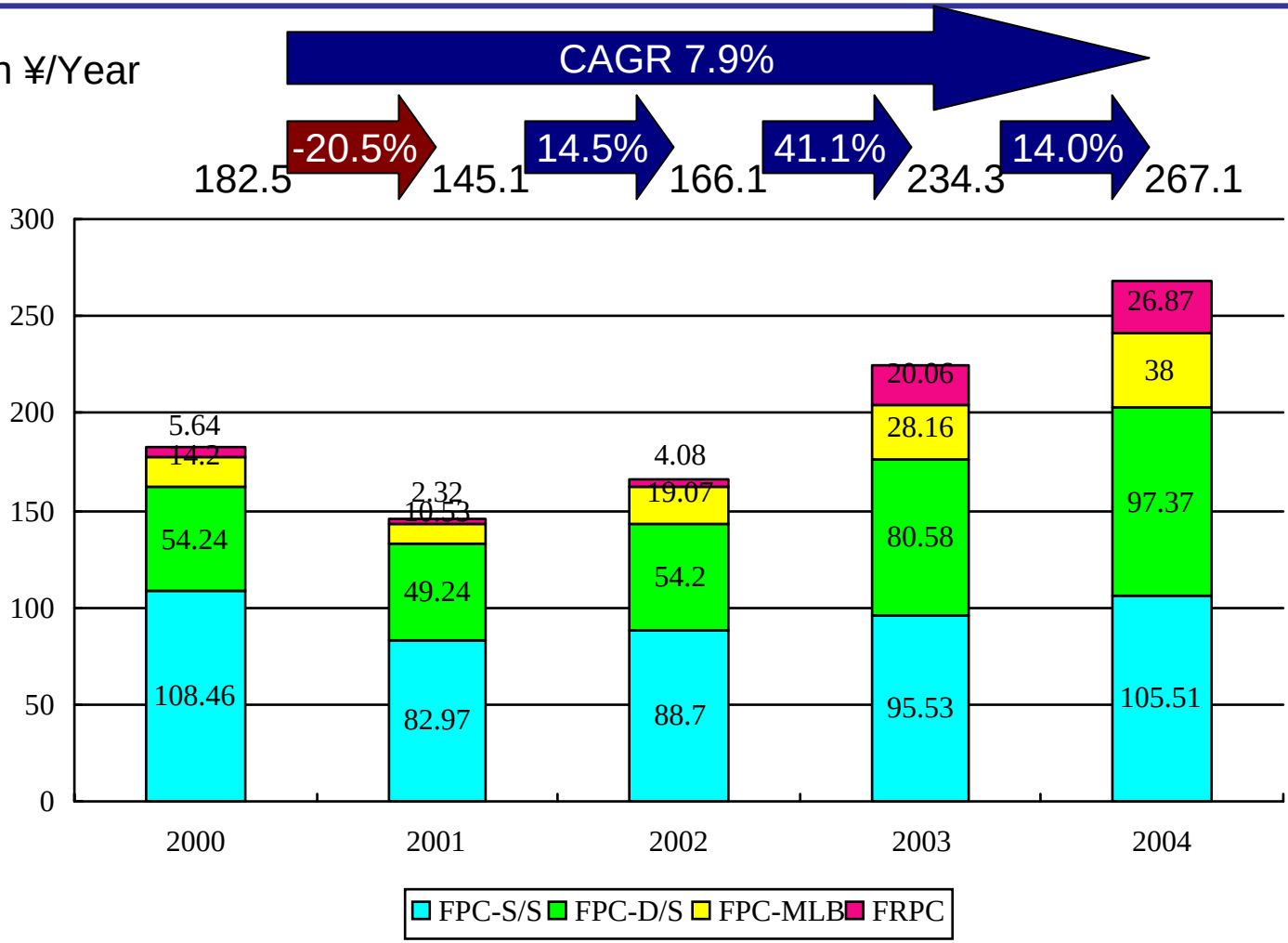
Unit: Billion ¥/Year



Source: Electronic Circuits Industry Survey Report 2004 Edition, JPCA

FPC Production Amount Progress

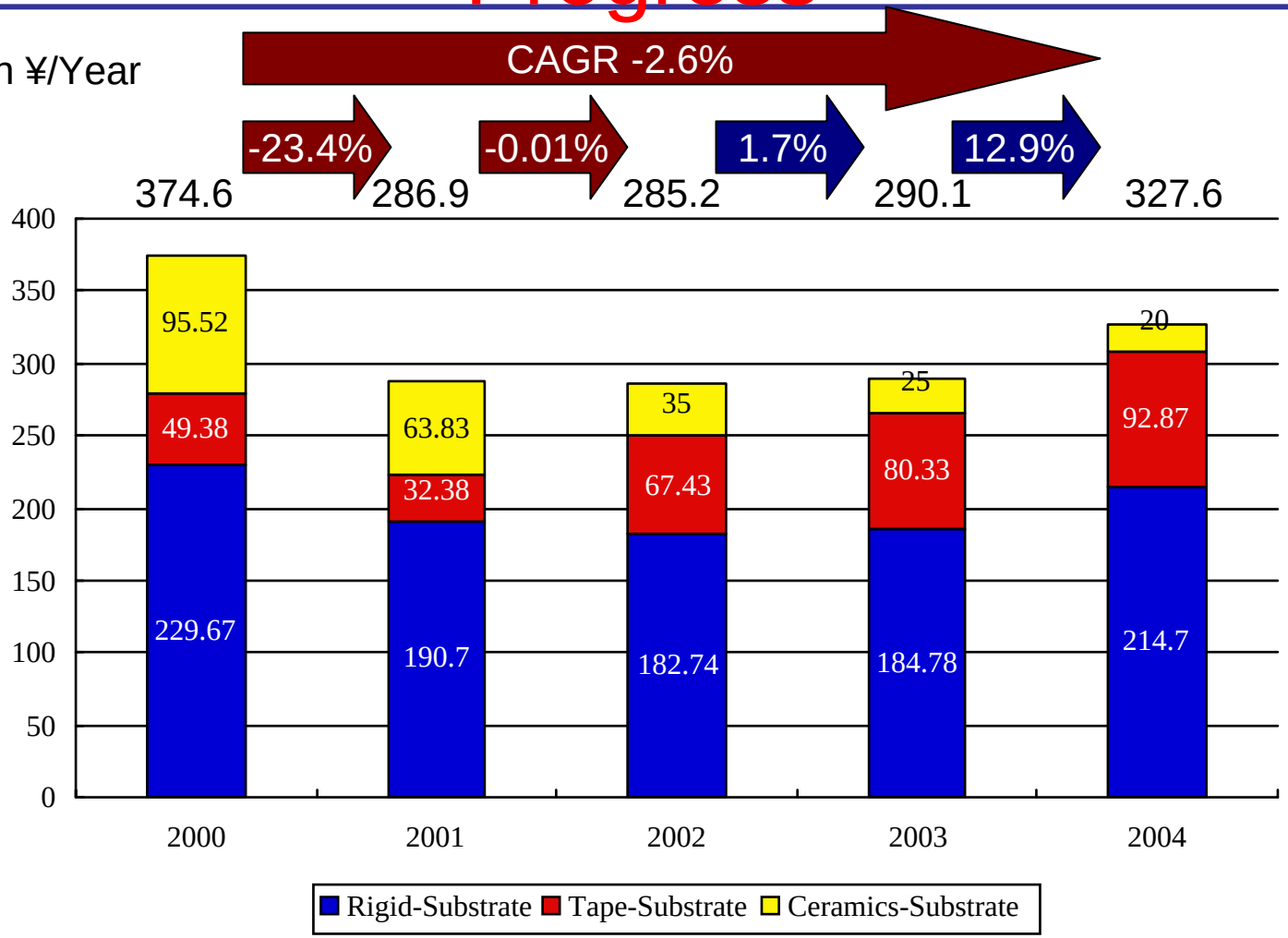
Unit: Billion ¥/Year



Source: Electronic Circuits Industry Survey Report 2004 Edition, JPCA

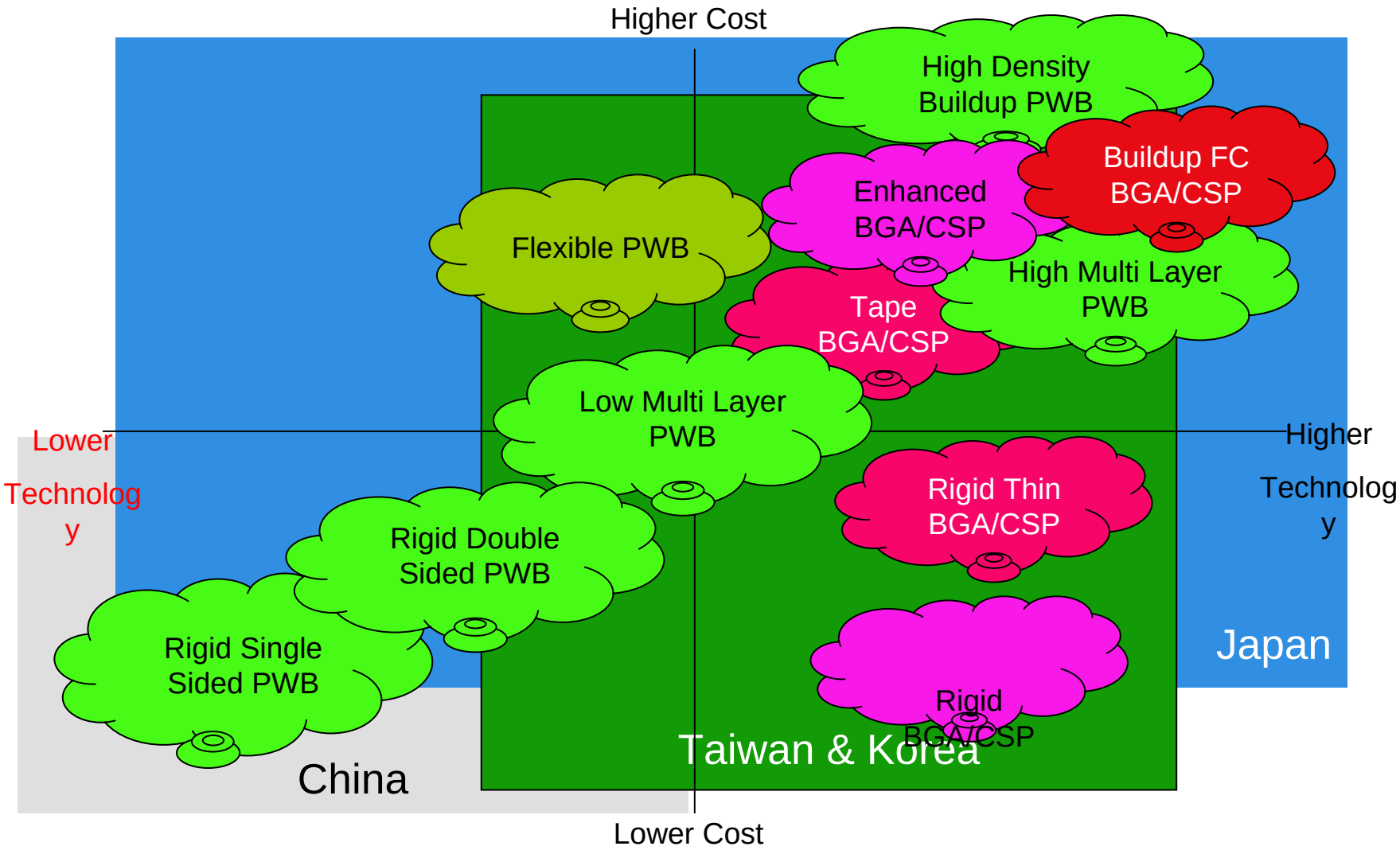
Substrate Production Amount Progress

Unit: Billion ¥/Year



Source: Electronic Circuits Industry Survey Report 2004 Edition, JPCA

PWB Products Positioning



2005 PWB Technology Roadmap

1. Rigid Printed Wiring Boards
   - Single-sided, Double-sided, Multilayer, Buildup
2. Flexible Printed Wiring Boards
   - Single-sided, Double-sided, Multilayer, Rigid-flex
3. Packaging Substrate
   - Tape, Rigid, Buildup, Ceramics
4. Common Technology
5. Difficult Challenges: Embedded Components
6. Gap Analysis

2005 PWB Technology Roadmap

Class A: Conventional Technology for volume production

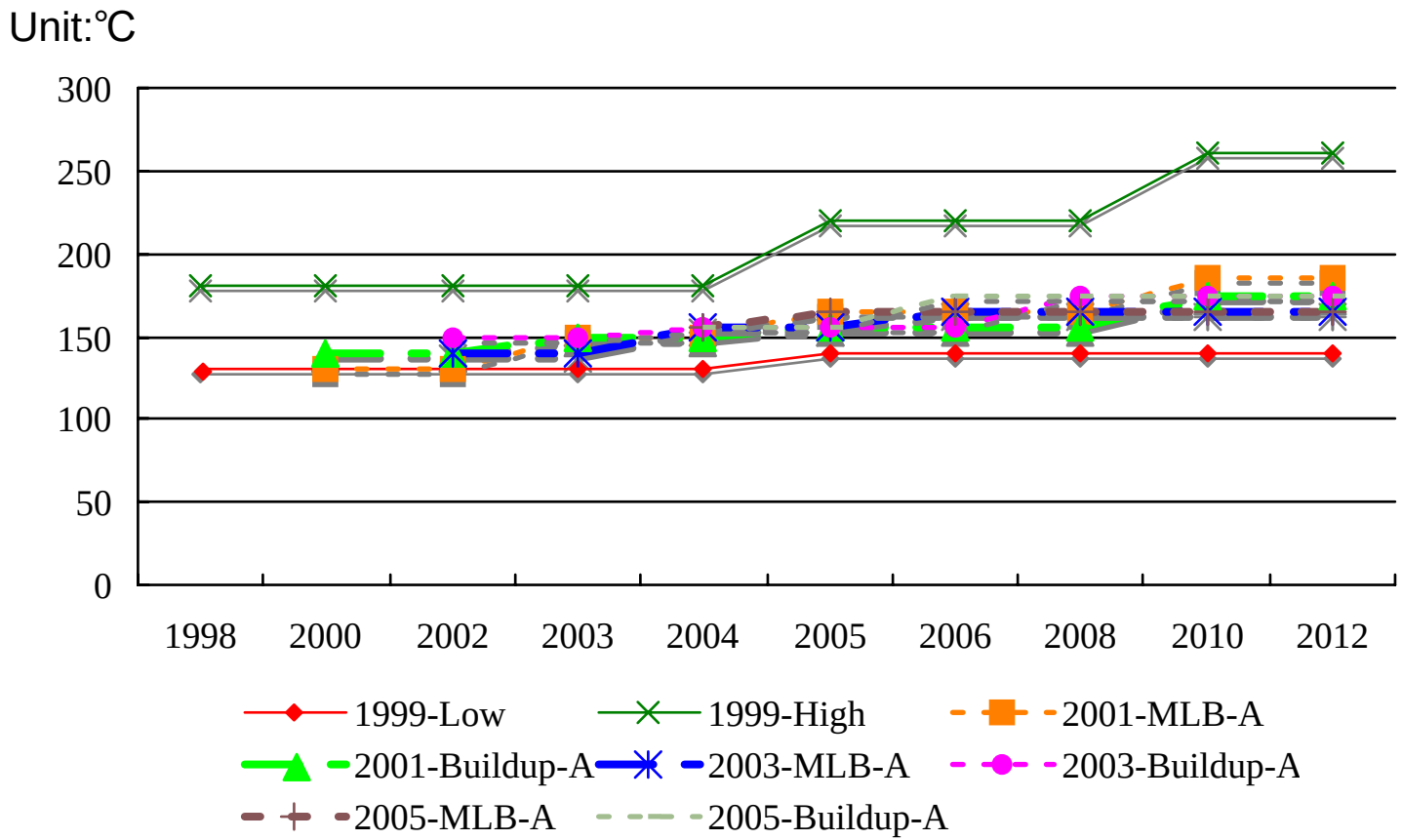
Class B: Leading Edge Technology for High-end Volume Production

Class C: State of the Art Technology for High-end Small Volume Production and Prototype

Base Material for Rigid PWB

- Glass Transition Temperature
- Dielectric Constant
- Diffusion Factor
- Co-efficient of Thermal Expansion

Glass Transition Temperature Trends



Glass Transition Temperature Trends

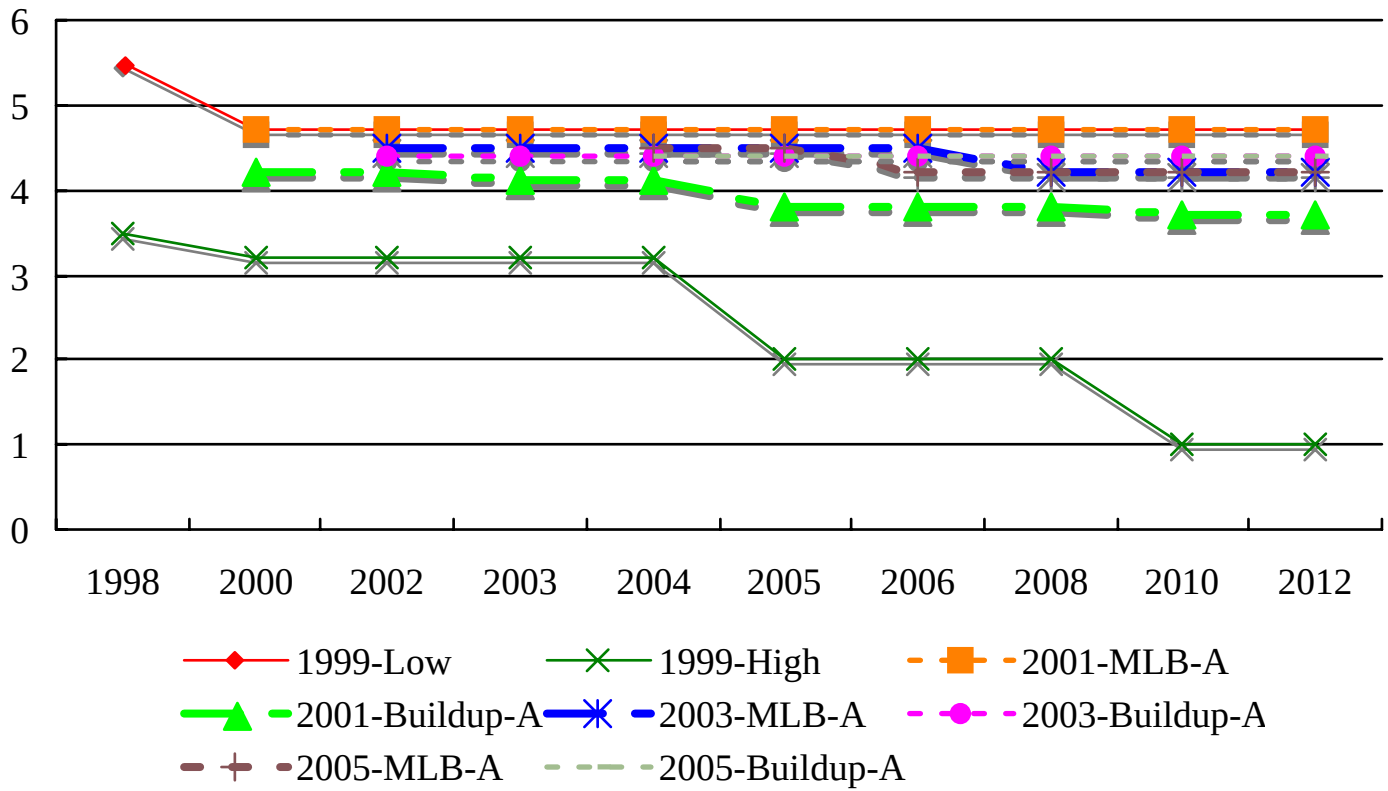
Unit:℃

Item	Description	2004	2006	2008	2010	2012	2014
Buildup	Buildup Layer	155	155	175	175	175	175
	Core Layer	155	165	165	165	165	165
Multi Layer		155	165	165	165	165	165
Double-sided		135	135	135	150	150	150
Single-sided		115	115	115	115	115	115

Class A Products

Dielectric Constant Trends

Unit: Nil



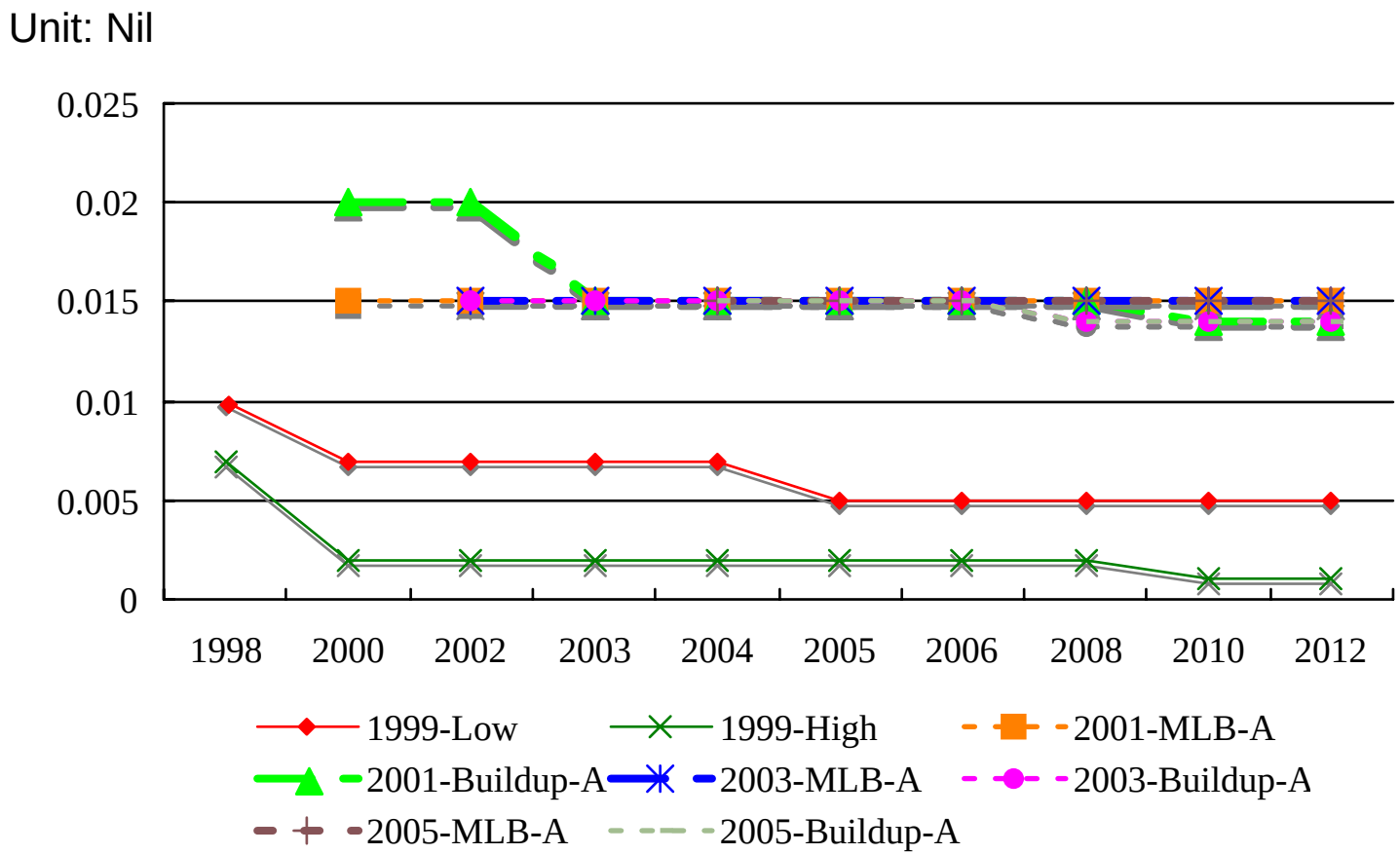
Dielectric Constant Trends

@ 1MHz

Item	Description	2004	2006	2008	2010	2012	2014
Buildup	Buildup Layer	4.7	4.7	4.7	4.7	4.7	4.7
	Core Layer	4.7	4.7	4.5	4.5	4.5	4.5
Multi Layer		4.7	4.7	4.5	4.5	4.5	4.5
Double-sided		4.7	4.7	4.7	4.7	4.7	4.7
Single-sided		4.8	4.8	4.8	4.8	4.8	4.8

Class A Products

Dielectric Loss Trends



Dielectric Loss Trends

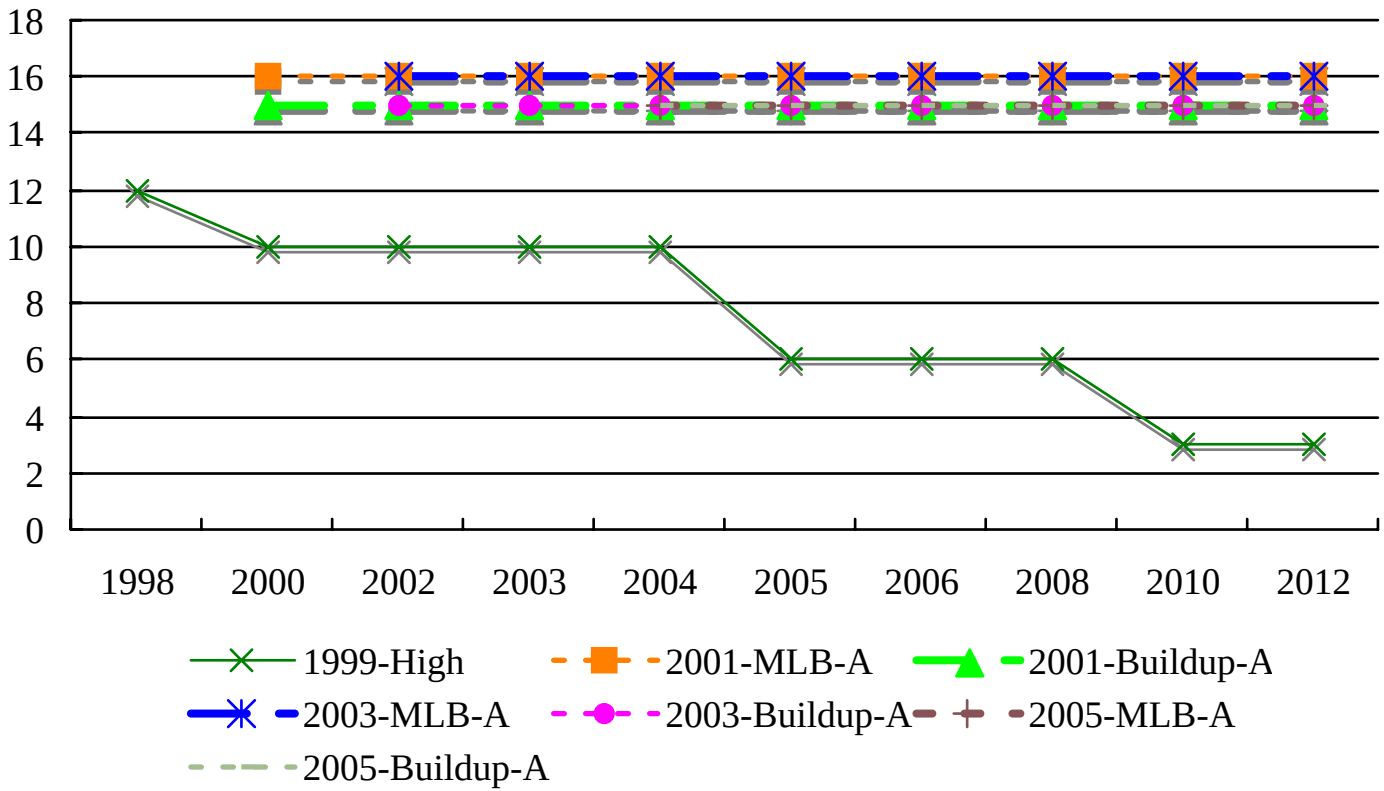
@ 1MHz

Item	Description	2004	2006	2008	2010	2012	2014
Buildup	Buildup Layer	0.015	0.015	0.014	0.014	0.014	0.014
	Core Layer	0.015	0.015	0.015	0.015	0.015	0.015
Multi Layer		0.015	0.015	0.015	0.015	0.015	0.015
Double-sided		0.018	0.018	0.018	0.018	0.018	0.018
Single-sided		0.035	0.035	0.035	0.035	0.035	0.035

Class A Products

X-Y Direction CTE Trends

Unit: Nil



X-Y Direction CTE Trends

Unit: ppm/℃

Item	Description	2004	2006	2008	2010	2012	2014
Buildup	Buildup Layer	15	15	15	15	15	15
	Core Layer	16	16	16	16	16	16
Multi Layer		15	15	15	15	15	15
Double-sided		16	16	16	16	16	16
Single-sided		60	60	60	60	60	60

Class A Products

Rigid PWB Specifications Trends

- Min. Line/Space
- Min. Via Hole Diameter/Land Diameter

Min. Line/Space Trends

Unit: micron meter

Item	Description	2004	2006	2008	2010	2012	2014
Buildup	Buildup Layer	75/75	50/50	50/50	50/50	50/50	50/50
	Core Layer	75/75	75/75	50/50	50/50	50/50	50/50
Multi Layer		100/100	100/100	75/75	75/75	75/75	75/75
Double-sided		100/100	100/100	75/75	75/75	75/75	75/75
Single-sided		125/100	125/100	100/75	100/75	100/75	100/75

Class A Products

Min. Via Hole/Land Diameter Trends

Unit: micron meter

Item	Description	2004	2006	2008	2010	2012	2014
Buildup	PTH	200/450	200/450	150/300	150/300	150/300	150/300
	IVH	200/400	200/400	125/325	125/325	125/325	125/325
	MVH	100/250	100/250	80/200	80/200	80/200	80/200
Multi Layer PTH		200/400	200/400	150/350	150/350	150/350	150/350
Double-sided		300/500	250/450	250/400	200/350	200/350	150/300
Single-sided		500/1000	500/1000	500/1000	500/1000	500/1000	500/1000

Class A Products

Base Material for Flexible PWB

- Glass Transition Temperature
- Dielectric Constant
- Diffusion Factor
- Co-efficient of Thermal Expansion

Glass Transition Temperature Trends

Unit:℃

Item	2004	2006	2008	2010	2012	2014
Class A	70	75	75	80	80	80
Class B	105	120	120	130	130	130
Class C	120	130	140	150	150	150

Adhesive Material Property

Dielectric Constant Trends

@ 1MHz

Item	2004	2006	2008	2010	2012	2014
Class A	4.0	4.0	4.0	4.0	4.0	4.0
Class B	3.2	3.2	3.2	3.2	3.2	3.2
Class C	3.0	3.0	3.0	3.0	3.0	3.0

Dielectric Loss Trends

@ 1MHz

Item	2004	2006	2008	2010	2012	2014
Class A	0.03	0.03	0.03	0.03	0.03	0.03
Class B	0.01	0.01	0.01	0.01	0.01	0.01
Class C	0.007	0.007	0.007	0.007	0.007	0.007

X-Y Direction CTE Trends

Unit: ppm/℃

Item	2004	2006	2008	2010	2012	2014
Class A	27	20	20	20	20	20
Class B	16	16	16	12	12	12
Class C	16	12	12	12	12	12

Class A Products

Flexible PWB Specifications Trends

- Min. Line/Space
- Min. Via Hole Diameter/Land Diameter

Min. Line/Space Trends

Unit: micron meter

Item	Description	2004	2006	2008	2010	2012	2014
Multi Layer	Outer Layer	75/75	60/60	60/60	40/40	40/40	40/40
	Inner Layer	70/70	60/60	60/60	50/50	50/50	50/50
Double-sided		75/85	75/85	60/70	60/70	50/60	50/60
Single-sided		50/60	40/50	40/50	30/40	30/40	30/40

Class A Products

Min. Via Hole/Land Diameter Trends

Unit: micron meter

Item	Description	2004	2006	2008	2010	2012	2014
Multilayer	PTH	300/500	250/450	250/450	200/400	200/350	150/400
	IVH	300/550	200/450	200/450	150/400	150/350	100/300
	Surface Via	125/300	125/275	100/250	100/250	100/250	100/250
Double-sided		150/350	150/350	100/300	100/300	100/300	100/300
Single-sided		150/350	150/350	100/300	100/300	100/300	100/300

Class A Products

Base Material for Packaging Substrate

- Glass Transition Temperature
- Dielectric Constant
- Diffusion Factor
- Co-efficient of Thermal Expansion

Glass Transition Temperature Trends

Unit:℃

Item	Description	2004	2006	2008	2010	2012	2014
Buildup	Buildup Layer	180	180	200	200	200	200
	Core Layer	200	200	210	210	210	210
Rigid		200	200	210	210	210	210
Tape		280	280	280	280	280	280
Ceramics		N/A	N/A	N/A	N/A	N/A	N/A

Class A Products

Dielectric Constant Trends

@ 1MHz

Item	Description	2004	2006	2008	2010	2012	2014
Buildup	Buildup Layer	3.4	3.4	3.4	3.0	3.0	3.0
	Core Layer	4.0	4.0	4.0	4.0	4.0	4.0
Rigid		3.7	3.7	3.3	3.1	3.0	3.0
Tape		3.5	3.5	3.5	3.5	3.5	3.5
Ceramics		4 - 20	4 - 20	4 - 20	4 - 20	4 - 20	4 - 20

Class A Products

Dielectric Loss Trends

@ 1MHz

Item	Description	2004	2006	2008	2010	2012	2014
Buildup	Buildup Layer	0.02	0.02	0.015	0.015	0.015	0.015
	Core Layer	0.013	0.013	0.013	0.013	0.013	0.013
Rigid		0.015	0.014	0.012	0.009	0.009	0.009
Tape		0.001	0.001	0.001	0.001	0.001	0.001
Ceramics		0.0005	0.0005	0.0005	0.0005	0.0005	0.0005

Class A Products

X-Y Direction CTE Trends

Unit: ppm/°C

Item	Description	2004	2006	2008	2010	2012	2014
Buildup	Buildup Layer	15	15	12	12	12	12
	Core Layer	13	11	11	11	11	11
Rigid		14	14	13	13	12	12
Tape		20	20	16	16	16	16
Ceramics		4 - 12	3 - 12	3 - 12	3 - 12	3 - 12	3 - 12

Class A Products

Packaging Substrate Specifications Trends

- Min. Line/Space
- Min. Via Hole Diameter/Land Diameter

Min. Line/Space Trends

Unit: micron meter

Item	2004	2006	2008	2010	2012	2014
Buildup	40/40	30/30	30/30	20/20	20/20	15/15
Rigid	50/50	40/40	35/35	35/35	35/35	35/35
Tape	25/25	20/20	20/20	15/15	15/15	15/15
Ceramics	75/75	75/75	50/50	50/50	50/50	50/50

Class A Products

Min. Via Hole/Land Diameter Trends

Unit: micron meter

Item	Description	2004	2006	2008	2010	2012	2014
Buildup	Core PTH	100/150	100/150	100/140	100/140	100/140	100/140
	MVH-Laser	60/110	60/110	40/80	40/80	40/80	30/70
	MVH-Photo	80/120	80/120	80/120	80/120	80/120	80/120
Rigid		75/230	75/180	50/170	50/170	50/170	50/170
Tape		80/130	80/130	50/90	50/90	50/90	30/60
Ceramics		75/75	75/75	75/75	50/50	50/50	50/50

Class A Products

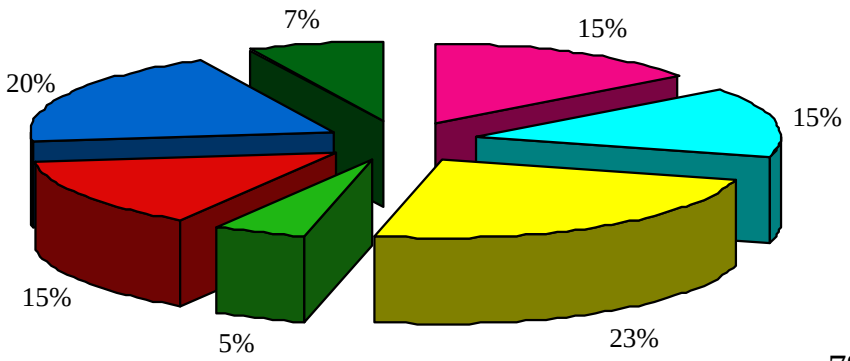
Embedded Components

- Embedded Active Devices
- Embedded Passive Devices
  - Resistors
  - Capacitors
  - Inductors

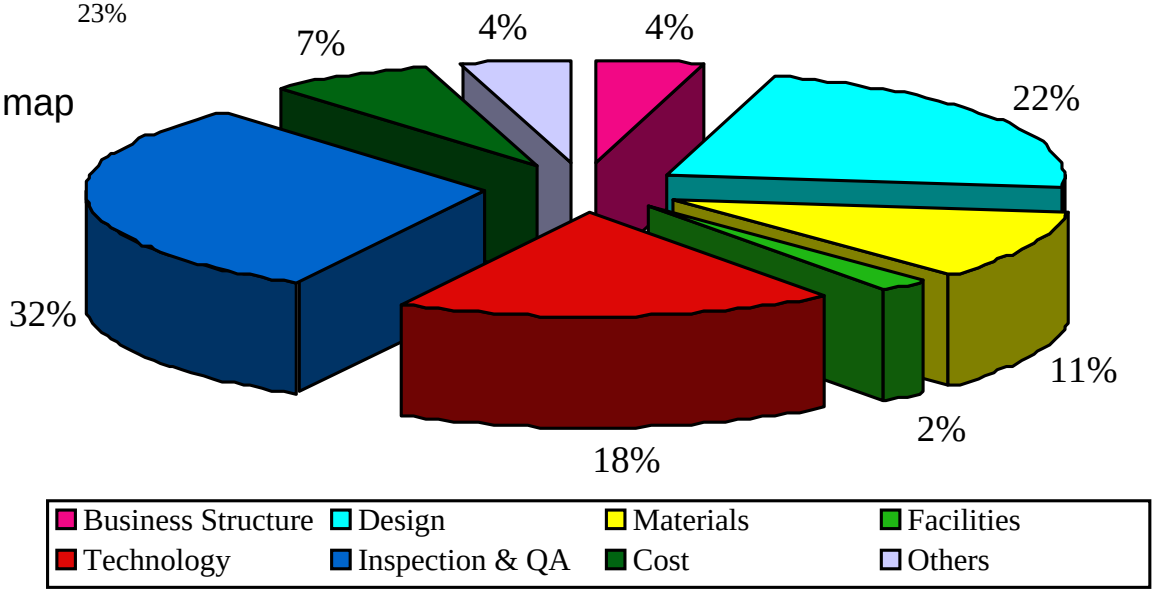
Embedded Components

Color	Code	Description
	A	In Volume Production
	B	Prototype Production for Customers
	C	Prototype Production for Sale Promotion
	D	Prototype Production for Internal Evaluation
	E	R & D for Production Process
	F	Investigation on Materials & Production Process
	G	Recognized Future Useful Technology But No Action
	H	No Intention to R & D for Embedded Technologies
	I	Doesn't Understand Well

Questions for Embedded PWBs



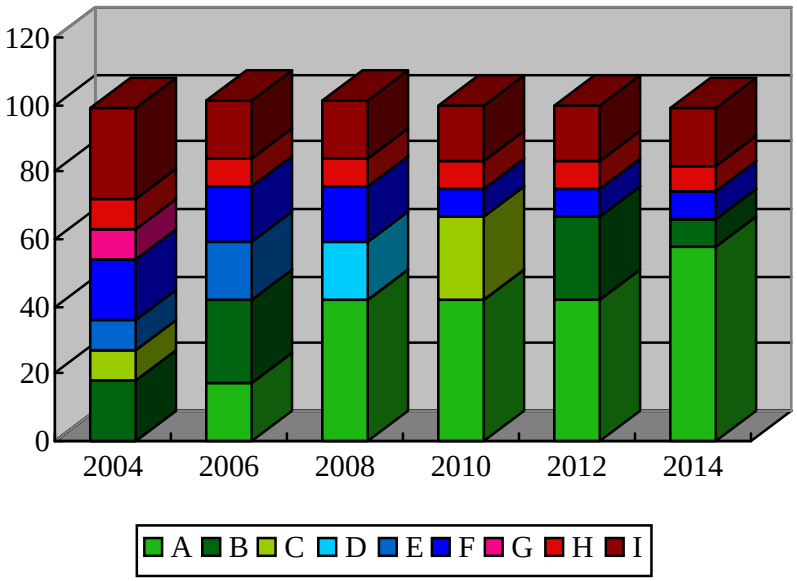
2003 Jisso Technology Roadmap



2005 Jisso Technology Roadmap

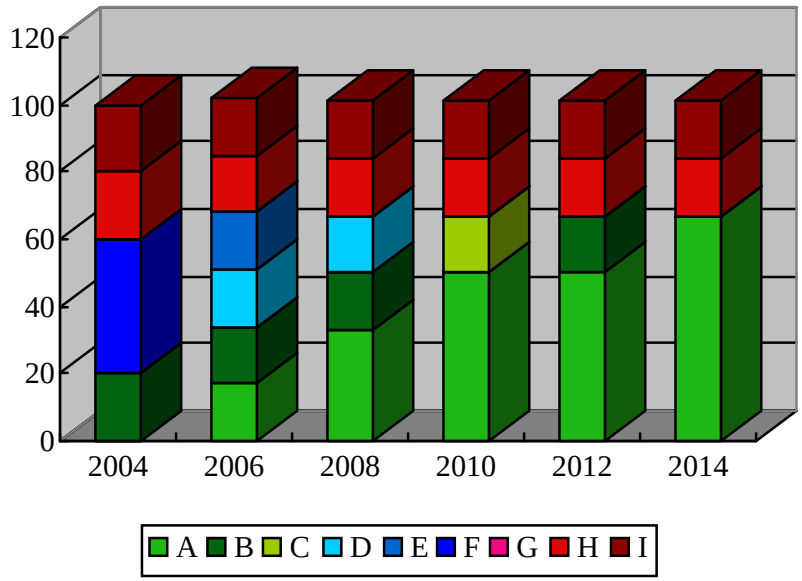
Embedded Active Devices in Buildup

Unit: # of Answers



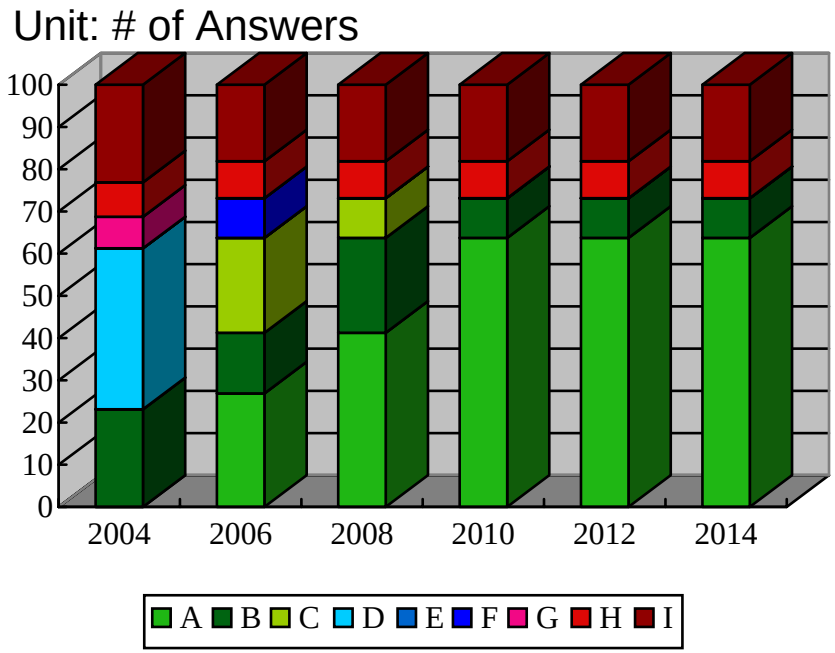
Buildup Mother Board Embedded

Unit: # of Answers

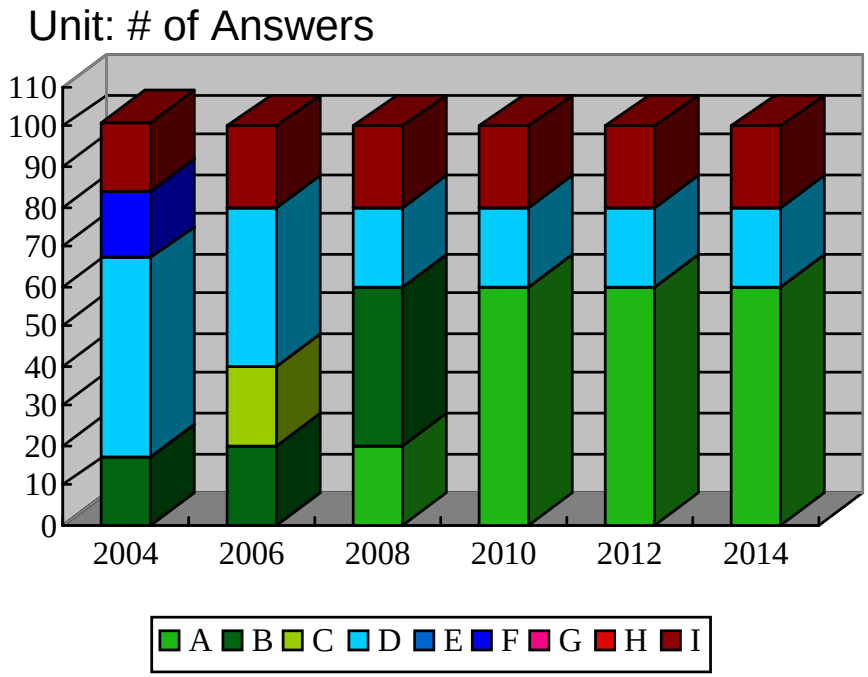


Buildup Substrate Embedded

Embedded Chip Resistor to Buildup

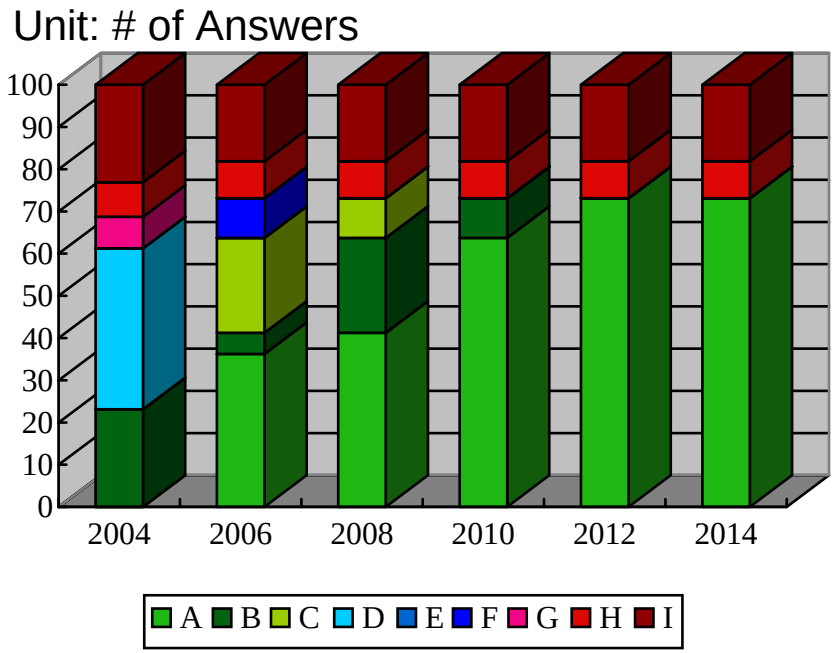


Buildup Motherboard

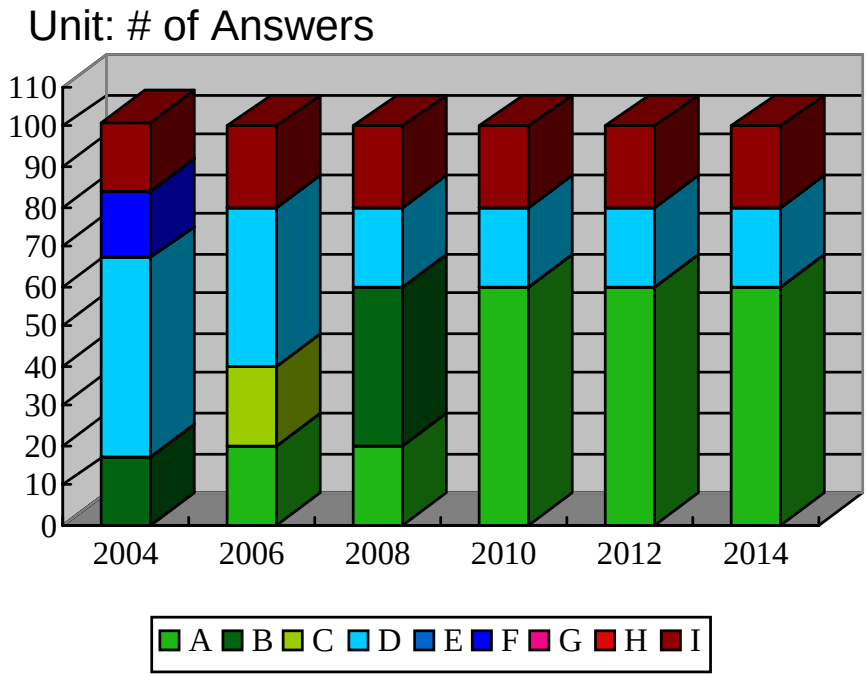


Buildup Substrate

Embedded Chip Capacitor to Buildup

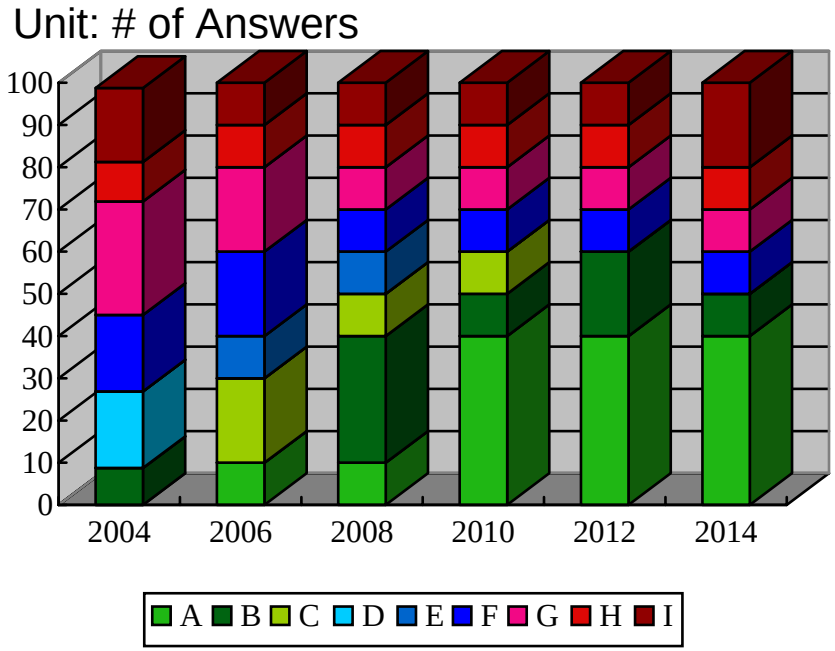


Buildup Motherboard

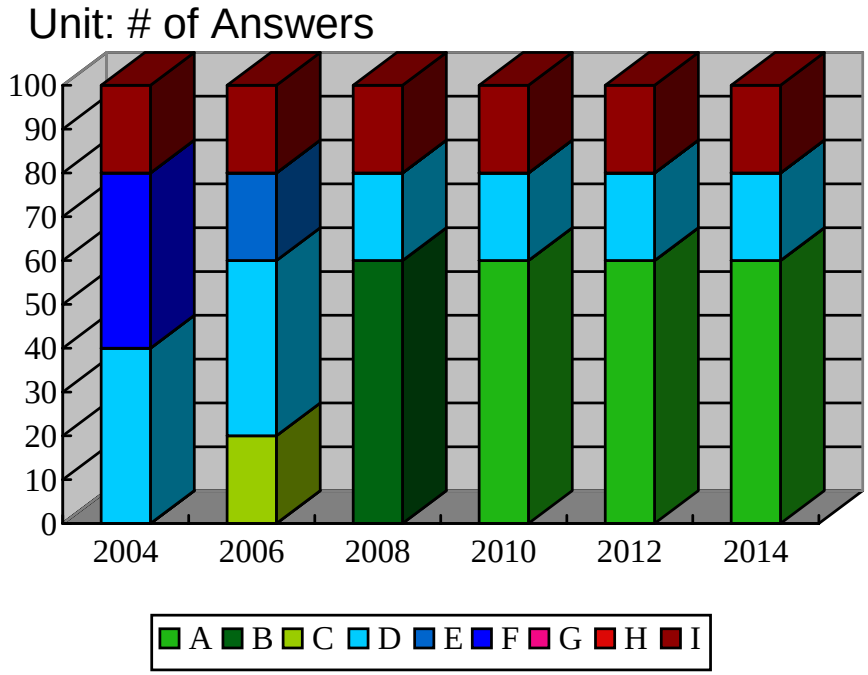


Buildup Substrate

Embedded Chip Inductor to Buildup

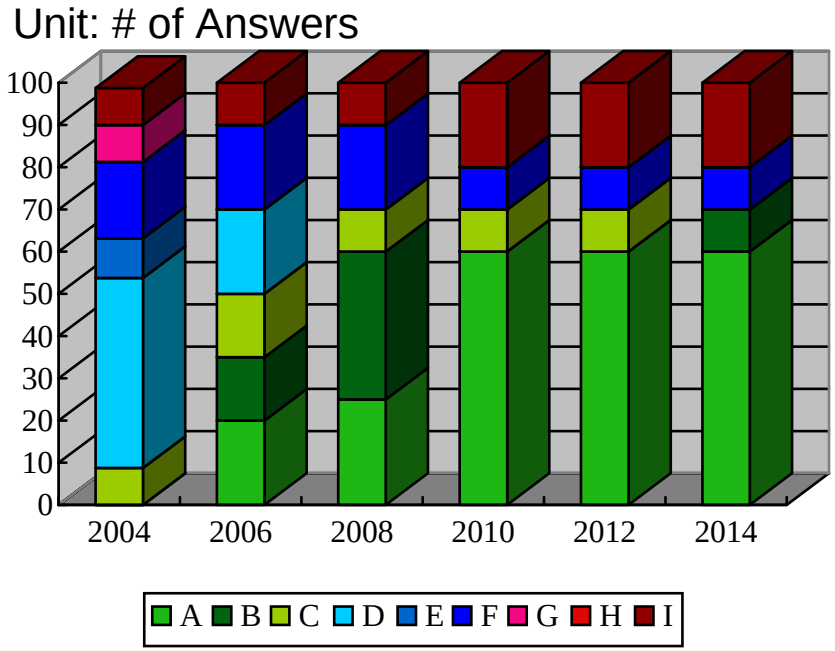


Buildup Motherboard

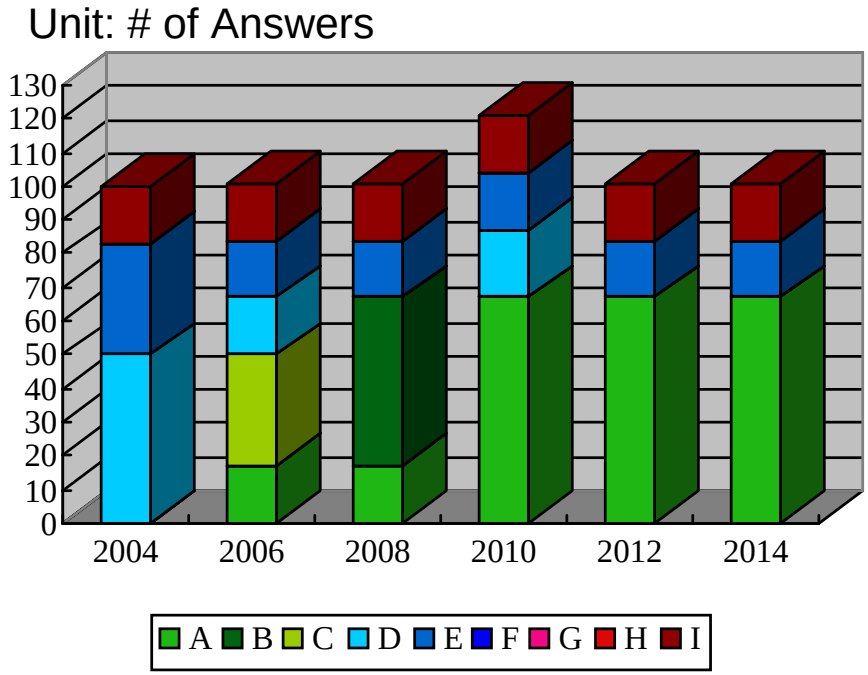


Buildup Substrate

Embedded Formed Resistor to Buildup

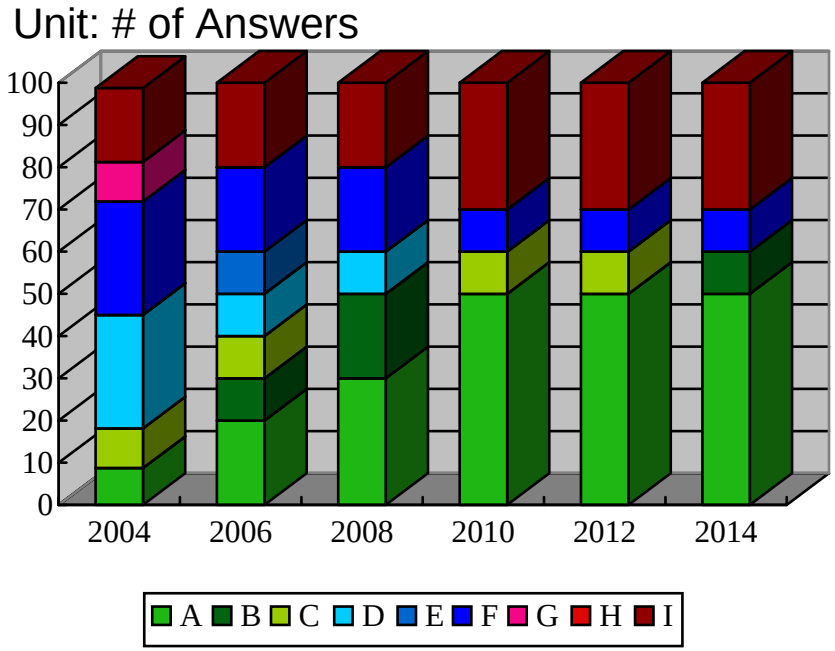


Buildup Motherboard

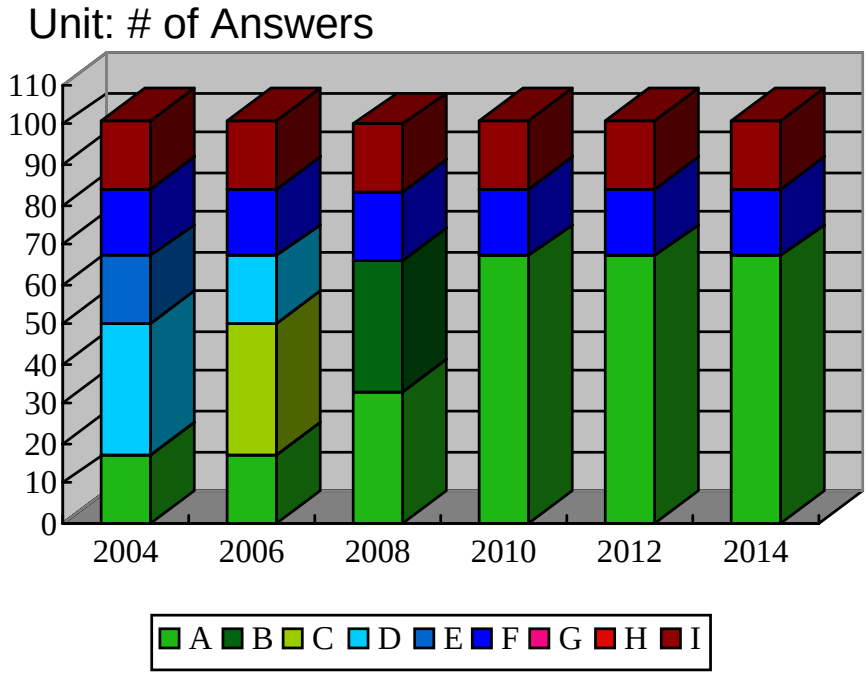


Buildup Substrate

Embedded Formed Capacitor to Buildup

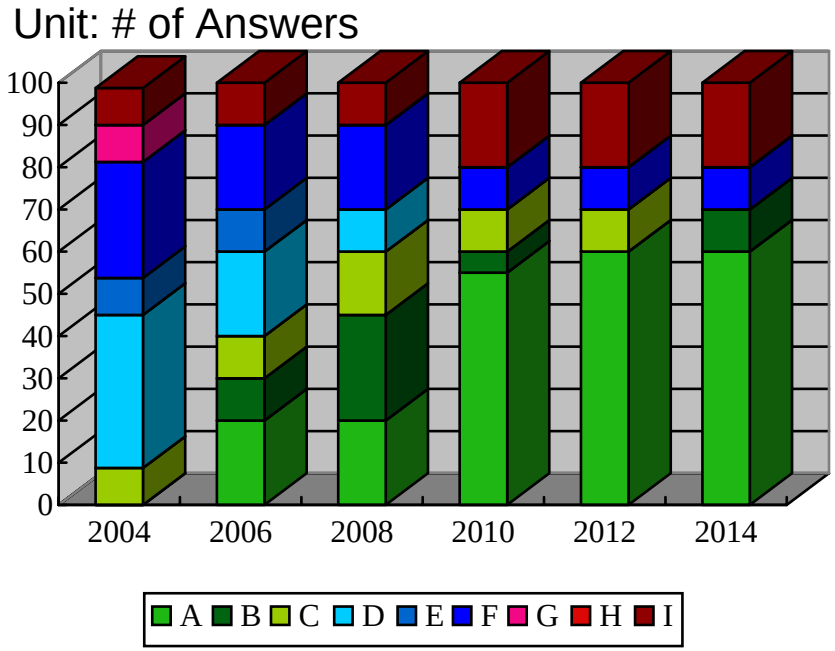


Distributed Capacitor to Buildup Motherboard

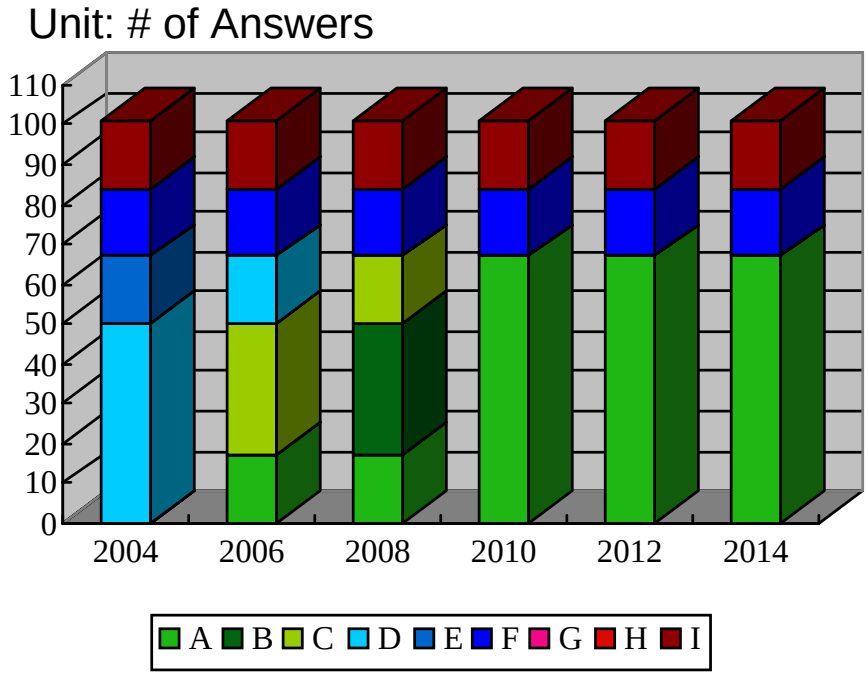


Distributed Capacitor to Buildup Substrate

Embedded Formed Capacitor to Buildup

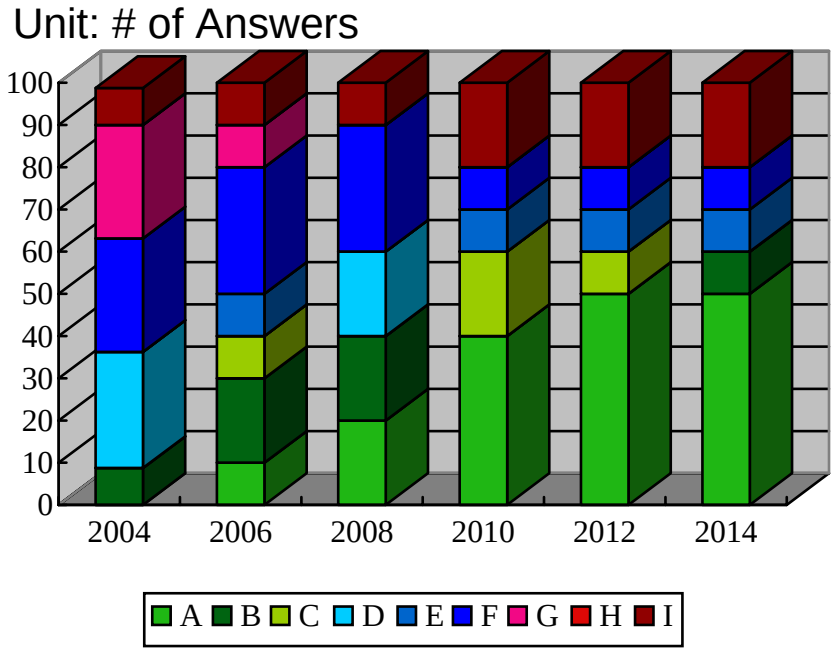


Individual Capacitor to Buildup Motherboard

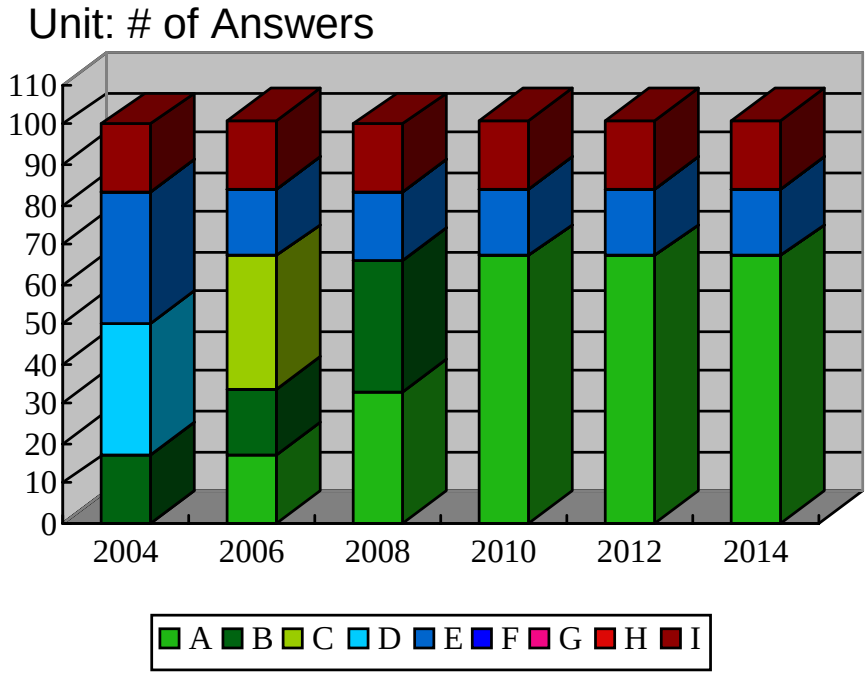


Individual Capacitor to Buildup Substrate

Embedded Formed Inductor to Buildup



Buildup Motherboard



Buildup Substrate

Challenges on PWBs

1. Limitation of Fine Line/Space Width
   - Conventional Technology Limitation at <20micron Line/Space and Via Hole Diameter
   - Increasing Additive Process and/or Semiconductor-like Process Requirements
2. Adoption for Signal Integrity
   - Shortage of Electronics Engineer in PWB Industry
   - Increasing Capital Investment for Embedded Components PWB
   - Modeling & Simulation are necessary for Embedded Components and SiP
   - Design for Manufacturing & Design for Test needs to establish
3. Adoption for Interconnection Reliability
   - Modeling & Simulation for Total Package Structure, especially for Low k & Cu Device
   - Improved Insulation material to adopt Reliability as well as Signal Integrity
   - Integration into Packaging Substrate to release Mother board density & Cost

Summary

- PWB products began to differentiate in 2 categories by the correspondence to complexity such as SiP, EAD and cost oriented type
  - Buildup Motherboard, FPC and packaging substrate is growing area
  - Conventional Motherboard production shift from Japan to Asian countries
- SiP can get a market opportunity early, and can save plant investment
- An active component embedded printed wiring board has the potential solution which improves the function of the unit area of SiP
- Failure at a design stage of the embedded component PWB isn't forgiven. Therefore, the maintenance of the design database and the maintenance of the modeling & simulation environment are necessary.
- Infrastructural enhancement of materials, manufacturing technologies, quality assurance and patent corresponding to High speed Mother board, SiP and the components embedded PWB are necessary.

Thank You Very Much!!

- Thank you very much for your attention
- Japan Jisso Technology Roadmap 2005 Edition will publish in June, 2005. Please Wait!!