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New Circuit Formation Technology for High Density PWB

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Abstract

To meet future requirements for PWBs, various technologies of processes, materials and tools of PWBs have been discussed. Especially important are technologies of circuit formation for high-end PWBs. Industrially the circuit formation method for fine pattern has been changed, in these years, from the subtractive process to the Semi-Additive Process (SAP). SAP can form finer circuits because it doesn't cause side etching that is the problem of subtractive method. However the flash etching process of SAP causes other problems such as short defects due to residual seed metal layer between circuits, circuit etching and circuit delamination due to etching. Also, because of the roughness of the insulator surface that the circuits are formed on, there are not only difficulties for fine circuits formation but loss of an electrical property.

In this paper, a new circuit formation method is discussed to overcome the problems that the flash etching process of SAP causes. It does not need flash etching process therefore it can form finer patterns. The capability of this fine line circuit formation depends upon the photo pattern resist resolution and was confirmed to perform well at L/S(Line/Space) = 10/10um or less. Also the circuit pattern is buried in the insulator layer and is planer with the insulator surface, therefore the circuits have high peel strength with insulator and there is less damage by manufacturing equipment or handling between processes. This method is applicable to build up PCBs and FCPs as a circuit formation technology that meets future requirements.

Introduction

For the evolution of electronic devices that is faster, smaller and more multi-functional but also more cost effective, various technologies of PWBs are required for higher density. Samsung Electro-Mechanics Co., Ltd. manufactures many kind of PWBs like HDI for mobile phones, digital still cameras, etc., BGA packages, FC BGA packages. To meet future requirements especially for FCBGA, it is getting difficult to manufacture products of FC BGA because of its high density. Circuit formation is one of the processes that needs to make rapid progress for the high density.

Subtractive process and Semi-Additive Process (SAP) as circuit formation process have both been discussed to improve its high density.[1,3] But the subtractive process has a basic problem of side etch due to chemical etching, and SAP has limitations due to flash etching process. The Flash etching process of SAP causes problems such as circuit etching, under cut at the circuit bottom as shown in Figure 1 and seed layer residue if flash etching is insufficient. As the seed layer is usually copper that is the same as the circuits, the flash etching process etches not only seed layer but also the circuits. Therefore circuit width and thickness have to be wider and thicker than final dimension before flash etching to keep design rule after flash etching. For example, after undercut the 20um circuit's bottom separation is 11.2um (5.2+6.0um) as shown in Figure 1 giving an adhered width of only 8.8um of the 20um pitch. This is considered to be inadequate to provide enough peel strength for the 20um circuits. When circuits become finer, undercut will be a bigger problem and manufacturing yield will be lower because of damage in processing by the manufacturing conveyors or rollers. For these reasons, a circuit formation technology based on new concepts is needed for finer line circuit formation and to settle these technology difficulties.

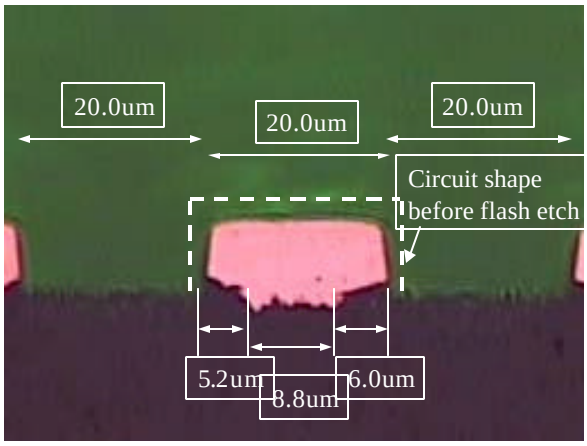


Figure 1 Circuit etching and Undercut by Flash Etching of Semi-Additive Process (SAP)

New Idea for Fine Line Circuit Formation

It was believed that for finer circuit formation a process that doesn't need flash etching process will not cause undercutting of circuits and circuit etching, and the structure of the circuits can be buried in the insulator to protect them from damage by contact during processing. Figure .2 shows the process flow of new circuit formation technology.

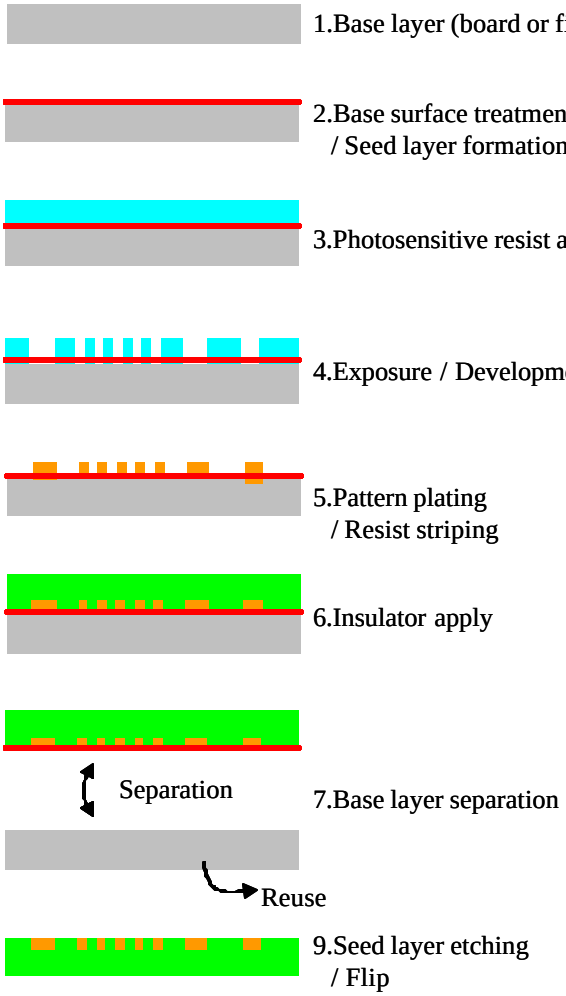


Figure 2 Process Flow

First of all, a base layer that is a rigid board or a film is prepared. Secondly, a surface treatment on the base layer is performed. Then the surface of base layer is metallized to provide a seed layer. A photosensitive resist is applied on the surface and circuits are formed with exposure and development processes. The photosensitive resist is used as a pattern plating resist. Then Cu pattern plating is performed on the seed layer. After pattern plating, the photosensitive resist is stripped then a surface treatment of Cu pattern is performed to get good adhesion to the insulator layer. the insulator is applied with liquid or film resists on the circuits and the base layer is separated. This base layer can be reused as a base layer again after the separation. After base layer separation the seed layer that remains on the circuits are etched out.

Compensation of plating, shown in Figure 1 is unnecessary, as resolution of circuits is decided by the resolution of the photosensitive resist which can make finer patterns than SAP circuits. And the structure of circuit board is unique in that the circuits are buried in the insulator and will see little damage in process. Note that circuit etching is not caused by layer etching with this process. This process is named CTP (Circuit Transfer Process) because circuits are transferred in the insulator using the base layer. In discussions below the CTP will be tested to determine if this process is suitable for fine line formation technology.

Circuit Formation on Base Layer

Surface treatment of the base layer is the one of key processes in this technology. The purpose of this surface treatment is to get enough adhesion with the seed layer and to release the base layer from substrate at base layer separation process. This surface treatment is available for both rigid board and flexible film as a base layer.

For better resolution and adhesion of the photosensitive resist on seed layer, a proper surface treatment to seed layer should be performed on its surface. Several surface treatments (condition A, B, C, D) were examined to check fine line formation capability on the seed layer. Figure 3 shows the result of the capability test. Condition A or B gave the best adhesion and resolution up to L/S=8/8 on the seed layer as a surface treatment condition. Figure 4 shows an SEM picture of Resist/Space = 8/8um after development. No residual resist on the copper surface was found by the SEM analysis, L/S = 8/8um pattern can be formed after pattern plating in this case with no defects.

Cu pattern plating is performed with conventional Cu plating process using the seed layer that is formed on the base layer. Thickness should be uniformly well controlled by adjusting the plating equipment and current density. It is also important to control the flow of plating solution in the plating bath for fine patterns like L/S = 10/10um or less.

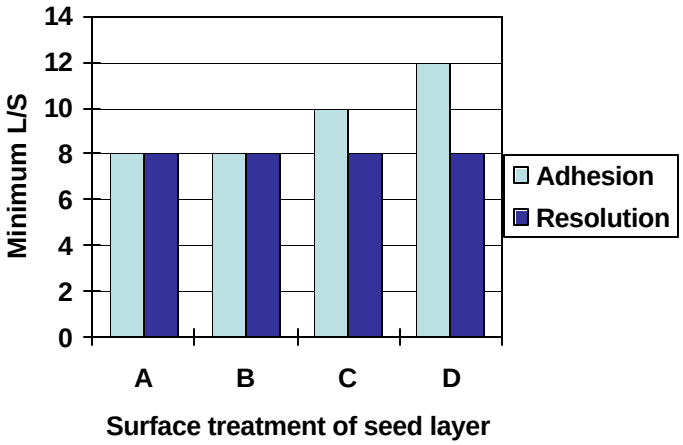


Figure 3 – Photosensitive Resist Capability

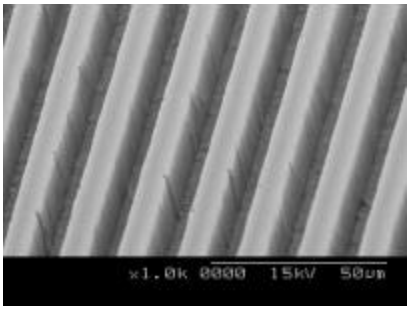


Figure 4 – Photosensitive Resist Circuits after Development

Insulator Formation

Cu surface treatment is required to get good adhesion of insulators on Cu circuits. A conventional Cu surface treatment process is used as the surface treatment, which is a micro roughening process by chemical etching. Etching volume should be minimized so as not to cause circuit etching and undercut of Cu circuit, otherwise compensation of plating width and plating thickness shown in Figure 1 has to be designed in or the circuits might be peeled out due to undercut at the bottom of Cu circuit. Insulators that use conventional materials and processes of PWB are also useable in CTP. After insulator lamination, the base layer is separated. The separation technology that was developed by Samsung Electro-Mechanics is unique compared with any other technology. After base layer separation, the seed layer is etched by etching solution from the backside of the insulator layer. When a dissimilar metal is used as a seed layer, it is possible to etch seed layer selectively. This makes the surface of the Cu circuits and insulator flat and a flat surface structure for the substrate.

Figure 5 shows SEM images of a L/S=10/10um circuit that were observed from circuit side after seed layer etching. Both the insulator and Cu surface are flat and no residual seed layer was observed on the surface. This observation shows selective seed layer etching was performed using dissimilar metal as the seed layer to Cu circuits, i.e. the seed layer was etched using an etching solution that works through bimetallic corrosion. Though not confirmed yet it's supposed that this flat substrate surface has advantages in the packaging processes.

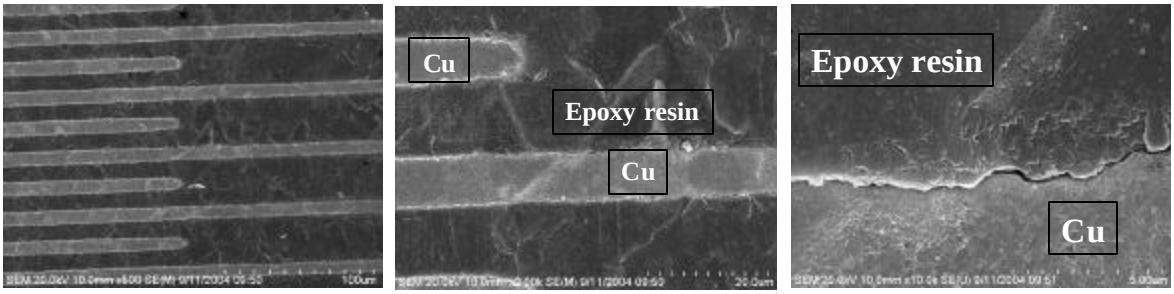
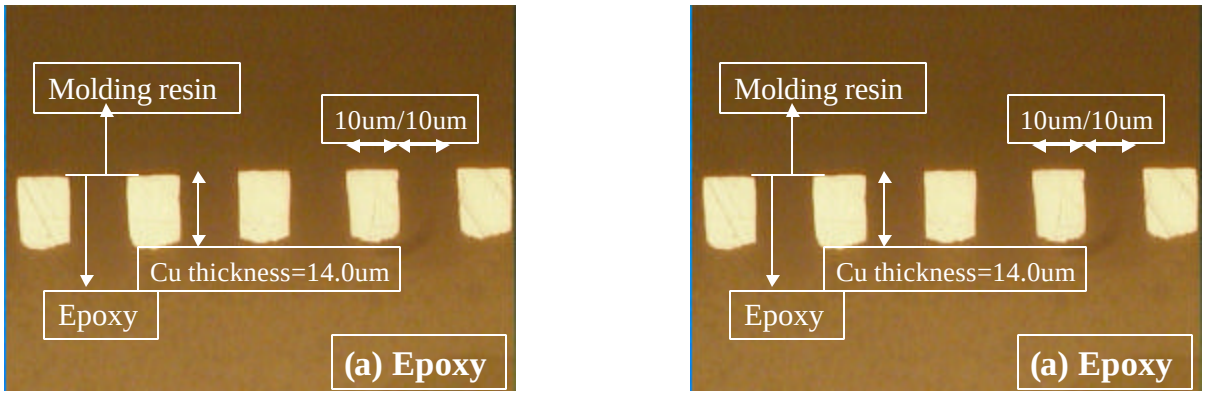


Figure 5 – SEM Images of Top View of 10/10 um Circuit with CTP after Seed Etching

Epoxy type build up insulator, epoxy RCC (Resin Coated Copper) reinforced with glass cloth type and epoxy RCC reinforced with aramid, LCP (Liquid Crystal Polymer) film were tested as insulators. Figure 6 shows X-sectional pictures of L/S=10/10um after seed etching. (a) shows epoxy lamination and (b) shows LCP lamination. Voids and delamination were checked by xsection and surface observation, and all insulator materials showed good lamination without voids or delamination in 10um spaces of lines.



(a) Epoxy laminated (b) LCP laminated

Figure 6 – X-sectional pictures after Seed Layer Etching

Advantage of CTP

Figure 7 shows the comparison of X-sectional structures of SAP and CTP. Only a bottom side of Cu circuit adheres on the insulator surface with SAP, whereas three sides of Cu circuit adhere in the insulator and circuit is buried in the insulator with CTP. It's supposed that CTP circuit adhesion adheres stronger than SAP circuit. This is a structural advantage of CTP with respect to circuit adhesion.

Under the assumption that the adhesion with the insulator is same at circuit bottom and circuit wall, and that Cu peel strength is 1.0kg/cm, line width is 10um, and thickness is 15um, a simulation of Cu peel strength is shown in Figure 8. Cu peel strength of CTP is always 3.0g higher at any line width than that that of SAP. This 3.0g is the part of adhesion with the circuit wall. Figure 9 shows the peel strength ratio of CTP / SAP. In cases of smaller, the peel strength ratio is notably higher. The curve has a point of inflection at about 5um of circuit width and the asymptote is $x=0$. This suggests that CTP has a bigger advantage in circuit peel strength compared with SAP when the circuits are finer especially for circuit widths of less than 10um.

Figure 10 shows L/S=10/8um (18um pitch) that was formed by CTP described in this paper. If the photosensitive resist has better capability for higher density design, that is less than 8/8um (16um pitch), it is supposed that finer circuit formation is possible. Therefore the feasibility of fine line formation with CTP is considered higher than that with SAP.

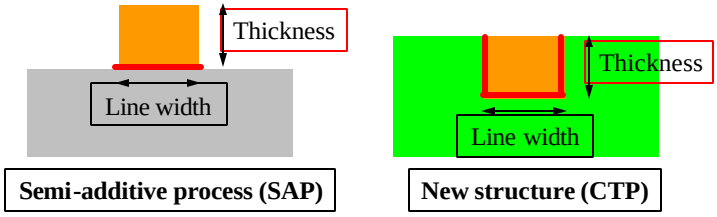


Figure 7 Circuit Structure Comparisons of SAP and CTP

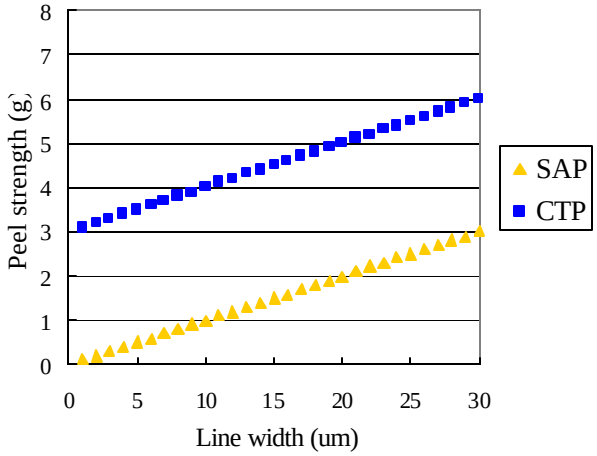


Figure 8 – Simulation of Cu Circuit Peel Strength (at Line Width: 10 um, Thickness: 15 um, Peel Strength: 1.0kg/cm)

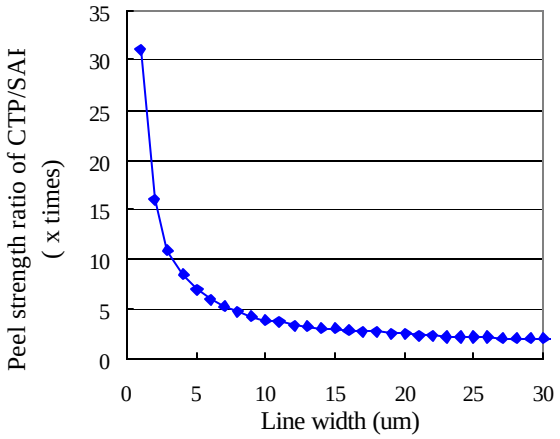


Figure 9 – Simulation of Cu Circuit Peel Strength Ratio of CTP/SAP (at Line: 10 um, Thickness: 15 um, Peel Strength: 1.0kg/cm)

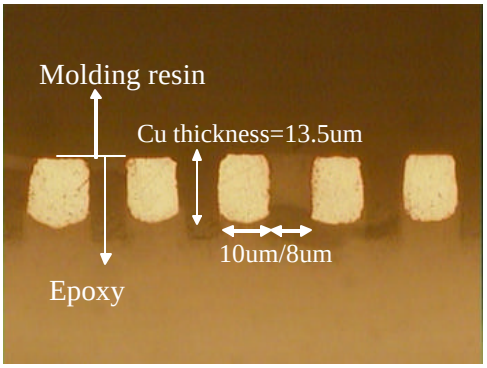


Figure 10 – X-sectional Picture of 10/8 um (18 um pitch) circuit by CTP (Circuit Transfer Process)

Outlook and Subject of CTP for the Future

Feasibility and advantages of CTP were described in this paper. But the following items should be confirmed for the further possibility of CTP:

1. Reliability data to show CTP performance.
2. Surface treatment of Cu circuit not to etch circuit for finer pattern.
3. Need development of build up substrate with CTP.
4. Investigation of cost estimation of CTP for mass production.
5. Double side process to reduce manufacturing cost.
6. Process optimization for mass production.

Conclusion

The following things were confirmed in this paper:

1. CTP has advantages in forming fine line circuits because there is no flash etching process.
2. CTP is available for various insulators.
3. CTP has a flat surface structure for both circuits and insulator
4. Most conventional processes are available for CTP
5. CTP is the new circuit formation technology for high density PWB.

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