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# Understanding the Impact of Accelerated Temperature Profiles on Lead-Free Soldering

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**Abstract**
Traditional reflow profiles for lead-free soldering typically require longer processing times due to elevated peak temperatures and flux activation times defined by solder paste suppliers. These profiles become particularly challenging when a wide variety of packaging types are integrated within a single circuit design. Further difficulty is presented when product designs with high thermal mass, such as heat slugs and metal substrates, are processed. These designs create large thermal gradients throughout a circuit assembly and add further complexity to finding an "optimal" profile window. All of these issues create a significant increase in reflow processing times for lead-free soldering.

This paper investigates these increased processing times required for high volume manufacturing of lead-free electronics. A study of typical process capacity and real throughput capacity is presented. The study evaluates high volume electronics manufacturing ranging from small circuit assemblies (e.g. cell phone) to large circuit assemblies (e.g. automotive and computers) and investigates a series of "best" reflow profiles to accelerate the standard lead-free process window to meet a targeted manufacturing capacity using an automated profiling system. A test vehicle is then fabricated using this defined process window and tested for quality (solder voiding and appearance) and solder joint reliability (accelerated life testing). The designed test vehicle includes components from a large physical distribution including: small and large BGAs, QFNs, and any type discrete components. During assembly, virtual profiling is used to document any deviations to the process profile window. The quality and reliability data are presented within this publication and failure analysis is included to determine the capability of this proposed profile.

When employed, this profiling strategy allows many manufacturers to reduce the processing time for reflowing lead-free circuit assemblies without significant lost in manufacturing quality or reliability. Furthermore, this study provides a sound understanding and limitations for using accelerated profiling speeds for lead-free soldering applications.

**Background**
Lead-free soldering is expanding at a rapid rate and the manufacturing issues associated with lead-free processing are creating difficulties for many manufacturers. These difficulties have been substantially documented over the past five years and include substrate and component plating changes, differences in solder wetting and solder joint characteristics, and solder joint reliability changes.[5] One of the more significant changes is the higher temperature soldering process and the impact these higher temperatures have on the quality and processing times for electronics products. In particular, the increased reflow temperature of solders (e.g. SnAgCu) increases board warpage by exposing a printed circuit board (with a normal glass transition temperature, $T_g$ of $140^OC$-$160^OC$) to temperatures in excess of $250^OC$. This change can create quality issues for products especially if processed for double-sided assembly.[8,4]

Another impact of the higher reflow temperature is the time extension to accommodate the higher reflow temperatures while maintaining a recommended temperature exposure. To increase the peak reflow temperature from the $220^OC$ - $230^OC$ range for standard eutectic SnPb solder to the range of $250^OC$ - $260^OC$ for SnAgCu, the recommended reflow profile time will increase significantly. This increase in processing time will require manufacturers to slow the belt speed of the reflow oven or add oven capacity to the manufacturing process. Either of these options can be expensive for high volume manufacturers.[7,9]

This research investigates an alternate path for handling the added reflow temperatures for lead-free soldering while minimizing the financial impact for many high volume manufacturers. This investigation focuses on the impact of not using "optimal" reflow profiles and maintaining the same processing window for high volume products. (Only high volume assemblies are considered since slowing the oven belt speed to meet the recommend processing window would not significantly impact low volume manufacturers).

**Reflow Profiling System**

The development of reflow profiles that are optimized on a specific profile statistic (Ex: Ramp rate) can be achieved through the utilization of advanced profiling technology. In order to evaluate the profiles for this experiment, the KIC 24/7 system was used at the Center for Advanced Vehicle Electronics (CAVE) and at the industry locations. CAVE had previously performed a capability study on the system and found it to be very effective in predicting temperatures throughout a wide variety of products and process speeds. This system uses a wireless profiler that passes through the reflow oven (Figure 1), transmitting real-time on-board component temperatures back to a desktop computer. From this input the provided software provides a recommended profile setting for the oven. This profiler provides data in real-time as it passes through the process and simultaneously records the data internally. When the profiler has completed its run through the process, the internally logged profile is wirelessly downloaded, filling in any gaps that may have occurred due to broken transmission of the real-time profile. The system charts the virtual critical process specs for each board: peak temperature, soak time, time above liquidus, etc. The data is plotted on real-time control charts and the process capability (Cpk) is calculated for each specification. The overall Process Window Index (PWI) is charted, provided any process drift outside of the control limits or defined Cpk value will bring an immediate alarm. For precise ranking of profile performance, the system uses the process window index (Figure 2). The PWI calculates how much of the available process window is used by a given profile in relation to its process specifications. Therefore, the lower the PWI, the more efficient and stable the process.

**Figure 1 - KIC System**

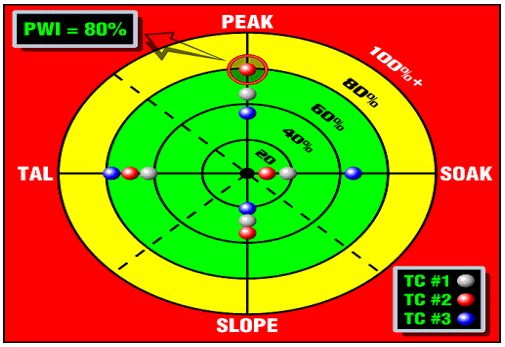


**Figure 2 - PWI Calculation**

**Experiment**

To perform this investigation a series of high volume products were selected from several electronics manufacturers. From these modules a matrix of reflow profiles were developed for SnPb and SnAgCu to estimate the range of additional reflow time needed for SnAgCu. Since this research focused primarily on the worst case scenario, modules with high thermal mass were selected for this experiment.[2,3]. Accelerated reflow profiles were then developed using the virtual profiling system to find the "best" profile while maintaining the reflow process window established for the SnPb solder. Each of these profiles was assigned a PWI that assessed the quality of the profile. From these PWI values, test boards were assembled to investigate the quality of solder joints (voiding and wetting) manufactured. (It should be noted the actual modules were not assembled under the accelerated reflow profiles since these products were not designed for lead-free solder). Thermal couples were attached to the product over a wide area of the printed circuit board (Figure 3). An attempt was made to look for locations with large thermal differentials to ensure high quality performance.

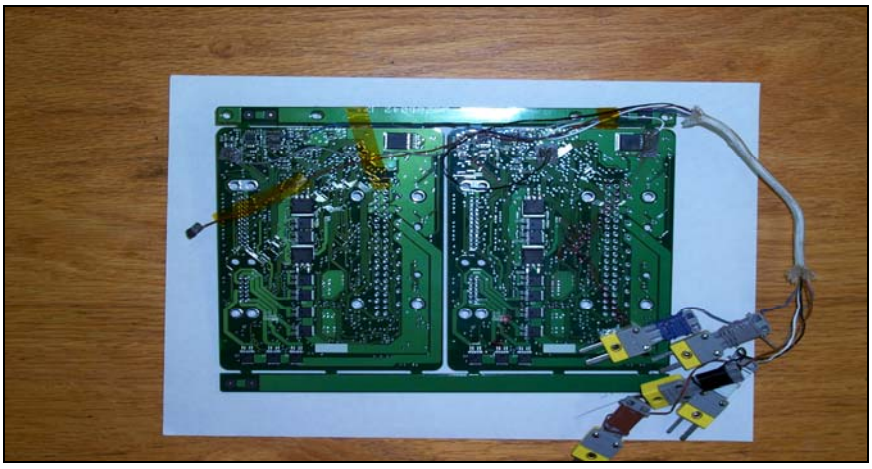

**Figure 3 - Tested Product with Thermal Couples Attached**

**Table 1 - Module Size and Weight**

| PRODUCT | LENGTH (Inches) | WIDTH (Inches) | WEIGHT (Grams) |
|---|---|---|---|
| Product A | 7.500 | 4.313 | 49.40 |
| Product B | 11.250 | 5.313 | 138.50 |
| Product C | 7.188 | 4.750 | 82.50 |
| Product D | 7.563 | 4.750 | 87.00 |
| Product E | 9.500 | 5.313 | 95.00 |
| Product F | 6.000 | 6.313 | 94.80 |
| Product G | 11.438 | 9.000 | 304.80 |
| Product H | 9.438 | 5.313 | 115.20 |
| Product I | 10.500 | 4.750 | 95.30 |
| Product J | 7.188 | 4.750 | 82.50 |
| Product K | 9.688 | 4.313 | 96.20 |
| Product L | 8.125 | 7.313 | 161.30 |

Table 1 provides a summery of twelve modules selected for this experiment. The dimensions of each module are provided along with the weight of each module. This provides some insight into the thermal mass of the module and gives some reference values to translate this work into other potential applications. While some products will exceed maximum size and weight, very few will require accelerated reflow processing times. In addition, modules that smaller and have less thermal mass should have less quality issues by accelerating the reflow processing time.

An “optimal” reflow profile was developed for each module using SnPb solder. The process times for each of these modules are shown in Table 2. In addition, “optimal” reflow profiles were developed for the same modules using SnAgCu. These values are also presented in Table 2 along with the belt speed for each profile. Finally, the time differential for each product is noted in Table 2. These time differentials range from 3 seconds for Products F and K to 83 seconds for Product G. These differences also coincide with the increase in product size and weight. Product A has a larger delta at 17 seconds but the overall processing time is less than the rest. It is also the smallest product manufactured. For the largest module, the reflow profile time increased by over 27% (300 seconds to 383 seconds) to switch Product G from SnPb solder to SnAgCu solder.

The profile variations are illustrated below. Figure 4 shows the SnPb profile for the product (Product L) with the largest processing time. It is also a product with one of the largest weights. Notice that the temperatures transients are typical for SnPb solder and that the temperatures are relatively uniform throughout the printed circuit board. Figure 5 shows the “optimal” reflow profile recommended by the Slim KIC profiling system for this same product with SnAgCu solder. The dashed line shows the virtual profile with an adjusted scale on the bottom of the graph. The initial SnPb profile also shown on this graph and the estimated increase in reflow time is 51 seconds.

Other products have less processing time but greater temperature differentials throughout the printed circuit board. This is usually caused by regions of the printed circuit assembly with very high thermal mass components (e.g. transformers and connectors) and other regions with very low thermal mass (e.g. small passive chip components). Figure 6 shows the reflow profile for Product E. Notice that the processing time is only increased by 24 seconds because there is a non-uniform cooling region for this product (Figure 7). These differences in board temperatures are often the cause of soldering failures and can create significant differences in solder grain structure and solder joint voiding.

**Table 2 - Processing Times SnPb and SnAgCu**

| PRODUCT | SOLDER | BELT SPEED (in/min) | TOTAL TIME (sec) | Delta (sec) |
|---|---|---|---|---|
| Product A | Sn63Pb37 | 33.7 | 248 | 17 |
| | Sn96Ag3.8Cu.7 | 31.6 | 265 | |
| Product B | Sn63Pb37 | 26.5 | 300 | 42 |
| | Sn96Ag3.8Cu.7 | 24 | 342 | |
| Product C | Sn63Pb37 | 29.2 | 303 | 13 |
| | Sn96Ag3.8Cu.7 | 28 | 316 | |
| Product D | Sn63Pb37 | 29.4 | 301 | 48 |
| | Sn96Ag3.8Cu.7 | 25.3 | 349 | |
| Product E | Sn63Pb37 | 30.7 | 300 | 24 |
| | Sn96Ag3.8Cu.7 | 29.5 | 324 | |
| Product F | Sn63Pb37 | 31.5 | 305 | 3 |
| | Sn96Ag3.8Cu.7 | 30.7 | 308 | |
| Product G | Sn63Pb37 | 31.7 | 300 | 83 |
| | Sn96Ag3.8Cu.7 | 24.9 | 383 | |
| Product H | Sn63Pb37 | 33.7 | 268 | 20 |
| | Sn96Ag3.8Cu.7 | 31.2 | 288 | |
| Product I | Sn63Pb37 | 27.4 | 352 | 27 |
| | Sn96Ag3.8Cu.7 | 25.4 | 379 | |
| Product J | Sn63Pb37 | 30.3 | 285 | 19 |
| | Sn96Ag3.8Cu.7 | 28.9 | 294 | |
| Product K | Sn63Pb37 | 27.2 | 304 | 3 |
| | Sn96Ag3.8Cu.7 | 26.9 | 307 | |
| Product L | Sn63Pb37 | 23.4 | 400 | 51 |
| | Sn96Ag3.8Cu.7 | 20.7 | 451 | |

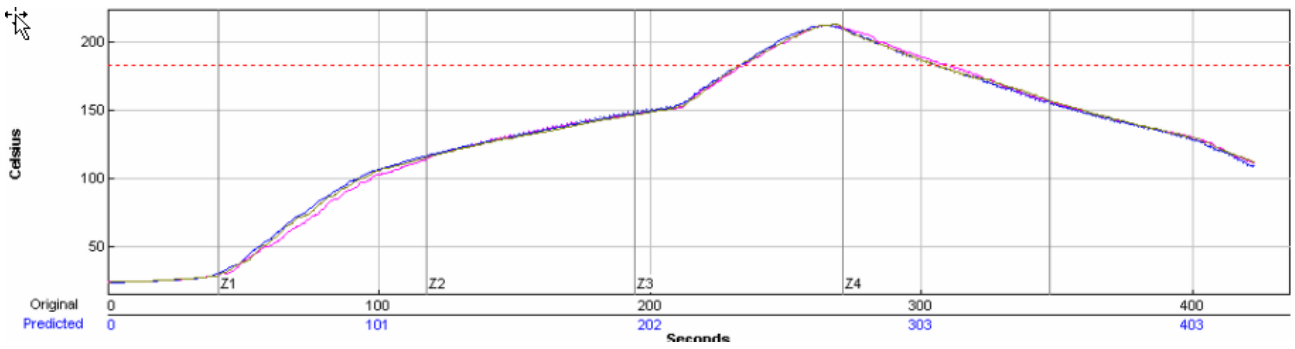


**Figure 4 - Reflow Profile of Product L Using SnPb Solder**

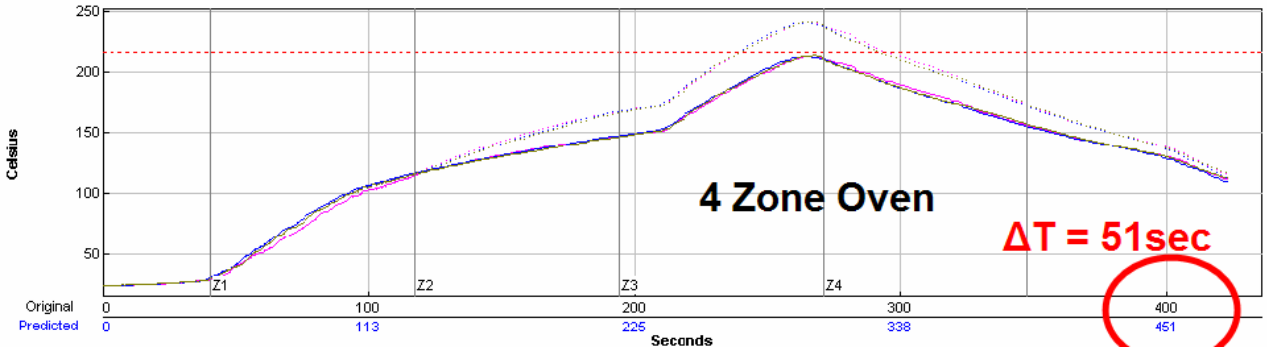


**Figure 5 - Reflow Profile of Product L Using SnAgCu Solder**

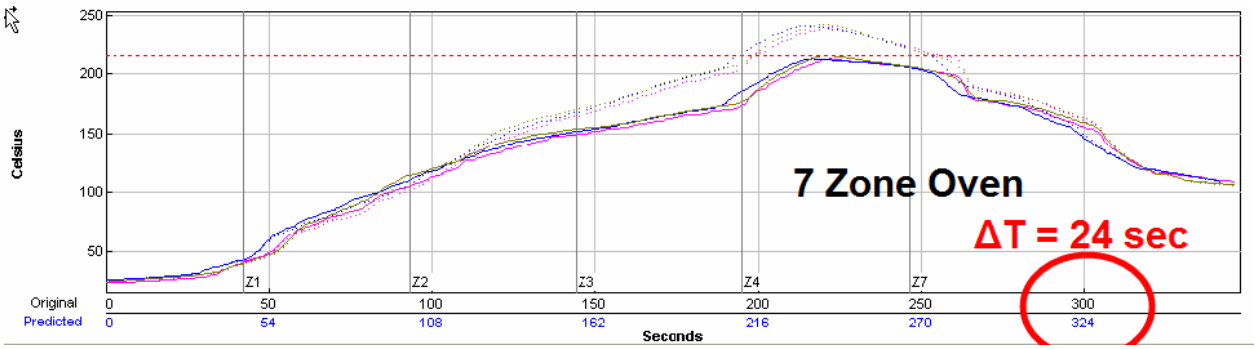


**Figure 6 - Product E Reflow Profile SnPb and SnAgCu Solder (dashed)**

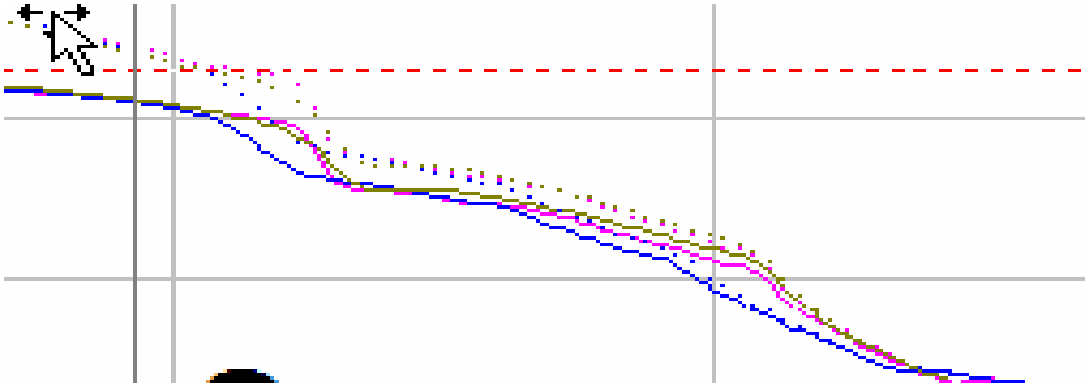

**Figure 7 - Cooling Zone for Product E Showing Temperature Differences**

**Equipment**

To develop a test vehicle to explore the impact of accelerated reflow profiles on lead-free solder joints a test board was fabricated at CAVE. The equipment used for the experiment was high volume capable and the processing parameters were typical of lead-free solder processed board. The screen printing process used was an MPM screen printer and a MVT 3D solder paste inspection process (Figure 8). The components were placed using an ACM placement machine supplied by Assembléon on (Figure 9). Finally, the reflow oven was a 10 zone systems supplied by Heller (Figure 10).

**Figure 8 - Screen Printing and Paste Inspection**


**Figure 9 - Assemble on ACM Placement**


**Figure 10 - Heller Reflow Oven**

**Solder Joint Quality**

Creating SnAgCu profiles which meet the processing time windows for SnPb solder is unproblematic; however, these accelerated profiles run the risk of a detrimental impact on solder joint quality. To investigate the impact on solder joint quality, a test vehicle board was processed under the same PWI conditions to emulate an average accelerated reflow profiles discussed above. Since the PWI values range from 10% to 70% for most of these products, CAVE selected a PWI value of 35% to run the test board. This allowed CAVE to investigate a nominal range of acceleration for the profiles for the initial experiment.

The test vehicle (Figure 11) had ten 2512 chip resistors, four 27mm BGAs, three 17mm BGAs, and four 4x4 mm QFN packages. These packages are often some of the most critical to manufacturer properly and can have reliability issues for many applications.[2,6,10] The 2512 chip resistors were Sn terminated, all BGAs used SnAgCu solder balls, and the QFNs had Sn plated pads. The substrates were OSP or ImAg plated and were FR4-06 (.062" thick) printed circuit boards. All of the packages were daisy chained (with silicon die) and the printed circuit boards were also daisy chained to monitor for solder joint defects.

CAVES used a Phoenix x-ray machine (Figure 12) to investigate the quality of solder joints related to location and solder voiding. In addition, the machine has the ability to calculate the percentage solder voiding for grid array solder joints (e.g. BGAs). This capability was used to estimate the solder voiding in comparison to industry maximum values. It should be noted that this test saw no significant difference in voiding between ImAg and OSP plating on the circuit board. For this reason, only the OSP plate boards were included below.

The solder joints created using the nominal accelerated profile were all acceptable with little solder voiding. Figure 13a shows one of the best solder joints created with the accelerated profile while Figure 13b shows one of the worst solder joints. Notice that even for the worse case solder joint, the voiding is minimal and would not cause any quality or reliability defects.

The impact on quality for the BGAs exposed to an accelerated reflow profile was somewhat more pronounced. Figure 14a shows one of the BGAs with the least solder ball voids. Notice that even the best processed BGA packages has some solder voiding. Figure 14b shows a BGA with the most solder voids in the solder balls. These voids are very noticeable but may not exceed recommended void limits for BGA packages. To address this issue, the void analysis algorithm in from the x-ray machine was used. Figures 15a and 15b shows the solder void calculations for the BGAs with the least and most solder voiding. This analysis yielded a worst case range of solder voiding from 15% to 20%. This level of solder voiding does not exceed the typical allowable solder voiding for BGA solder voiding.

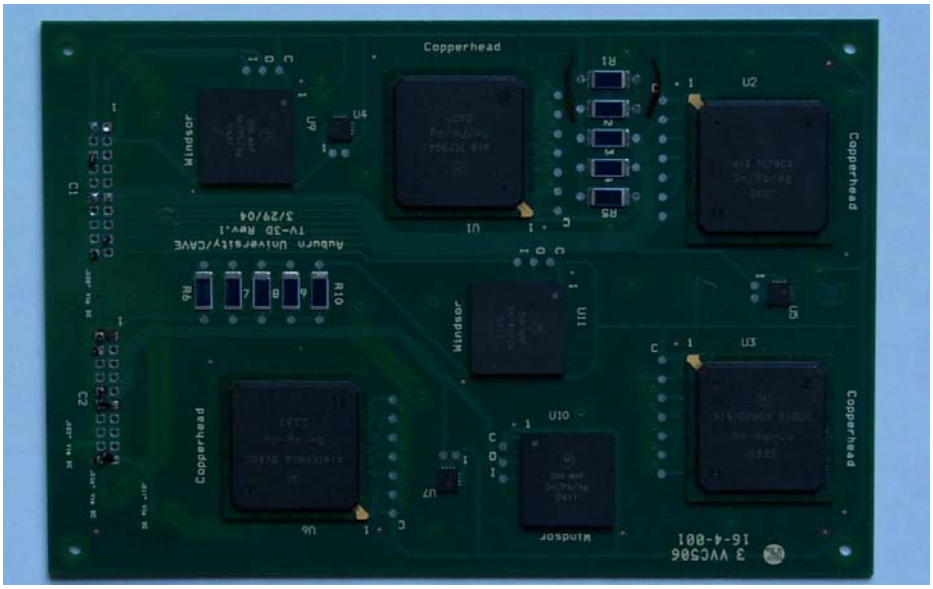


**Figure 11 - Test Vehicle – Accelerated Reflow Profile**

**Figure 12 - Phoenix X-Ray Inspection**

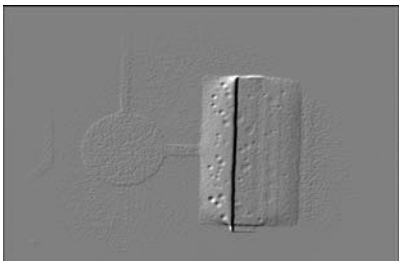

**Figure 13a - Best 2512 Solder Joint**

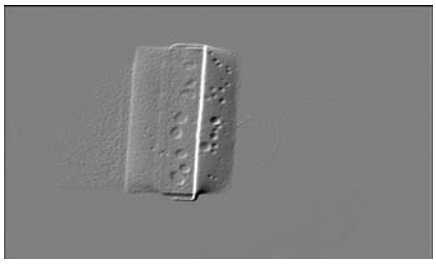

**Figure 13b - Worst 2512 Solder Joint**

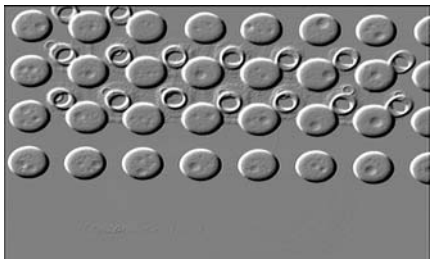

**Figure 14a - BGA with Least Voids**

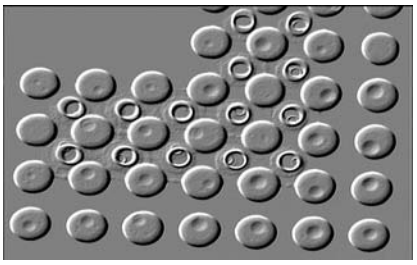

**Figure 14b - BGA with Most Voids**

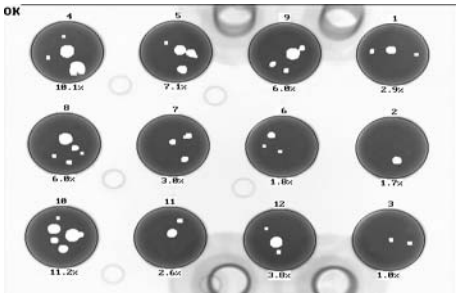

**Figure 15a - Calculation w/Least Voids**

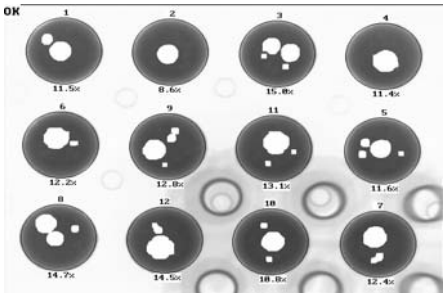

**Figure 15b - Calculation w/Most Voids**

The most important issue with BGA voiding is whether these solder voids will cause electrical defects and whether the voids have a detrimental impact on the long term solder joint reliability. For most applications, the realized solder joint voiding from the above accelerated profile will not have an electrical impact on the performance of the BGA. Even with 20%- 25% void, there will be enough surface contact to provide acceptable electrical performance and enough structure to ensure mechanical integrity of the solder joint. As for solder joint reliability, previous studies (including one performed at CAVE) have shown that solder joint voiding in BGA packages can have a positive impact in long term reliability. The voiding in these experiments were similar to those realized with previous studies at CAVE (15% - 30%) and improved the solder joint reliability by over 25%.[1] It should be noted that this study was performed on BGA packages using SnPb solder balls and SnPb solder paste. Lead-free solder (including SnAgCu) may not yield the same reliability results. Finally, while the solder

voids realized by these accelerated profiles may not create any quality or reliability problems, they might cause deterioration in thermal performance of BGA packages. Since BGAs often use the solder balls as the primary thermal path and often add thermal balls in the center of the BGA, solder voids could have some thermal impact for product designs that are in a marginal thermal performance region.

The final package investigated with this study is the impact on voiding for the QFN packages. QFN packages are becoming a very popular package for many new products due to their smaller package size and their low cost. These packages are often not as reliable as QFP or BGA packages although this reduction is usually one an issue for electronics in very harsh environments. Figures 16a and 16b show the least and most solder voiding for the QFN packages using the accelerated profile. The voiding generated by this profile on the perimeter interconnect does not appear to be significant. The estimated voiding for these perimeter interconnects range from 5% to 20%. A reliability study should be performed on these packages, although, no significant impact is expected. However, the voiding for the center QFN thermal pad is somewhat significant. The voids for these pads range from 15% to around 50%. If the contact area is critical for electrical or thermal performance, the solder voiding in the center of the QFN package may create and manufacturing defect. An electrical or thermal analysis should be performed to ensure that any voiding is within the acceptable limits for the specific product design.

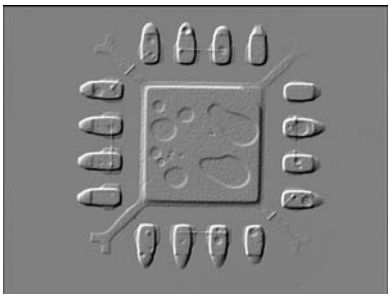

**Figure 16a - Least QFN Voiding**

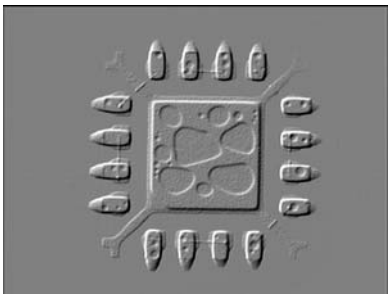

**Figure 16b - Most QFN Voiding**

**Conclusions**

This work provides several significant contributions for the issue of accelerated profiles for lead-free analysis. First, a general range of expected time differences between products reflowed with SnPb profiles versus SnAgCu profiles are defined. Since most of these products are high in thermal mass compared to typical industrial designs, these results may be considered worst case. In addition, this experiment illustrates that accelerating profiles for many applications can continue to yield solder joints with acceptable quality. This experiment also shows how design specific the acceleration of reflow profiles are when considering lead-free solders. Finally, this experiment illustrates how a prediction and monitoring system for reflow profile evaluation can be used to significantly improve the performance of an electronics manufacturing operation.

**Future Work**

There are several additional experiments which need to be investigated further. First, this work focuses on SnAgCu solder for the lead-free application. There are many other solder solutions for lead-free and these results may differ from SnAgCu. Next, this experiment only looks at two common plating materials. Results from alternate platings may also be different. Another issue is the component usage for this experiment. While CAVE attempted to consider many of the most critical solder joints in this investigation, other packages (such as flip-chip and through-hole connectors) may perform differently. As noted above, the impact of accelerating the reflow profile is very design dependent. A better solution may be available for individual components by specifically investigating a “best” solution for a particular product. This solution may include extending the available time window for the profile while still significantly reducing the profile time over the preferred lead-free profile. And finally, while CAVE believes that the solder voiding illustrated in the above experiment should not cause any significant deterioration in solder joint reliability, the reliability should be evaluated based on the field requirements for the specific product design.

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