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A Performance Simulation Tool for Bipolar Pulsed PCB Plating

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Abstract
The copper plating process is one of the most critical steps in the high end PCB manufacturing process. Although the deposition inside through holes and blind holes is the key factor for reducing the fall out fraction, the thickness distribution over the entire layout is also critical, in particular for multiplayer designs. A performance plating simulation tool (P2ST) for the prediction of layer thickness distributions over PCB's is presented. This tool takes into account the bath characteristics (conductivity, electrode polarization), the PCB layout, the electrical signal parameters (DC current or bipolar current amplitudes and duty cycle), and the PCB positioning in the plating tank.

This tool allows us to perform a fast prediction of the layer thickness distribution over tracks, pads, ground planes, robbers etc. The tool can be used by any PCB manufacturer either in the cost estimation phase and/or as an auxiliary tool in the CAM work flow. In the latter case, the tools represents a powerful asset for the optimization of pulse signal and/or background patters (copper balancing) towards layer uniformity specifications.

Introduction
Simulating current density and layer thickness distributions in electrochemical plating tanks has become common practice over the last few decades. Most simulations are based on Laplace type models that take into account:

- plating tank configuration
- configuration of work piece or substrate to be plated
- presence and position of screens, current thieves and auxiliary anodes;
- ohmic drop effects in the electrolyte (depending on electrolyte conductivity);
- linear or non-linear polarization/current density relations at the electrodes;
- injected current (DC or pulsed) through the anodes;

The validity and accuracy of these Laplace type models depends on the rate of stirring or electrolyte refreshment in the reactor (compared to the range of applied current densities), enabling to neglect metal ion mass transfer problems. The acid copper plating bath characteristics (cathodic and anodic polarization behavior) can for example be measured at a Rotating Disc Electrode (RDE).

The result of this type of simulation is basically a current density distribution j over the electrodes. The layer thickness distribution d on the cathodes is easily obtained using Faraday's law:

$$\Delta d = \frac{M\,\Delta t\, j}{\rho\, z\, F}$$

Assuming 100% efficiency for the deposition process. M holds for the atomic weight of the metal, ρ for the density, z is the number of electrons exchanged in the metal deposition reaction, and F is Faraday's constant.

Most literature publications deal with simplified two dimensional (2D) cross sections of a plating tank for simulation proposes, only a few papers deal with full three dimensional (3D) current density distribution and layer thickness simulations, for example.[1, 2]

Modeling PCB Plating Processes
Modeling PCB or wafer plating processes poses some additional difficulties, since the patterned electrode surface is to be accounted for. Moreover, 2D cross sections are irrelevant in this case and a full 3D approach is required.

For vertical PCB plating processes (Figure 1), a distinction can be made between reactor (plating tank) scale simulations (= macro scale), PCB / pattern scale simulations (= meso scale) and feature scale simulations (= micro scale). Macro scale simulations predict the difference in layer thickness from one board to another or from one printed circuit to another one on the same board. An example of the macro scale current density distribution is given in Figure 2 for normal operating conditions and for an anomalous situation with 2 empty anode baskets in Figure 3. Remark that the influence of the circuit

layout has not been taken into account. Meso scale simulations however incorporate the printed circuit layout, since the layout is determinant for the distribution of electro-active zones on the board. An example of a typical printed circuit layout is given in Figure 4. Calculations for an acid cupper DC process based on the numerical model presented in[1] have been performed. Figure 5 shows the corresponding current density distribution, with the blue color corresponding to high (cathodic) current densities. Clearly, the edge effects on the electro-active surfaces are visible. The red zones correspond to the masked area.

Figure 6 shows the cupper deposit layer thickness resulting from the calculations. Again the very high edge built-up is visible, especially for isolated features. Based on these calculations, improvements to the plating process can be determined.

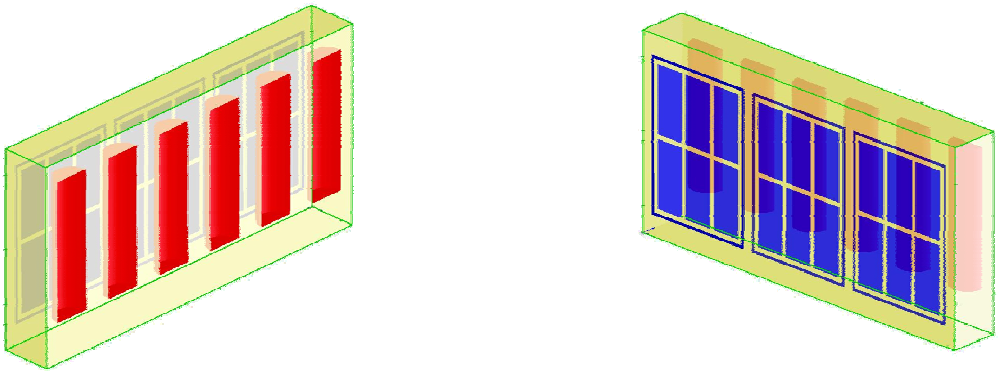

Figure 1 - Vertical Plating Tank Configuration With Anode Baskets (Red) and PCB's (Blue)

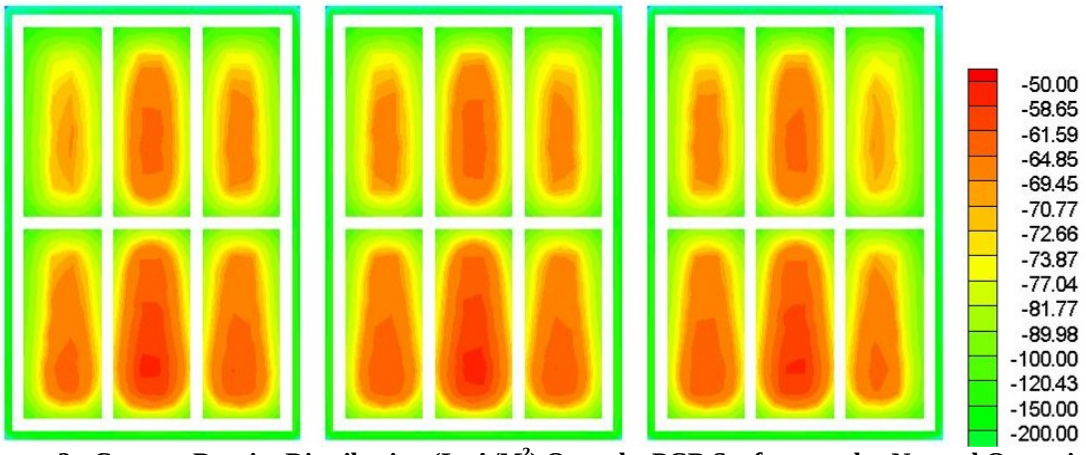

Figure 2 - Current Density Distribution (In A/M^2) Over the PCB Surfaces under Normal Operating

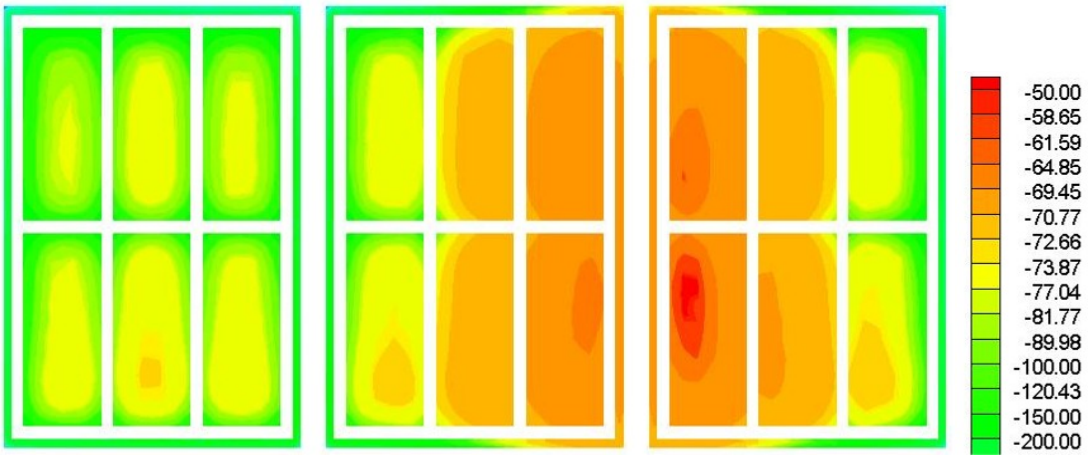

Figure 3 - Current Density Distribution (In A/M^2) Over the PCB Surfaces with Two Anode Baskets Empty

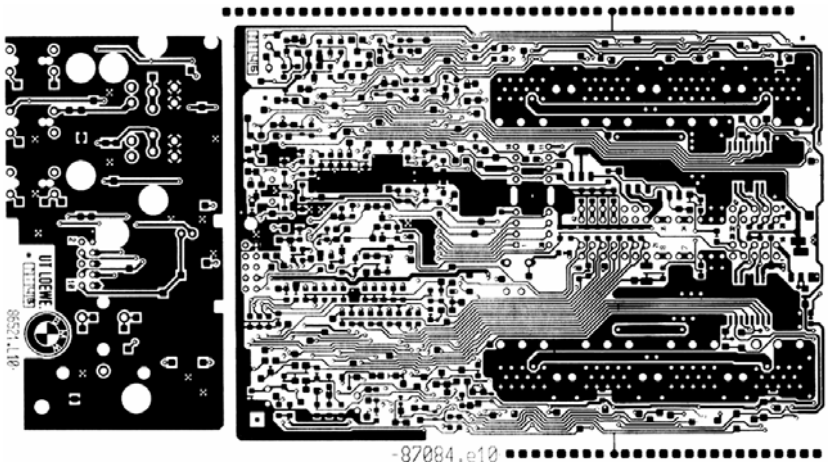

Figure 4 - Typical Printed Circuit Layout

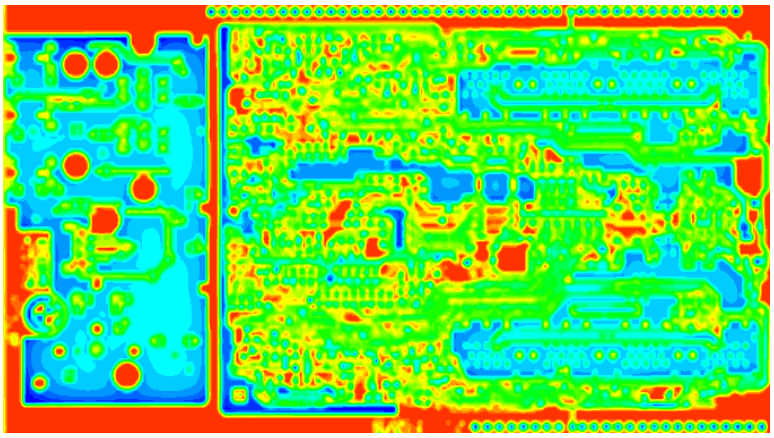

Figure 5 - Current Density Distribution (High Values Are In Blue. Red Corresponds To Masked Areas)

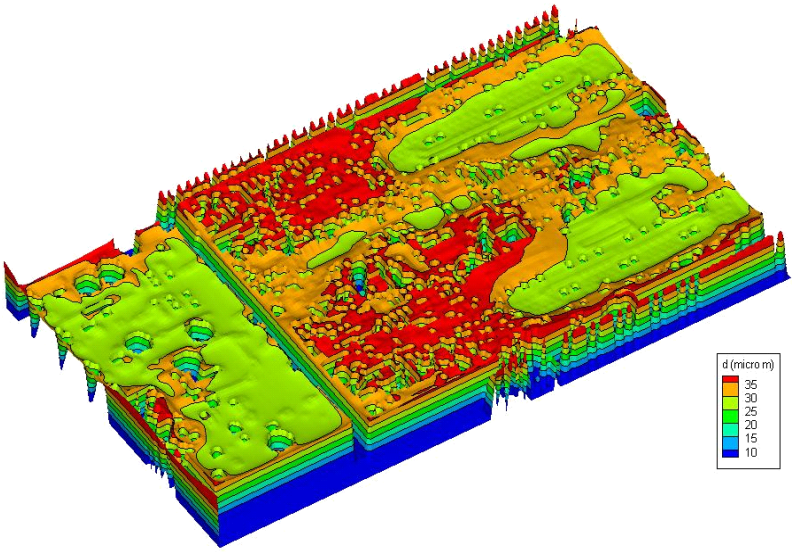

Figure 6 - Copper Layer Thickness Distribution in Micron (High Deposit Thickness Regions in Red)

To gain more insight in the plating processes on the micro scale (through holes, vias, etc), simulations need to be performed using more elaborated models. These models include the fluid flow, mass transport and detailed reaction mechanisms (both chemical and electrochemical) in order to generate accurate simulation results of the layer thickness distributions. Results from through-hole plating simulations using these extended models can be found for example in papers[3, 4] but are beyond the scope of this paper.

The P²ST Concept

Macro scale current density distribution problems are mainly due to an improper plating tank configuration, e.g. empty anode baskets, partly dissolved anode rods, an ill-defined PCB rack configuration etc as shown in the examples presented in Figures 1 and 2. But these problems can be solved relatively easily, and are of inferior importance to the meso scale current density distribution problems.

The performance plating simulation tool focuses on the meso scale level, while capturing also part of the macro scale effects. The concept is given in the flow chart of Figure 8. First, the circuit layout has to be read from some proprietary or standard file format (e.g. Gerber). Next the electrolyte bath characteristics for a specified acid copper type bath are retrieved from the available database. Also the most relevant reactor configuration dimensions need to be defined (distance of boards to anodes, distance from one board to the next etc.). Finally the Bipolar Pulse parameters (anodic and cathodic pulse height, anodic and cathodic on-time, off-time, etc) as shown in Figure 7 or the DC current amplitude is to be specified in order to complete the required set of simulation input data. Possible also an on-board thieving grid is to be specified. Next the layer thickness distribution on the PCB is computed, and the result is compared to the specifications (minimal and maximal allowed Cu layer thickness). The results of the simulation also give indications on the local micro scale plating performance (i.e. especially in blind and through-holes) through more detailed calculations or an expert system. If specifications are not met, the layer thickness distribution is computed for another pulse program. In a first release (v1.0) of the tool, the user has to specify by hand the pulse program for each simulation run. In later releases, an automated optimization algorithm will be implemented on top of the simulations, and the optimal pulse plating program is delivered by the tool.

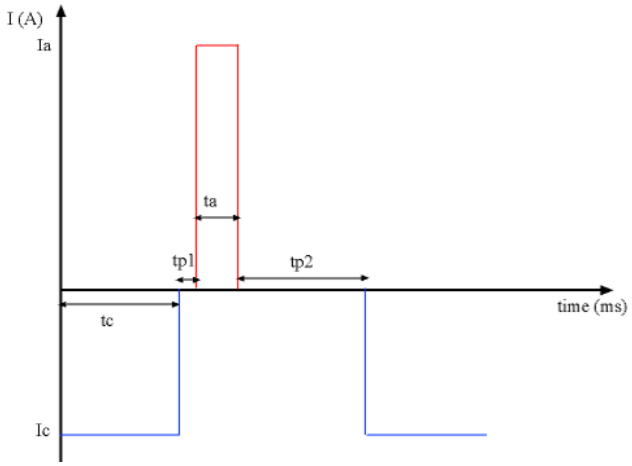

Figure 7 - Bipolar Pulsed Current Signal

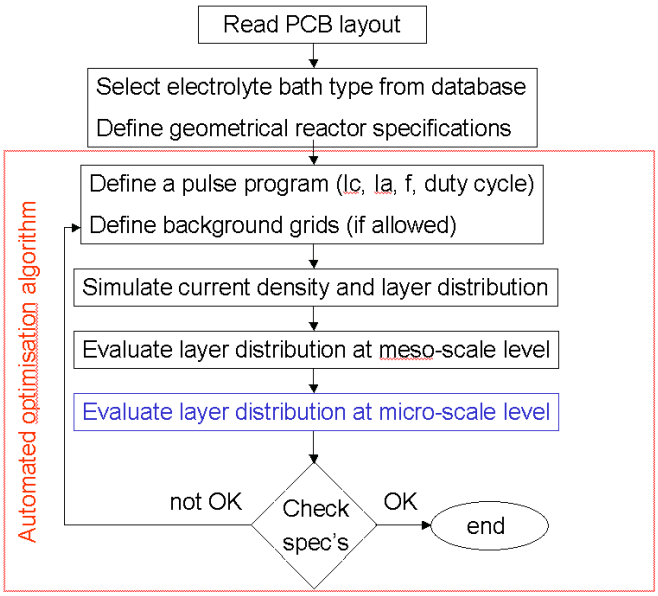

Figure 8 - P²ST Operational Flow Chart

Conclusion

A performance plating simulation tool for the prediction of layer thickness distributions over PCBs and optimization of the pulse parameters has been presented. The focus is on meso-scale current density distribution problems (i.e. non-uniform layer thickness distribution caused by the circuit layout), but also macro (reactor) scale parameters are partly included, and a link to micro scale level layer thickness distributions is established.

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