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System in Package: Identified Technology Needs from the 2994 iNEMI Roadmap

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System in package (SiP) technology has grown significantly in the past several years. It was barely mentioned in the National Electronics Manufacturing Initiative's (NEMI's) 2000 roadmap, but by the 2002 roadmap, SiP was one of the fastest growing packaging technologies. Even though, at that time, SiP represented a relatively small percentage of the total unit volume, the 2002 NEMI roadmap noted that SIP was becoming a common technology in the high-growth Bluetooth, WLAN (wireless local area network) and mobile phone applications. By 2004, SiP had grown so significantly that it was added to the roadmap as a new product emulator group (one of seven), which are used to define future manufacturing needs across the entire electronics supply chain.

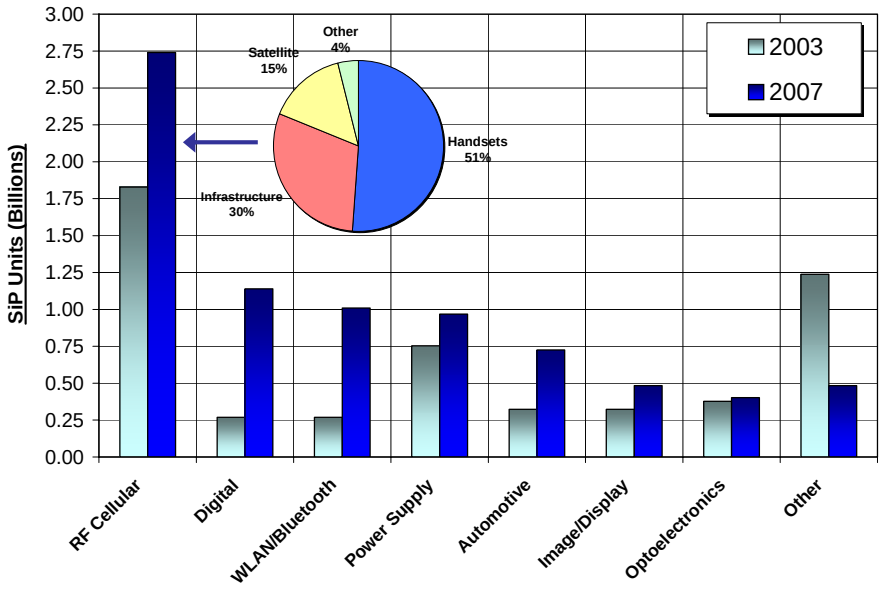
The ability to integrate different technologies and to reduce total product cost and time to market are the prime drivers for SiP packaging. For the wireless markets, which require very high performance, SiPs have enabled the rapid integration of SiGe, GaAs, Si and passive devices into single package solutions that are not possible today with single-chip solutions. In most cases, this approach has also reduced product costs, allowing systems to be partitioned into the most cost-effective blocks. For the system company, these highly integrated functional blocks simplify system design, assembly process and test requirements. Stacking logic and memory chips in a single package is another fast-growing application for SiP. These stacked SiP configurations reduce system size and eliminate the cost of individual packages for each die. They also improve signal transmission times and, as an added bonus, reduce power by minimizing capacitive loads between ICs.

SiPs, interestingly enough, are supported by OEMs because they want to continue to push more technology back into the semiconductor side of the business (because of the tremendous average selling price (ASP) erosion experienced in that market) while holding onto extremely high yields and reliability.

There is much discussion, even confusion, about whether system on a chip (SoC) or SiP is the better approach for system design. However, they are often complementary. Development of a new SoC requires a significantly greater investment, both in terms of expense and product cycles. Some products simply cannot support the additional cost or do not have a lifecycle that warrants SoC development, making SiP the cost-effective solution. However, in other cases, a SiP may be used in interim products to add functionality while a SoC is being developed. For example, an OEM might design a first-generation product using an SiP; then the next generation will add more functionality — with the use of a new SiP version — and, possibly the third generation will integrate all of the second-generation functionality onto a single chip. At that point, the SiP transforms itself into another package that now supports the SoC and other functions such as antennas, crystals, filters, shields and/or other passive components that are not part of the SoC.

At present, there are three types of SiPs that are running in very high volumes: modules, stacked die packages and stacked package on package. (See "Types of SiPs" for descriptions.) Laminate substrate-based SiPs continue to dominate the market, but ceramic, lead frame and tape substrate technologies are rapidly growing.

Overall SiP Market: 2003 vs. 2007



Other markets = military, medical

Figure 1 - Overall SiP Market 2003-2007

Sources: Prismark (primary), Deutch Bank, Credit Suisse First Boston, Allied Business Intelligence.

State of the Technology

Rapid expansion of the SiP market has stimulated research and development in SiP-related technology by IDMs (integrated device manufactures) as well as electronic manufacturing services (EMS) providers and semiconductor assembly services (SAS). R&D efforts have also led to development of SiP-specific design tools, equipment, materials and components. However, like most emerging technologies, R&D expenditure has not been increased to the level required in several key areas.

One of the technology challenges for early adoption of SiP was the lack of integrated design tools that would enable chip and package co-design. Several of the large EDA companies and numerous small design tool specialists now have commercial tools available for SiP. As the complexity and performance targets for SiP increase, these tools need to be enhanced to provide faster 3D electrical and mechanical simulation capability. One area in particular that needs to be developed is the ability to evaluate the impact of manufacturing variance on SiP electrical performance.

SiP technology is pushing equipment and related process capabilities to their limits for SMT, die attach, wirebond and flip chip processes. Equipment companies have started to develop dedicated platforms for SiP applications in some of these areas, which has helped to resolve process capability problems. One of the biggest areas of opportunity for further cost reduction is the development of die attach and flip chip placement. The 2004 NEMI SiP roadmap calls for placement equipment to be able to handle die placements from wafer format with 15-micron accuracy at less than $.005 per placement. Industry can not meet this target with today's equipment.

In the materials and component technologies areas, SiP is driving new material applications and the related need to develop new qualification requirements. Most SiP technologies are already based on lead-free assembly processes and qualified to MSL level 3 250°C reflow conditions, well ahead of the general electronics industry. As SiP applications continue to grow, the focus on new materials tailored to these applications will be needed to further improve cost and reliability.

As higher complexity, multifunction SiPs are developed, the need for optical and MEMs-based components will also become more significant. These component types utilize specialty packaging technology, which is difficult to integrate into many SiP

configurations due to thickness, size and cost. Low-profile, low-cost wafer-level packaging needs to be further developed by industry to resolve these problems.

Roadmap of Key Attributes

To help quantify requirements for design, assembly processes, materials, components, and reliability, a limited set of metrics have been defined for SiP. Given the broad range of applications and the immature nature of SiP products, the metrics were selected based on the ability to verify a trend and relevance to the research community.

Table 1 - SiP Critical Requirements Forecast

System In Package Requirements											
Year of Production	***2005***	***2006***	***2007***	***2008***	***2009***	***2010***	***2011***	***2012***	***2013***	***2014***	***2015***
Number of Terminals-Max MCM	*2000*	*2000*	*2000*	*2000*	*2000*	*2000*	*2000*	*2000*	*2000*	*2000*	*2000*
Number of Terminals-Max RF Module	*80*	*100*	*120*	*140*	*160*	*160*	*160*	*?*	*?*	*?*	*?*
Max number of stack die	*7*	*7*	*7*	*7*	*9*	*9*	*9*	*9*	*9*	*9*	*9*
Max number die in Module	*10*	*10*	*10*	*8*	*8*	*8*	*6*	*6*	*6*	*6*	*6*
Minimum Component size in.	*0201*	*01005*	*01005*	*01005*	*01005*	*01005*	*01005*	*01005*	*01005*	*01005*	*01005*
Embedded Passives in Laminate	*L*	*CL*	*CL*	*CL*	*CL*	*CL*	*CL*	*CL*	*CL*	*CL*	*CL*
Embedded Passives in Ceramic	*R, L, C*	*R, L, C*	*R, L, C*	*R, L, C*	*R, L, C*	*R, L, C*	*R, L, C*	*R, L, C*	*R, L, C*	*R, L, C*	*R, L, C*
MSL Level	*2a*	*2a*	*2a*	*2*	*2*	*2*	*2*	*2*	*2*	*2*	*2*
Max Reflow temp C	*260*	*260*	*260*	*260*	*260*	*260*	*260*	*260*	*260*	*260*	*260*

The maximum number of terminals for MCM is driven by the large computing system and network markets where complex systems are being implemented using large scale MCM technology. Performance is a key driver in this market. Terminal I/O has been driven high enough for mainframe applications that it pushes the limits of the PCB technology and as a result is not expected to increase further.

Terminal counts for RF modules have been limited primarily by the RF systems requirements, which do not in general drive high I/O counts. With the projected increase in module functions and transition to digital interfaces, this I/O count is expected to increase rapidly over time until it reaches the limits of I/O density. Most module products use single row perimeter I/O with .5mm pitch, so the increase in I/O count is expected to push I/O density to the .4mm pitch in the 2007 time frame. This will drive test socket requirements, SMT processes, and motherboard density improvements.

The max number of stacked die is being driven by the increasing use of memory in space constrained applications. This requirement will continue to drive the need for improved wafer thinning, die attachment, and wirebond processes - optimized for stacked package assembly.

Die counts for module based SiP is expected to drop over time as many applications will use higher levels of SOC integration to reduce total die counts. One key change in this trend could be the introduction of specialized device technologies like sensors to add functionality. These devices are projected to utilize wafer level packaging and be surface mountable, but if wafer level packaging does not become dominate, die counts could increase.

Embedded passives are being broadly utilized in ceramic, laminate, and even lead frame based SiPs today. However there is some clear segmentation in complexity and type. In lead frames, the formation inductors based on simple conductor spirals (having a limited range of values) are typical. In laminates, a broader range of inductor types are available and capacitor structures based on new dielectrics are beginning to emerge. In ceramics, there is a broad range of resistor, capacitor and inductor types available, based on the range of specialized dielectrics. The most critical requirements for embedded components are improved tolerances and reduced cost.

Infrastructure Issues

SiP technology merges the surface mount technology of the EMS industry with the semiconductor assembly and test technologies of the SAS industry. This convergence thrusts surface mount technology (SMT) and bare die assembly technologies together in a single factory, which poses several challenges and raises critical infrastructure issues that must be addressed. The two groups (EMS and SAS) have different business models as well as different requirements and specifications. Then there are issues of equipment and skill sets.

In order to hit reasonable profit levels, the SAS companies target gross margins in the 20% range, while the EMS companies target gross margins in the 10% range. The difference in these operating models is due to differences in factory overhead (clean room vs. standard manufacturing), R&D, equipment and labor cost. For SiP, manufacturing companies must develop a new operating model that mixes the SAS and EMS structures. This model must also be able to support the industry target of a 15% reduction in product cost per year to maintain competitiveness.

In addition, EMS and SAS operations do not follow the same quality and reliability specifications. EMS providers use IPC board mount specifications while the SAS use JEDEC component specifications. This can create some major differences, depending where the SiPs are built and what is needed for the end market requirements.

Skill set is another big issue. The mixed technology skills required for SiPs are not readily available and require taking specialists from different areas and combining their skills. Typically, a company has to hire one or the other skill set, and then train the individual, which is a two-year process. The industry will need to develop better SiP training forums to help resolve this issue.

Recommendations

- A number of recommendations have been made for SiP technology in the roadmap including:
- Improved design tools for emerging technologies like embedded passives and optoelectronic PWBs.
- Develop automated printing, dispensing, placement, and rework equipment capable of the pitch requirements for SiP package assembly at current process speeds.
- Develop Low cost, higher thermal conductivity, packaging materials, such as adhesives, thermal pastes, and thermal spreaders.
- Develop new approaches to organic substrate fabrication which address needs for dramatic increases in density, reduced process variability, improved electrical performance, and radical reductions in cost.
- Establish an iNEMI SiP Technology Implementation Group (TIG) to develop a research and development plan for closing the SiP gaps identified in the roadmap
- Efforts to organize the recommended iNEMI SiP TIG have already begun. This group will address the other recommendations made in the roadmap.

Conclusion

SiP technology offers a viable alternative to the product designer. While the march to ever increasing silicon integration continues, SiP provides the ability to mix semiconductor technologies along with other functional components in a package that, in many cases, looks and feels like a single chip device (from the board assembly point of view). Advantages can include increased packaging density, improved supply chain flexibility (i.e., design for postponement), reduced risk (over fully integrated silicon) and lower total system cost. A number of infrastructure issues need to be addressed in order to allow this technology to achieve full potential. Given the margin pressures on this segment, industry collaboration could provide a cost-effective way to close the identified gaps without any one company taking on the full development burden.