Presented in the ECWC 10 Conference at IPC Printed
Circuits Expo®, SMEMA Council APEX® and
Designers Summit 05

New Concept Multi-Layer FPC "SBic" For High-Density Device Mounting

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Abstract
We have developed a thin, high-density device-mounting, multilayer flexible printed circuit (hereinafter flexible printed circuit is referred to as FPC) "SBic" (stands for Solder Bump Interconnection Circuit) based on our original materials and manufacturing technologies of FPCs.[1)]

The features of this multilayer FPC are attainment of high-density device mounting, high reliability, and super-thin thickness, for example six layers: 0.3mm, eight layers: 0.4mm, etc., with an all-layer IVH (stands for Interstitial Via-Hole) structure. The interconnection consists of a solder bump, which has a copper bump as the core, and a capture pad. The flux activity of Deoxidizable Bonding Film, our proprietary interlayer adhesive, supports the bump and the pad connected by solder.

We verified formation of the alloy of tin and copper by cross sectional observation. The reliability of the interconnection passed a temperature cycle test (1,000 cycles at the range of -25°C to 125°C), a thermal shock test (100 cycles at the range of room temperature to 260°C), etc. The conductive resistance of the interconnection kept an almost theoretical value during the temperature cycle test.

We adopted the simultaneous interconnecting lamination of all-layer method, and attained shortening of the processes and a high yield ratio. Moreover, halogen-free and lead-free materials were adopted for all the components in consideration of environmental protection.

Introduction
The increasing demand for smaller, lighter, and faster electronic products has encouraged the development of technology for higher integration and higher density mounting of electronic devices. Consequently, the demand for a printed circuit board (PCB) 's capability of miniaturization, lightened-weight and high-density mounting, and the use of multilayers has increased. The general multilayer PCB has been moving from a conventional one with through hole interconnection, to build-up PCBs suitable for high density circuits. Moreover, multilayer PCBs that have new structures such as a stacked via-hole, have been developed.

Multilayer PCBs are mainly used for motherboards and module baseboards of electronic products. As portable products such as cellular phones and digital video cameras have become smaller and lighter, the occupation of connecters and cables that connect PCBs in electronic products has been becoming an obstacle of further miniaturization lately. To solve this difficulty, the use of multilayer flexible printed circuits (FPCs) has been rising rapidly, and their market growth is expected in the future.

Concepts
The market of multilayer FPCs is growing, and the mainstream is a four-layered to six-layered FPC with through-hole interconnection. On the other hand, the production of high layer count multilayer FPCs like a ten-layered FPC made by using a build-up process is also growing steadily, and many companies have developed multilayer FPCs with stacked via-hole structure aiming at higher circuit density.

Therefore we have developed a new multilayer FPC capable of high-density mounting on the basis of our fabrication technology and material technology. The following are the concepts:
1. Capability of high density-mounting by all IVH structure
2. High reliability by solder interconnection
3. Use of environmentally-friendly materials such as halogen-free, antimony-free, and lead-free materials.
4. A high yield rate by all-layer simultaneous laminating

Structure

Figure 1 shows the schematic structure of a multilayer FPC "SBic (Solder Bump Interconnection Circuit)". Table 1 shows a road map of its design.

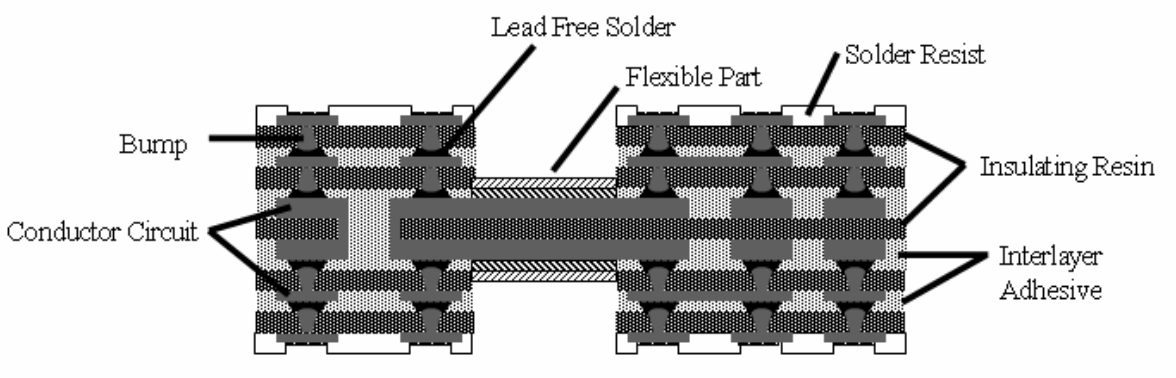


Figure 1 – Schematic Structure (6-layered)

Table 1 – Road Map of Design Rule

		Unit	Current	2006	2007
Inner layer FPC (Double sided)	Base material thickness	μm	25	25	25
	Conductor thickness	μm	22	12	9
	Minimum L/S	μm	75/75	40/40	25/25
	Via diameter	μm	100	75	50
	Land diameter	μm	300	250	200
Outer layer (Single sided)	Base material thickness	μm	25	25	25
	Conductor thickness	μm	12	12	9
	Adhesive thickness	μm	25	20	20
	Minimum L/S	μm	50/50	40/40	25/25
	Bump diameter	μm	80	70	60
	Land diameter	μm	250	200	150
Minimum thickness of a six-layered FPC		μm	approx. 310	approx. 270	approx. 250

The SBic consists of a double-sided FPC as its inner layer circuit board and single-sided FPCs that are laminated on the inner layer circuit board with adhesive. The circuits in each layer are interconnected by lead-free solder between the copper bump and pad of the circuits. The SBic has high density and reliability by using an all-layer IVH and a stacked via-hole structure. In addition, the SBic is thin because the base film is made of polyimide. For example, thicknesses of six-layered and eight-layered SBics are 0.3 mm and 0.4 mm respectively. Although the first generation of SBics cannot have an all-layer stacked via-hole structure because the through-hole interconnection is used in the inner layer circuit board, the second generation will have an all-layer stacked via-hole structure and its features will be enhanced.

Fabrication Process

Figure 2 shows the fabrication process of the SBic.

The inner layer circuit board is a general double-sided FPC and fabricated by processes as follows.

1. Through holes are formed on a double-sided copper-clad laminate with polyimide base by drilling and electroplating.
2. Dry film resist is laminated on both sides of it, and the circuit is formed by processes such as exposure, developing, etching, and DFR stripping.
3. Its flexible area is covered with a cover layer film by a heat-press process. Thus the inner layer circuit board is obtained. The following processes fabricate the outer layer circuit board.
4. Micro via-holes are drilled on the polyimide side of a single sided copper clad laminate by UV laser.
5. The via-holes are filled with electroplated copper, and the top of the bumps protrude from its surface about 5-10 micrometers in height. Then lead-free solder is electroplated on the bumps about 5-15 micrometers in thickness.
6. Dry film resist is laminated on it, and the circuit is formed by processes such as exposure, developing, etching and DFR stripping.
7. Deoxidizable bonding film (DBF) is laminated on its polyimide side. Areas on which the inner circuit board needs to be exposed, are punched out. Thus the outer layer circuit board is obtained.
8. The inner layer circuit board is layered with the outer layer circuit boards by processes as follows. The inner layer circuit board and required number of the outer circuit boards are aligned and stacked, and then the stacked circuit board is heat-

pressed below the melting point of the solder in vacuum.

9. The stacked circuit board is heat-pressed above the melting point of the solder with low pressure for a short period. This process results in the melting of the lead-free solder, forming of solder fillets, and interconnecting of each layer.
10. DBF is fully cured by baking, and then the solder resist layer is formed on the surface of the board. Surface treatments such as plating and preflux are done if necessary.
11. A Punching or router cutting process shapes the board.

The above processes finish the SBic.

Technologies

Bump Forming Technology

The bump forming technology of an SBic consists of four processes: laser drilling, desmear, copper bump electroplating, and solder electroplating. Figure 3 shows the micro via hole and the bump that are obtained by these processes.

The micro via-holes are formed on the resin side of the single-sided copper-clad laminate by laser drilling. Not only polyimide and liquid crystalline polymer but also materials that are easy to drill by laser, can be used as the resin of the copper-clad laminate. We adopted a 355 nm UV laser for drilling because a short wave length has an advantage in the micro process. We obtained the micro via-holes whose etching factor was more than three by the optimization of the energy density of the laser.

Resin smears on the bottom and sidewall of the via-holes are removed by the desmear process. This is an important process that affects the qualities of the copper bump electroplating considerably. A wet desmear process by $KMnO_4$ was been examined, but liquid did not been penetrate into the-via hole well. As a result, a plasma dry desmear was adopted. We optimized its condition by examining several gases.

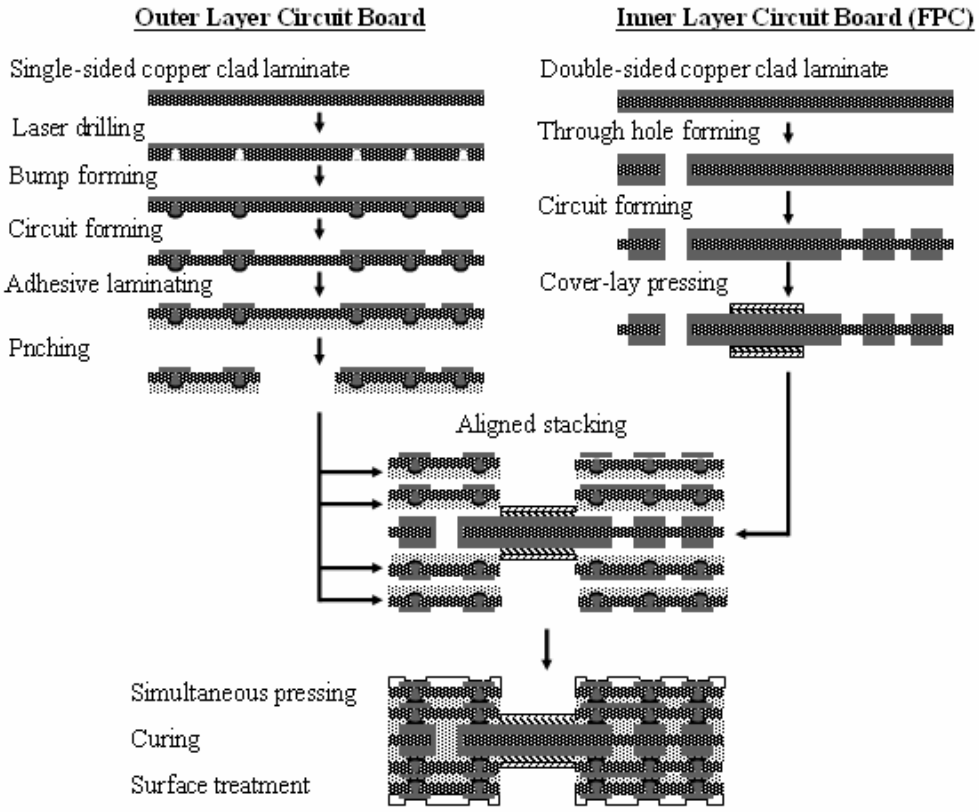


Figure 2 - Fabrication Process

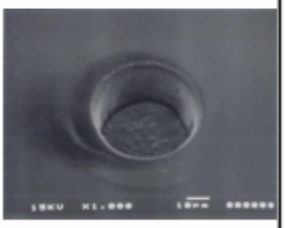
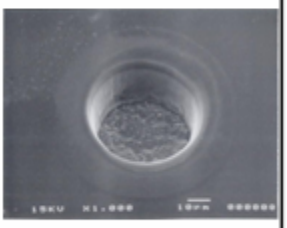
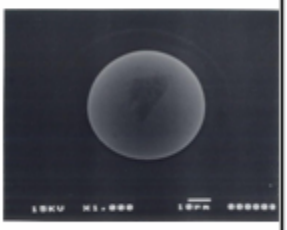
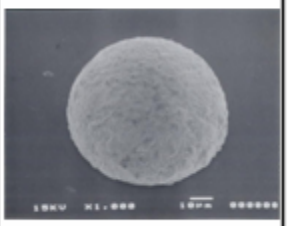
Processes	(1) Laser drilling	(2) Desmear	(3) Copper bump plating	(4) Solder plating
SEM Image				

Figure 3 - Bump Forming Process

The next process is the electroplating of copper bumps. The copper bumps are obtained by filling via-holes from its bottom by electroplating, using the foil of the copper-clad laminate as an electrode. The top of the bumps protrudes from the resin side of the copper-clad laminate with a dome shape. Accuracy of the electroplating current is required in this process because the sum of the bottom area of the bumps is very small. Additionally, accuracy of the drilling is also required because small differences between areas of the micro via-holes affect current density considerably. The sum of the electroplating area increases with the growth of copper bumps because the diameter of the via-hole at the top is bigger than that at the bottom. Then the electroplating current is changed during the via-hole filling process in order to keep the current density constant and the grain size of the copper equalized. The optimization of additives yielded high speed electroplating technology and reduced tact time to one tenth of its initial value, and vastly improved productivity. Additives affect the shape of the bump, and they control the growth direction of the copper, not along the surface of the copper-clad laminate but off it.

After the electroplating process of the copper bumps, they are covered with solder by electroplating. We have been examining lead-free solders from the beginning in consideration of the environment. Currently we are using Sn-Ag solder, which has good joint strength. In the process of the solder electroplating, the current is also controlled accurately. The solder layer is formed on the copper bumps with 5-15 micrometers in thickness. Dispersion of the bump height after the solder electroplating is less than 5 micrometers, and this yields reliability of the interconnection.

All layer Simultaneous Laminating Technology

Deoxidizable Bonding Film (DBF)

As an adhesive, DBF plays an important role in the all-layer simultaneous laminating process of a SBic. DBF is required to have (1) high bonding strength between each layer, (2) good forming characteristic in heat-press with low temperature and low pressure, (3) high flux activity on the copper surface and the solder surface during the interconnecting process, (4) high fluidity in order to shape solder fillets during the interconnecting process and (5) high reliability as an insulator after curing. In addition, DBF should be prevented from squeezing out on the area on which the inner layer circuit board should be exposed because it is used for the multilayer FPC.

For these purposes, DBF is designed not to have raw materials that cause voids under the condition that pressure is low and temperature is higher than the melting point of the solder. To achieve it, resins that do not include any monomers and volatile contents were selected. Thermosetting resins and hardeners that have molecular structure bringing low water absorption, high heat resistance, and high bonding strength are used in DBF.

If the fluidity of DBF is not enough at the melting point of the solder, the solder does not sufficiently spread and shape fillets. On the other hand, DBF should not be too much fluid, in order to hold a certain thickness between each layer. The optimization of the molecular weight of the resin solves this difficult problem.

To give flux activity to the DBF, a small amount of additive that is not activated below the melting point of the solder, and has a deoxidizing function group which combines with the resin after curing is added.

The flux activity is evaluated by observing the surface of the solder covered with DBF in the heating process. If the DBF contains a sufficient amount of additive, the surface of the solder gets gloss above the melting point of the solder because of the flux activity. On the other hand, the solder does not get gloss during heating if an amount of additive is not enough. A suitable quantity of additive was decided by this evaluation.

All-Layer Simultaneous Laminating Process

The laminating process of a SBic consists of four processes, which are aligned stacking, laminating press, interconnecting, and curing. Photos and illustrations in Figure 4 show a sequence of the process.

During the aligned stacking process, the outer layer circuit boards are aligned and stacked sequentially on both sides of the inner layer circuit board, and the circuit boards are fastened together by bonding the periphery of the circuit board temporarily. Although the positioning accuracy between each layer is currently about plus-minus 75 micrometers because the circuit boards are aligned by a pin lamination method, we are developing a highly accurate stacking machine using image processing, and plan to improve the positioning accuracy.

After aligned stacking, the circuit board is laminated by heat-press in a vacuum. DBF runs into spaces between the circuit lines, and the bumps approach pads of the circuit. Because DBF is designed to have a good molding ability at low temperature and low pressure, and to have suitable fluidity, it can minimize not only the dislocation of the inner layer, which can be a problem with a laminating process using heat-press, but also its squeezing out onto the exposed area of the inner layer circuit board.

Next to the laminating, the circuit board is interconnected by heat-press at a temperature above the melting point of the lead free solder. During the heat-press, the temperature is kept at about 250°C with low press pressure for one minute. DBF has good fluidity at about this temperature, and cleans the surfaces of the bumps and pads with its flux activity. The solder melts and spreads on the pad of the circuit as it pushes out DBF around it. Solder fillets are shaped under the balance of the fluidity of DBF and surface tension of the solder. If an amount of the additive is not sufficient for the flux activity of DBF, the growth of the fillet is not enough to get a reliable interconnection (Figure 5). Because the pressure of heat-press in the interconnecting process is low, the thickness of DBF almost does not change, and DBF does not squeeze out. Since the thickness of the solder is held too, the solder forms a steady joint between the layers.

Since DBF is not fully cured by the interconnecting process, the circuit board is post-baked. It is baked at about 180°C, which is below the melting point of the solder, for about an hour. These processes completely bond all layers with each other.

Figure 6 shows a cross sectional photograph of a six-layered SBic fabricated through the processes mentioned above.

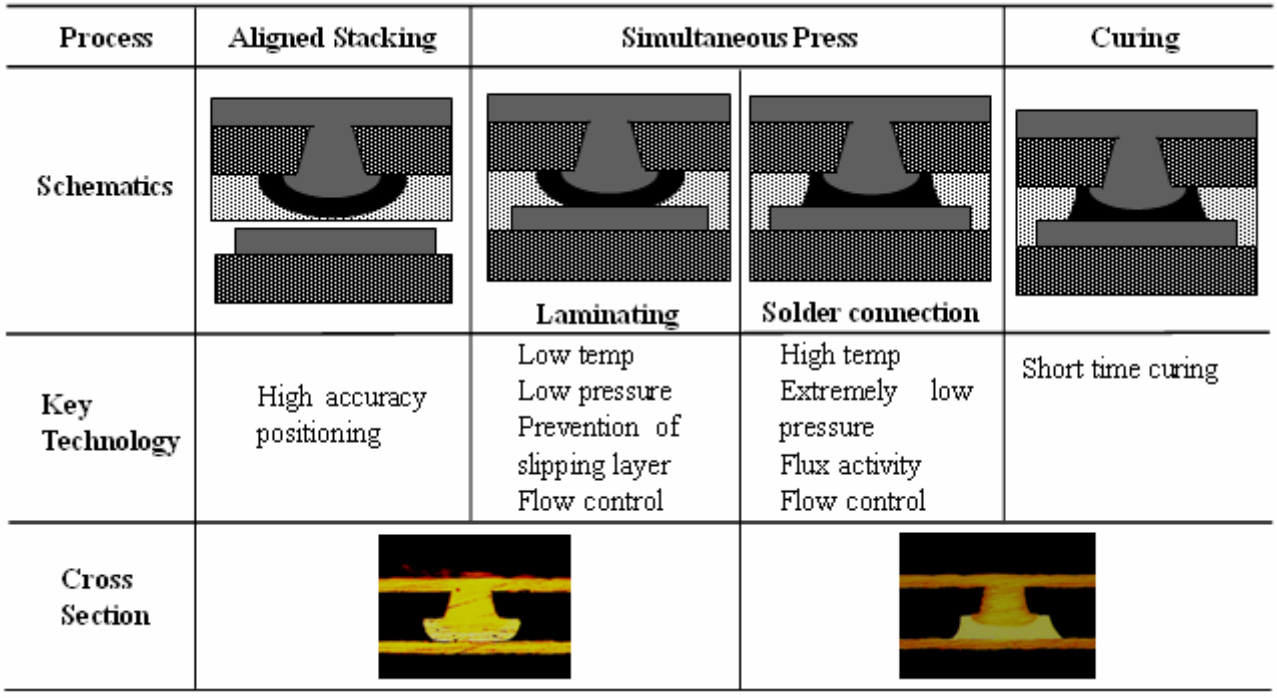
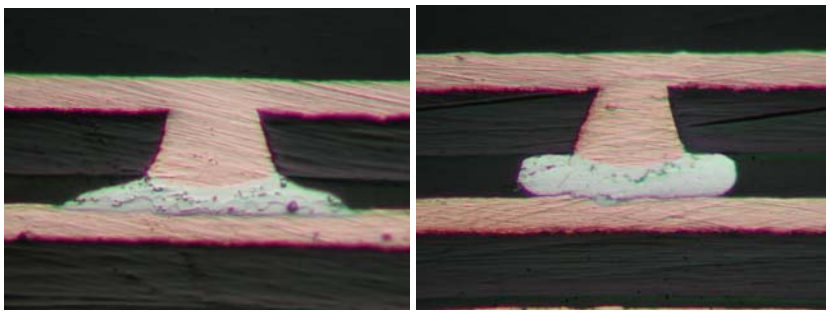


Figure 4 - Simultaneous Laminating Process



Good Shape **Bad Shape**

Figure 5 – Fillet Shape

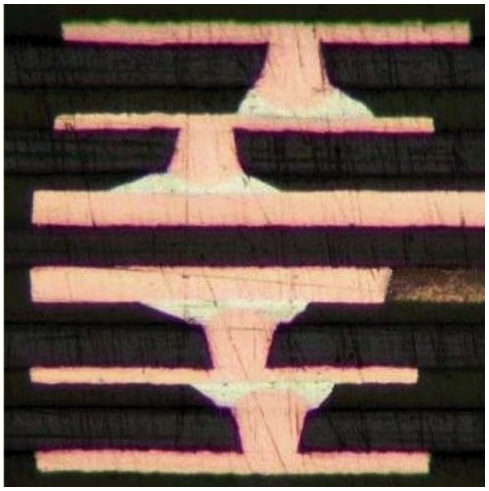


Figure 6 - Cross Section Photograph of 6-Layered SBic

Reliability

We evaluated the reliability of a six-layered SBic that consists of a double-sided FPC as an inner circuit board and two single-sided FPCs each on both sides of the inner circuit board. Reliability of the interconnections is especially important; therefore a thermal shock test and a temperature cycle test were carried out. The specimen has a daisy chain of 480 or 960 bumps (Figure 7). Reliability of the insulation resistance was evaluated by an ionic migration test using two kinds of specimens, which had a comb pattern and a pattern for the evaluation of the bump-to-bump insulation resistance, respectively. One set of specimens was tested without any treatment and the other set was tested after a two-time reflow treatment. The specimens with treatment were heated in a reflow oven above 260°C (up to 265°C) for 15 seconds twice.

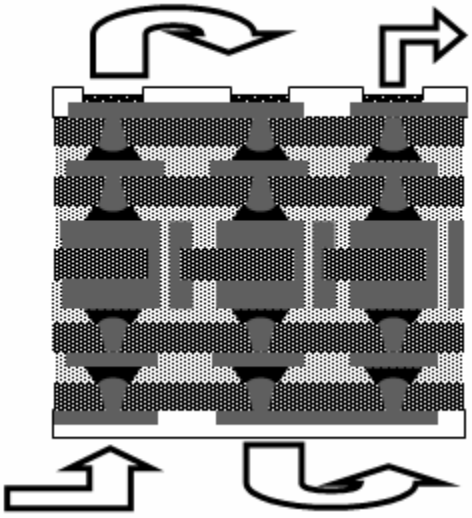


Figure 7 - Daisy Chain of Specimen

In addition, the thermal shock test and temperature cycle test were carried out to evaluate reliability of the interconnections using the specimen with a high temperature storage of 150°C for 500 hours.

Thermal Shock Test
The specimen was immersed in oil of 260°C for 10 seconds and in oil of room temperature for 20 seconds per cycle. After 100 cycles, the change of the total resistance of the daisy chain was measured and the cross section of the specimen was observed. As a result, the total resistance was stable and its change was less than 5%, and no failure like a crack was found in the specimen.

Temperature Cycle Test
The specimen was held at –25°C and 125°C for 9 minutes respectively, and 1000 cycles were done. In this test, the specimen had no failure either, and the change of the total resistance was less than 5%.

Ionic Migration Test
The insulation resistance of the specimen, which was kept in an environment of 85°C and 85%RH and applied 50 V between its electrodes, was measured for 1000 hours.

The comb pattern of the specimen was line/space=75/75 micrometers on the inner layer circuit board and L/S=50/50 micrometers on the outer layer circuit board. The specimen for evaluation of the bump-to-bump insulation resistance had a 300-micrometer space between the bumps and a 100-micrometer space between the circuit lines that were connected to each bump. The circuits on the first layer and sixth layer were covered with solder resist, and the circuits on the other layers were covered with DBF.

During the test, the specimen kept the insulation resistance of more than 10^8 ohm, and it was stable for more than 1000 hours (Figure 8). No failures, like dendrites, were found between the circuit lines (Figure 8A) and the bumps (Figure 8B).

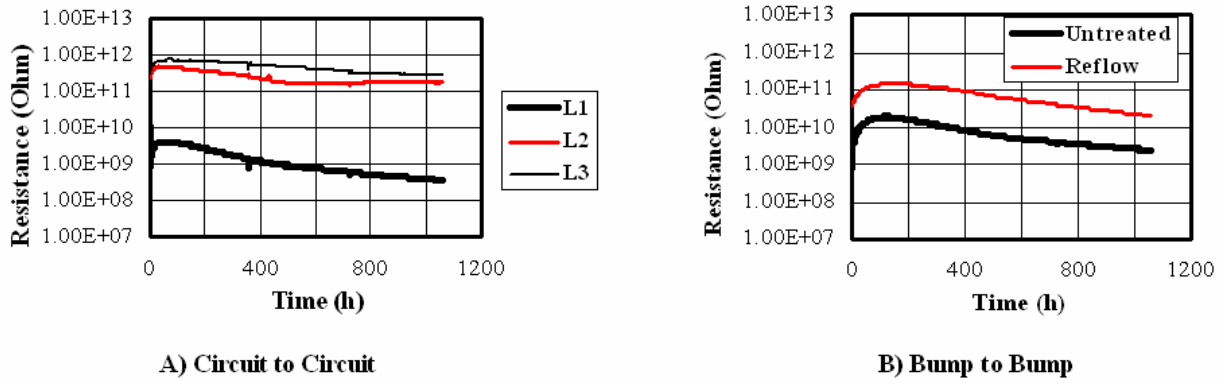


Figure 8 - Insulating Resistance Plot during Ion Migretion Test

Reliability after High Temperature Storage
The resistive change of the specimen after high temperature storage was measured. The conditions were: 200°C for 48 hours, 180 °C for 96 hours, and 150°C for 500 hours. The change of the total resistance was less than 10 %, and no failure was found.

Moreover, reliability of the specimen with high temperature storage of 150°C for 500 hours was examined by a heat shock test and a temperature cycle test.

The change of the total resistance was less than 10 %, and no failure such as a crack or an open circuit was found by microscopic observation of the cross section.

Performance of Solder Interconnection
Alloys between Sn-2.5Ag solder covering the bump and copper of the corresponding pads, interconnect each layer of the SBic. DBF supports the interconnection by its flux activity. Although we were apprehensive of the degradation of the insulation resistance by the dissolution of metal caused by the flux activity, the insulation ability was verified by an ionic migration test. These results show that the SBic has sufficient resistance to ionic migration.

Copper, which is contiguous to tin, diffuses into tin at a high temperature, and an intermetallic compound grows in the solder of the interconnection. This phenomenon continues until all tin changes to Cu_3Sn. We were apprehensive of the degradation of interconnection reliability because the intermetallic compound is harder and less flexible than the original solder. Then its reliability was verified by a heat shock test and a temperature cycle test using the specimen with a treatment of 150°C for 500 hours. The change of the total resistance was less than 10 %. This result shows that a SBic has sufficient reliability. Table 2 shows these results.

Table 2 – Result of Reliability Test

Item		Judgment	Result	
			Untreated	Reflow
Temperature cycle test		Less than 10% resistive change	4.0%	-
Thermal shock test (hot oil)			3.5%	-
High temperature storage	200°C, 48hr		3.3%	4.5%
	180°C, 96hr		2.2%	2.8%
	150°C, 500hr		1.6%	1.9%
Migration test		More than 10^7 ohm	Pass	Pass

Conclusions

We have developed the laminating and interconnecting technology of the multilayer flexible printed circuit board “SBic” suitable for high-density mounting. The results of the reliability tests of its interconnection showed that it has sufficient reliability. Now we are developing technology of mass production in order to respond to the increasing demand for multilayer FPCs, enabling portable equipment, such as cellular phones, digital still cameras and digital video cameras, to achieve high speed, high performance, and smaller dimensions. We started to offer the prototype in 2004, and have a plan to start the mass production in 2005.

References

1. T. Komiyatani, T.Chuma, M. Ishibashi, M. Kato, “Multi-Layer FPC S-Bic for High-Density Device Mounting”, Electronic Parts and Materials, Japan, Vol. 42, No. 10, Oct. 2003, pp.45-49.