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Wiring Process by Electrophotography and Electroless Plating

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Abstract
For the purpose of mask-less manufacturing for Printed Circuit Board (PCB), a new process using electrophotography technology, principle of copy machines, has been proposed and evaluated. Wiring patterns can be formed by electroless plating on the seeding patterns printed with the novel toner that is made of thermosetting resin and metal fine particles. Insulating layer can be also patterned by printing with resin toner. To build up multi-layered structure of PCB, these two processes are repeated in turns. This new method has some big potential to simplify manufacturing process for wiring and reduce the cost of PCB.

The first technical issues were to control electrostatic charge of toner including metal particles and to get enough quality of printed seeding patterns for electroless plating. We started to develop the novel toner from investigating about the relationship between metal contents, electrostatic charge of toner, and plating ability. And it was established that new wiring process using electrophotography is available for PCB tracing. Similarly, insulating single slayer and multi-layered structure were formed by new process and appraised. Additionally, some trial samples by this new process were evaluated by some basic reliability tests. For demonstration, flip chip assembly was carried out and antenna substrates for RFID tags were fabricated.

Introduction
The ratio of PCB cost in electronic components is increasing recently because of the needs of finer wiring design that forced by higher density and miniaturization of IC chips. Therefore, cost reduction of PCB will greatly affect the product competitiveness of electronic components. Conventional manufacturing process of fine wiring PCB needs many complex steps and many exposure-masks for each layer, which have a severe impact on cost and turn around time, from circuit design to product.

In terms of investigation of mask-less circuit patterning, some printing technologies such as inkjet and electrophotography with metal fine particles have been reported.[1, 2] In general, inkjet process needs control of wettability and adhesion onto base material or substrates. Sometimes it may require certain special treatment for the surface of base material. On the other hand, electrophotography process has some difficulties, especially in case of direct metal toner printing, because it needs management of Coulomb force. Few researches with electrophotography approach have been reported. In both technologies for direct metal wiring with metal particles (such as silver), there are some problems to use as PCB. For example:

- Curing in high temperature is needed to form a metal conductivity with metal particles. In many case, the curing temperatures are above 200 °C.
- Since the thickness of metal layer is thin due to the printing process, the electrical resistance is higher than conventional wiring.
- Because there is no adhesion layer between base substrate and metal, adhesion in high temperature especially in soldering processes could not be reliable.

To solve the problems and realize the mask-less manufacturing, new toner is introduced to electrophotography process.

New Process for Manufacturing Printed Circuit Board
Figure 1 shows the outline of the new manufacturing process flow with electrophotography process for PCB. First, the wiring pattern is printed on a base sheet by electrophotography with the thermosetting resin toner including metal fine particles (“seed toner“). This pattern works as seeding layer for electroless plating because of the metal particles, acting as a catalyst, are dispersed and exposed on the pattern. Then, electroless copper plating forms conductive layer on the pattern. In the next step, “insulator toner” with no metal particles is printed with electrophotography again. In order to a build up multi-layer structure, these steps of wiring and insulating layer formations are repeated in turns.

The advantageous characteristics of this process and PCB are,

- Mask-less process by electrophotography.
- Low resistance of metal layer, because of the required thickness deposited by electroless plating.
- Enough adhesion obtained from thermosetting resin in “seed toner”.
- Pattern of insulating layer with via hole is also formed by electrophotography.
- Capability of easier building up the multi-layered

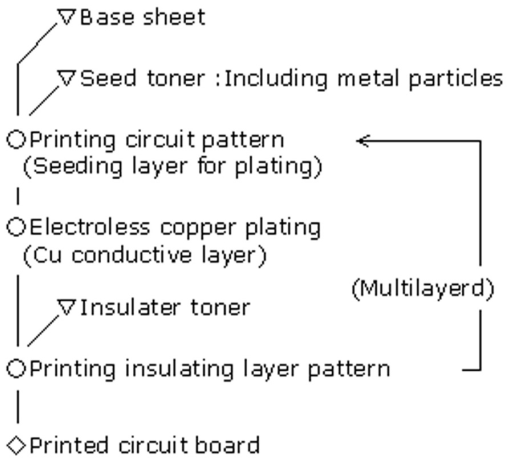

Figure 1 - New Process Flow for Printed Circuit Board

Electrophotography Process and Toner for Seeding Layer Patterning

Electrophotography, in other words "Xerography", is one of the imaging technologies in such as Plain Paper Copier (PPC) machine, which use the photoelectric phenomenon and Coulomb force. The process is explained briefly here. First, whole surface of a photosensitive drum is electrically charged. Next, electrostatic latent image is formed on the drum surface by laser scanning. Then, toner is developed on the latent image because of the toner is charged oppositely to the image on the drum. Finally the toner image is transferred to the sheet and fixed. In these processes, it is the most important to control the electrostatic charge of the toner. If the charge is too large, the pattern image is disturbed because the toners repel each other. On the other hand, if the charge is too small, the pattern is not developed. Moreover, it is important to hold the toner in a charged state appropriately, thus conductive toners, such as metal particles, are difficult to print by electrophotography. However, electrophotography process supplies printing at high speed such as 100 sheets / min directly from digital data. In addition, the electrophotography process has the advantage of easy material design control. Thus the mechanical characteristics and adhesion of the toner are easily controlled because the toner is a solid state material. Accordingly, we have developed "seed toner" including metal fine particle as catalyst for electroless plating so as to take electrophotography technology to a level suitable for fine line PWB manuafcture.[3, 4]

Figure 2 shows the SEM micrograph of seed toner. It is made by almost same process as conventional two-component dry toner. The toner consists of phenol-novolac-epoxy resin and fine particles of copper. This thermosetting resin shows good adhesion between metal layer and base sheet in high temperature such as soldering processes. Copper was selected from the group of metals having good catalysis properties for electroless plating and because of the cost and usability. From some experiments, it was found that there is the optimum trade off relationship between electrostatic charge and copper plating quality to copper content. As a result, copper content of seed toner is selected to be 50 weight%. The printability of seed toner had evaluated with a 600 dpi, monochrome, PPC printer for office use, the printed lines with seed toner shows the resolution as good as conventional black toner. The minimum pitch with this machine is about 300 μm. After 5μm thickness of copper electroless plating, the sheet resistance is 3 - 4 mΩ / Sq. the specific resistance is 2μΩ-cm which is good enough even if compared with pure copper.

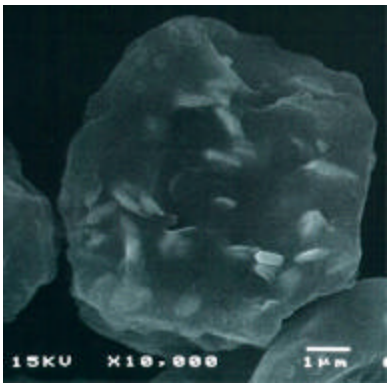

Figure 2 - SEM Micrograph of Seed Toner

Insulating Layer

The insulating layer is also printed with an "insulator toner" consisting of epoxy resin without metal particles. The thickness of printed pattern by electrophotography depends on toner size and setting condition of developing process. The maximum of thickness is around 5 µm in order not to reduce the patterning resolution. However, the insulating layer for PCB requires more thickness because of necessary requirement of good insulation resistance and a reliable protection of the metal layers from corrosion and oxidization. Therefore there is need for repeated printing to get sufficient thickness. Two sizes of toners were prepared and the relation between the pattern thickness and times of printing were investigated. The result is shown in Figure 3. The thickness of 15 µm is achieved with6 times printing with the small toner and with 3 times printing with the large toner.

It is a disadvantage to form insulating layers by printing same patterns repeatedly in the view of the process printing accuracy. On the other hand, the process has some advantages with regard to pinholes besides being a mask-less process. In the field of the printing industry which includes other technologies, the problem of pinholes, especially in case of printing large areas, is often discussed. However, if an insulating layer is formed by the process of piling up a series of thin printed layers, there is little probability of the appearance of a void or a pinhole though all of the layers.

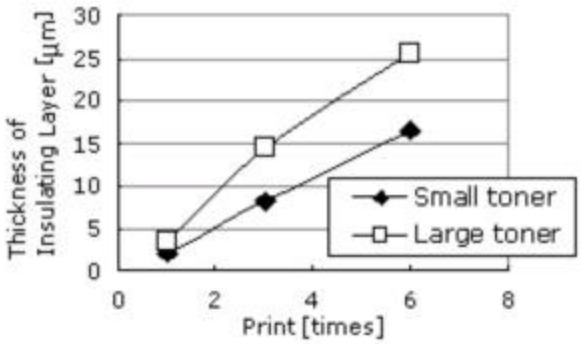

Figure 3 - Number of times of Printing and Thickness of Insulating Layer

Wiring Reliability

The wiring reliability tests as shown in Table 1 were carried out. Pass or fail was judged by electrical resistance (pass criteria is less than 10% resistance change) and visual inspection with a microscope to find cracks, color changes, dendrites and so on. All samples passed as results of the examinations.

Table 1 - Wiring Reliability Tests

Reflow test	260C peak, 8 times	20/20 OK
Moisture absorption Reflow test (JEDEC Level 1)	260C peak, 8 times (85C / 85%, 168h)	20/20 OK
High temperature storage test	150C, 1000 hours	20/20 OK
Temperature cycle test	-55 / 125 C, 1000 cycles	20/20 OK
High temperature bias test	85C / 85%, 20V, 1000 hours	2/2 OK

2nd Copper Layer

The photograph of the via chain between 2 copper layers is shown in Figure 4. It was formed by the new process. The layer construction is done on a glass-epoxy base sheet putting down 1st a copper layer, then an insulating layer and then a 2nd copper layer. The insulating layer pattern has 289 via-holes; the via-hole size is 2 mm and the pitch of holes is 5mm. The copper lines of 1 mm width that connect via-holes are formed in 2 copper layers. The electrical resistance is about 13.5 Ω throughout the chain , 5 - 7 mΩ per a via-hole.

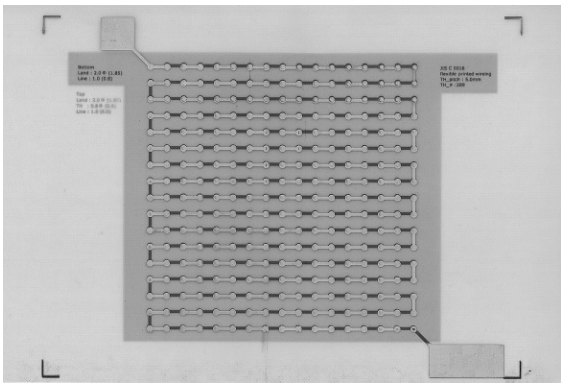

Figure 4 - Via Chain between 1st and 2nd Copper Layers

Flip Chip Assembly

Solderability

Flip chip assembly on PCB samples by the new process was carried out in order to evaluate the soldering ability. The samples have area array bonding pads in 350 µm pad pitch and wires of daisy chains to examine electrical interconnection with test chip. The 15mm sq. size test chip has 1030 solder bumps. The chip is connected with the PCB through conventional Pb free solder reflow process (the peak temperature 260 °C) with flux. Figure 5 shows the cross section of the connected bumps between the test chip and the PCB. Test chip assembly was ensured by electrical resistance check of daisy chains and by observation of fracture mode by destructive testing. As a result, all bumps on the 10 samples had good connections.

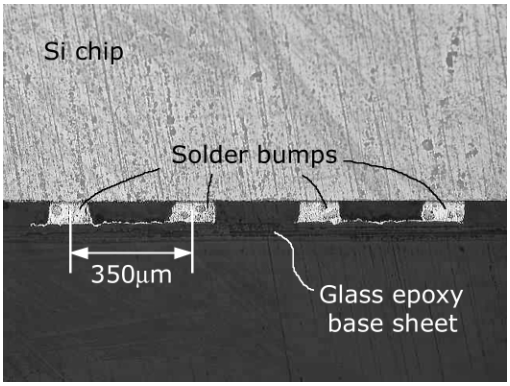

Figure 5 - Cross Section of Flip Chip Assembly (Solder bumps)

Anisotropic Conductive Film (ACF) Bonding for RFID Tag Antenna

For another demonstration, the antenna substrate of RFID tag was constructed. A general-purpose RFID IC chip is about 2 mm Sq.; it has gold bumps made by electrode plating. The chip was connected onto the tag antenna by flip chip bonding with ACF. Figure 6 shows the cross section of an assembled sample. It indicates that gold bump connected successfully to the antenna pattern with ACF.

The resonant frequency of the tag depends mainly on the shape of antenna. The antennas, for 5 kinds of design ("a" to "e"), were prepared for optimizing the resonant frequency by slightly changing the CAD design of antenna pattern. The proportional relation between designed and experimental data is shown in Figure 7. The resonant frequency of design "d" is most suitable for the target frequency of 13.56 MHz.

For some kinds of tag antenna substrates that have several capacitors in them and during the trimming process some of capacitors is cut off in order to fit the resonant frequency to the target after assembly. In contrast, it is really easy to change designs in the new process because now it is possible to print patterns from CAD digital data to fit the individual characteristic of each IC wafer lot. It is also easy to produce a small quantity of products and change designs so as to follow the refinement of the IC's design.

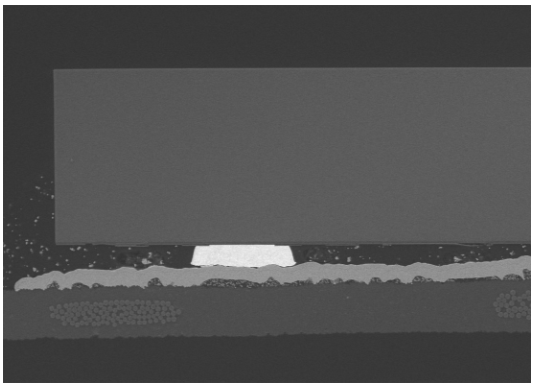

Figure 6 - Cross Section of Flip Chip Assembly (ACF Contact)

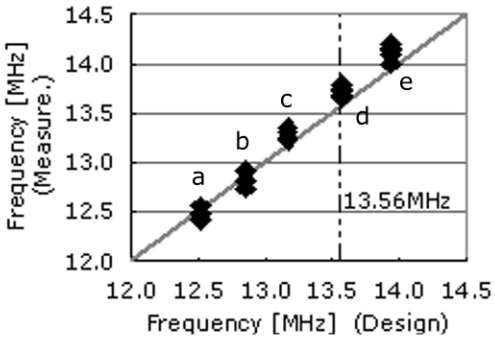

Figure 7 - Antenna Design and Characteristic Frequency

Conclusion

A new manufacturing process for Printed Circuit Board using electrophotography and electroless plating has been proposed and evaluated. Without any mask, wiring, insulating layers and via-chain between 2 layers of Cu were easily fabricated. The conductive layers show good electrical characteristics, the specific resistance is about 2mW-cm, and good reliability. Moreover, the result of experiments with flip chip assembly indicates good soldering and ACF bonding ability for this process. Consequently, an RFID tag could be fabricated with an antenna substrate with this new mask-less process and operated with good performance. The "On-demand" characteristic of electrophotography makes it easy to optimize the antenna design by changing CAD data. Good performance of PCB fabricated with the proposed process was demonstrated.

Acknowledgments

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