Presented in the ECWC 10 Conference at IPC Printed
Circuits Expo®, SMEMA Council APEX® and
Designers Summit 05

Electrical Behavior of Thin Film Embedded Decoupling Capacitor in Printed Circuit Boards

Seokkyu Lee, Jongkuk Hong, Changsup Ryu, and Byungkook Sun
Samsung Electro-Mechanics Co., Ltd.
Suwon, Korea

Hyungsoo Kim and Joungho Kim
Korea Advanced Institute of Science and Technology
Daejon, Korea

Abstract
In this study, we developed the thin film embedded decoupling capacitors and experimentally investigated its electrical behavior in terms of power-ground impedance and simultaneous switching noise (SSN). Several test vehicles and network system boards were fabricated and the effectiveness of embedded decoupling capacitors was compared with that of discrete surface mounted (SMT) ceramic capacitors. For the test vehicles, five types of embedded capacitance materials were used, with various capacitance densities ranging from 0.45 to 12nF/in^2. According to the frequency and time domain measurement of power-ground impedance and SSN, the better performance was obtained as the distance of power-ground decreases while capacitance value increases. In the high-speed system boards evaluation, the embedded capacitor board showed lower radiated electromagnetic interference (EMI) by about 10dB μV/m compared with the conventional board with SMT ceramic capacitors especially in the higher frequency range over 1GHz. The construction design for the embedded capacitance board and reliability guideline will be also presented.

Introduction
Until now, the speed of LSIs has increased dramatically. To meet this trend toward higher speed, more power consumption and lower supply voltages in high-end computers and networking systems, more stable power distribution network (PDN) strongly required for the high-speed digital integrated circuits (IC's) operating properly.[1-4] However, it has not been an easy way to get the stable PDN without decreasing the overall impedance between the power/ground network impedance. Thus, it can also prevent the simultaneous switching noise (SSN). The SSN is mostly generated by the parasitic inductance due to the interconnections like via holes including the configurations, pins and bond-wires.[5] The SSN can be defined as:

$$\text{Simultaneous Switching Noise (SSN)} = \Delta V = L\,(\Delta I / \Delta t)$$

In this formula, V is the voltage, L is the parasitic inductance, I is the current and t is the clock frequency of the systems.

To mitigate this power bus noise (Delta V) by isolating the parasitic inductance of the PDN, decoupling capacitors with low impedances and low inductances have been intensively used. Currently, the decoupling capacitors are placed on the PCB as multilayer ceramic capacitors (MLCC), on the package as like low inductance ceramic capacitor (LICC) operating roughly from 10 up to 50MHz and on the chip levels as internal capacitors operating at higher frequencies over multi-hundred MHz respectively.[2, 6] Figure 1 shows the roles of different decoupling capacitors placed on the different location depending on the impedance paths (Z). By placing many different decoupling capacitors with various impedance paths in parallel on the different levels respectively, the total impedance can be below the target impedance across the wide frequency range. In particular, a large number of ceramic chip capacitors like MLCC and LICC have been widely used on the PCB mother board and package level to mitigate a sudden voltage drop by supplying proper current to micro processors having high speed clock rates because of its cost effectiveness and re-workable merits during surface mounting process. However, not only as the clock frequency and its harmonics are increased over GHz frequency range, but also the space for mounting chip capacitors including chip resistors and inductors is constantly decreased, those discrete decoupling capacitors are no longer effective for satisfying the trend of high speed and size reduction of high-performance applications.[1, 7]

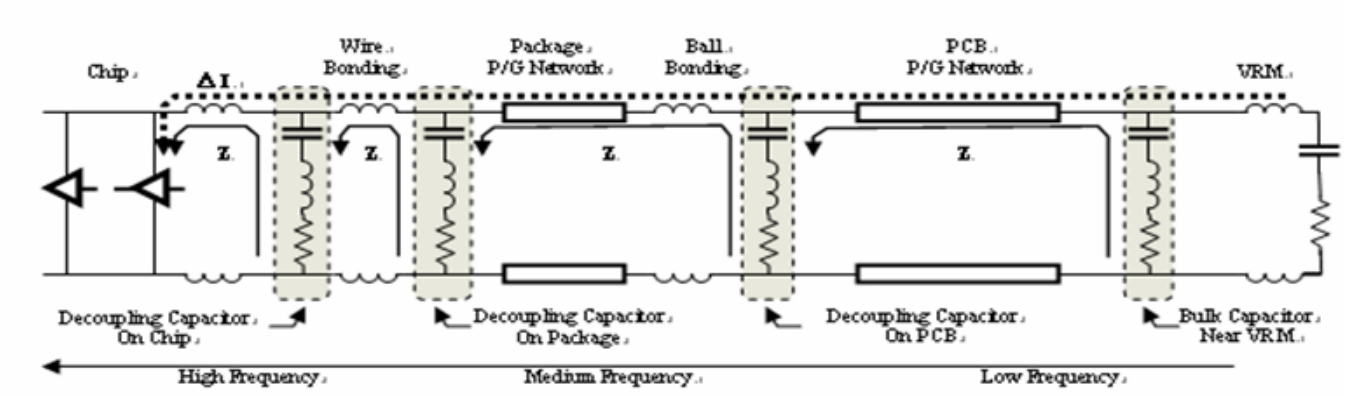

Figure 1 - Simplified Circuit Schematic[8]

On the other hand, as described above, on-chip decoupling capacitors with high capacitance, low ESR and low ESL placed in the LSIs can be still powerful to come up with the very fast clock rates. However, the high manufacturing cost, long fabrication lead-time, low design freedom and low processing yield are major bottlenecks for the on-chip decoupling capacitors to overcome. Thus, both of these discrete ceramic decoupling capacitors and on-chip capacitors have advantages and disadvantages respectively.[1, 7]

As an alternative solution to provide the low noise digital power/ground network and low manufacturing cost together, embedded capacitance thin film is strongly emerging, to exhibit better noise performance (lower impedance and consequently smaller SSN) at high frequency range over GHz. These effects are expected by the help of low inductive power/ground current path to remove the excessive inductances of the discrete decoupling capacitors, long through vias, mount pads, and traces.[2, 5, 7]

In this paper, we have experimentally investigated the effectiveness of the thin film embedded capacitor in terms of frequency and time domain measurement of power/ground impedance and Simultaneous Switching Noise (SSN). This paper is organized as follows. In the next section, fabrication of the test vehicles including the embedded thin film capacitance materials is briefly described. Some representative measured power/ground impedance and the simultaneous switching noise (SSN) results of the test vehicles are shown in the following sections. Some reliability test results of the test vehicles regarding environmental and electrical reliability. Finally, we successfully demonstrated the EMI characteristics using a 14-layer system board having two high capacitance and very thin power/ground cores compared with 12-layer conventional system board without any embedded capacitance material at a same time.

Fabrication of the Test Vehicles

To experimentally demonstrate the effectiveness of the thin film embedded capacitor, two pairs of thin film layers (copper clad laminate type, 5cm by 5cm) were inserted to conventional 4-layer PCB whose size was 6cm by 9cm as shown in the Figure 2-(a, b) and Figure 2-(c, d) shows the cross-sections of a test vehicle using 12μm thin film embedded capacitance material. The five different materials (EC-A~E) as thin film embedded capacitor are described in Table 1.

For measuring the power/ground impedance (frequency domain) and SSN, we used Agilent 8753D vector network analyzer with Cascade FPC series G-S probe system and Agilent 54616B digital oscilloscope (500MHz bandwidth) with high impedance probe respectively. ALTERA was mounted on test vehicle and was programmed as eight clock drivers with frequency of 50MHz to generate SSN on the power/ground network.

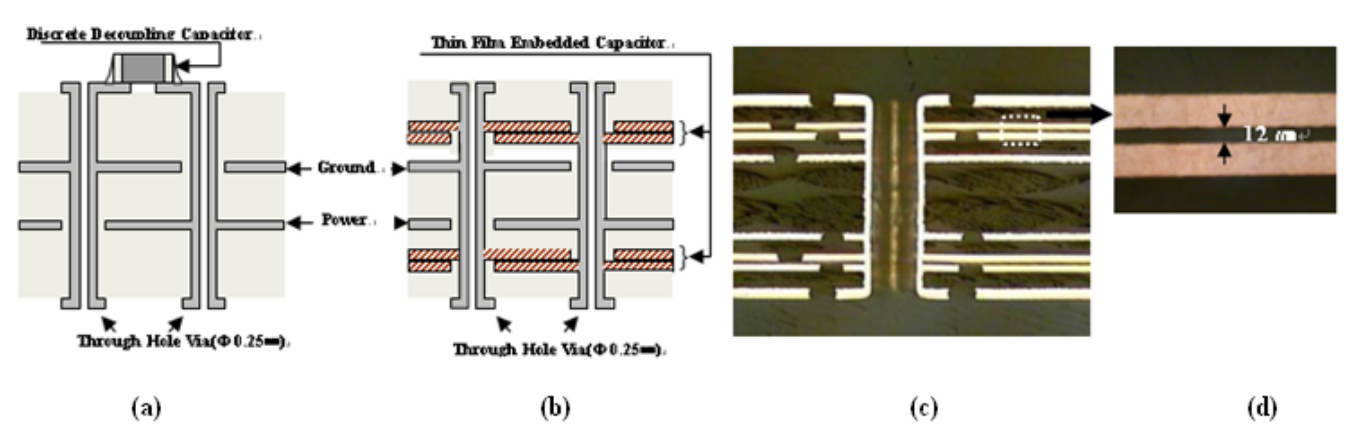

Figure 2 - Schematic of Test Vehicles with (a) Discrete Chip-Type Decoupling Capacitor and (b) Embedded Capacitor Film - Cross-Section of (c) 8 Layer Test Vehicle Using (d) 12μm Thin Film Embedded Capacitance Material

Table 1 - Thin Film Embedded Capacitance Materials Evaluated in this Study

Item	EC-A	EC-B	EC-C	EC-D	EC-E
Resin	Epoxy	Epoxy	Epoxy	Epoxy	Epoxy
Reinforcement	106E glass	No	No	High Dk filler	High Dk filler
Dielectric Thickness (㎛)	50	24	12	16	12
Capacitance (nF/in^2)	~0.5	~1.0	~2.1	~6	~12
Dk	3.9~4.1	4.4~4.6	4.4~4.6	16~18	25~30
Df	0.012~0.015	0.012~0.015	0.012~0.015	0.004~0.005	0.014~0.015

Measured Power/Ground Impedance and Simultaneous Switching Noise of Test Vehicles

In general, the higher capacitance of discrete decoupling capacitors lower the power/ground impedance in the frequency range from its self resonance frequency (SRF) to the frequency below GHz. However, there is no big power/ground impedance difference between the boards with discrete decoupling capacitors and without them over 500MHz as shown in Figure 3-(a). That is because of the inductive property of the impedance introduced by its mount pads, traces and vias. Unlike the discrete decoupling capacitors, the significant reduction of the power/ground inductive impedance over GHz was measured by adopting thin film embedded capacitor which has even very low capacitance about one-thirties of the discrete decoupling capacitor as shown in

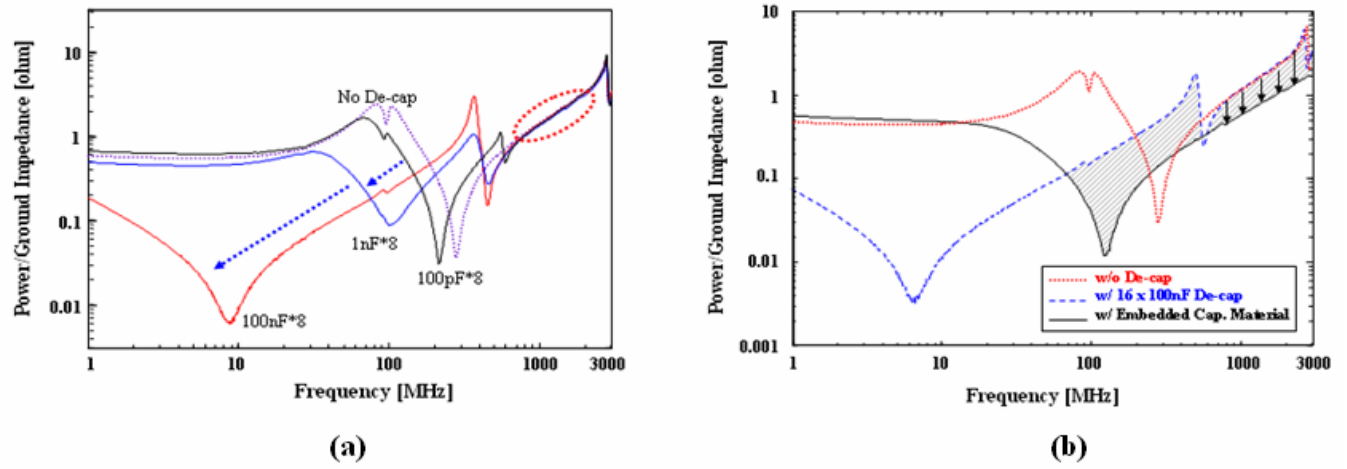

Figure 3-(b). So its benefit just appears from 60MHz and significant reduction of the P/G inductive impedance is confirmed by using the thin film embedded capacitor up to 3GHz frequency range. Similar to the result of discrete capacitors earlier, the higher embedded capacitance lower the power/ground impedance in the low frequency range while the thinner power/ground spacing of the thin film embedded capacitor can obtain the lower power/ground impedance in the high frequency range as shown in Figure 4-(a). These electrical behaviors in high frequency region can be described by the help of reducing the parasitic inductance of power/ground plane itself that can be formulated by this equation:

$L_{Plane} = \mu_o * h$

where L_{Plane} is the inductance of plane, $\mu_o = 4\pi 10^{-7}$[H/m] is the permeability of vacuum, h is the thickness of planes.[4] In brief, the lower power/ground impedance can be achievable in the wide frequency range by applying the higher capacitance and the thinner power/ground spacing of thin film embedded capacitors. Figure 4-(b) shows the power voltage fluctuations of the test vehicles employing three different thin film embedded capacitors (EC-C, D, E), with the sixteen 100 nF discrete decoupling capacitors and without any discrete or thin film embedded capacitor.

This study using test vehicles demonstrate that the thin film embedded capacitors have better high frequency performance than that of the discrete decoupling capacitors. It will be confirmed by the real case study using 14-layer system board having two high capacitance and very thin power/ground cores in section V.

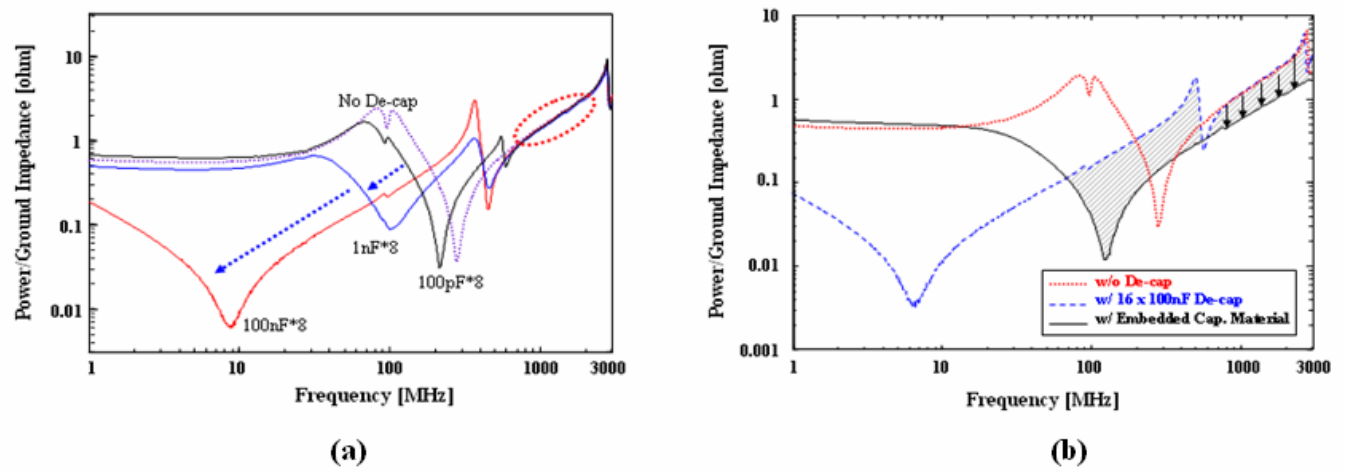

Figure 3 - Measured (a) Power/Ground Network Impedance Curves Depending on the Different Discrete Capacitors (b) P/G Network Impedance Curves without any Decoupling Capacitor (Dotted Line), with the Sixteen Discrete Decoupling Capacitors (Dashed Line), and with the Embedded Capacitor Film (Solid Line)

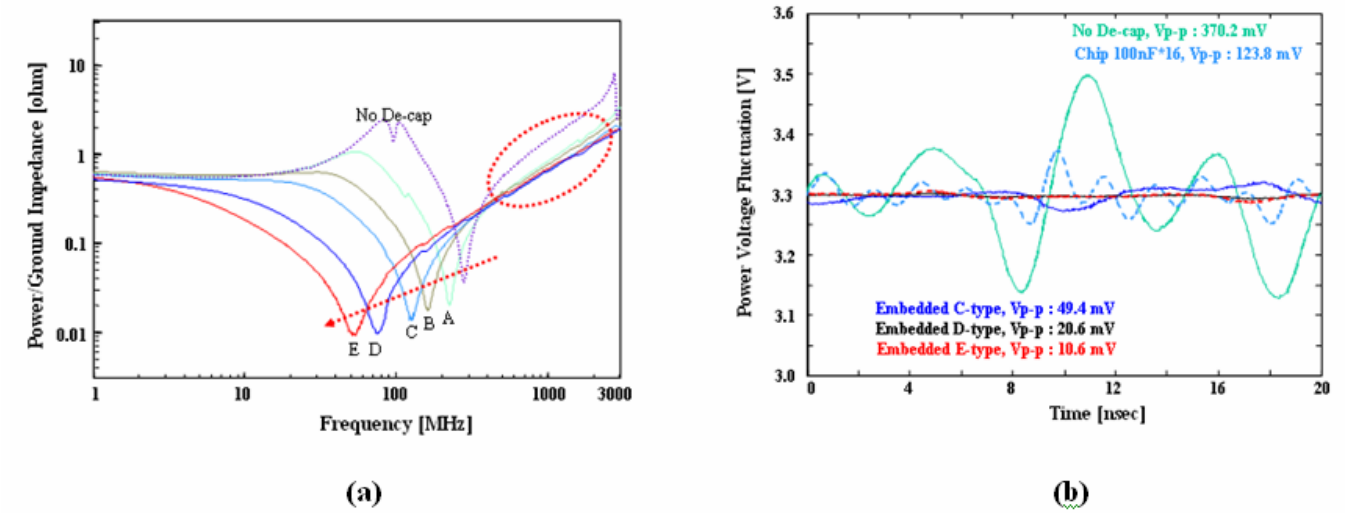

Figure 4 - Measured (a) Power/Ground Network Impedance Curves and (b) Time-Domain P/G SSN Depending on the Different Thin Film Embedded Capacitors

Reliability of Test Vehicles

The reliability of the test vehicles comprising five different thin film embedded capacitance materials was evaluated as listed in Table 2. All of them have passed the tests and we found that these materials are quite reliable to be fabricated in real PCB products.

Table 2 - Reliability Tests Item and Results

	Item	Condition	Results
1	Solder pot	Floating: 288 °C 10sec 1cycle	OK
		Dipping: 260°C 10sec 1cycle	OK
2	Highly-Accelerated Temperature and Humidity Stress test (HAST)	130□, 85%, 96Hr	OK
3	Liquid to Liquid Thermal Shock (LLTS)	-55°C (5min) ~ +125 °C (5min) 100cycle	OK
4	Temperature Humidity Bias (THB)	85 °C, 85%RH, DC3.3V, 168Hr	OK
5	Withstanding Voltage	Keeping time (30sec), Leakage current spec. (0.1mA), Ramp rate: 10 V/sec	Over 150V
6	Temperature Coefficient of Capacitance (TCC)	-55 °C ~ +125 °C	±15% ~ ±20%

EMI Behavior of 14-Layer System Board Having Thin Film Embedded Capacitors

To investigate the effect of thin film embedded capacitor, we fabricated a 14-layer system board having two high capacitance and very thin power/ground cores. The design of the 14-layer board was modified from the original that has 12-layer system board (W*L*T=35*25*1.96 mm) operating at 2.0 GHz without any embedded capacitance material. We added the ground and power one more respectively. Then, we examined the EMI noise at a same time. Figure 5 shows the cross-section of the 14-layer system board (W*L*T=35*25*2.05 mm) and thin film embedded capacitor also.

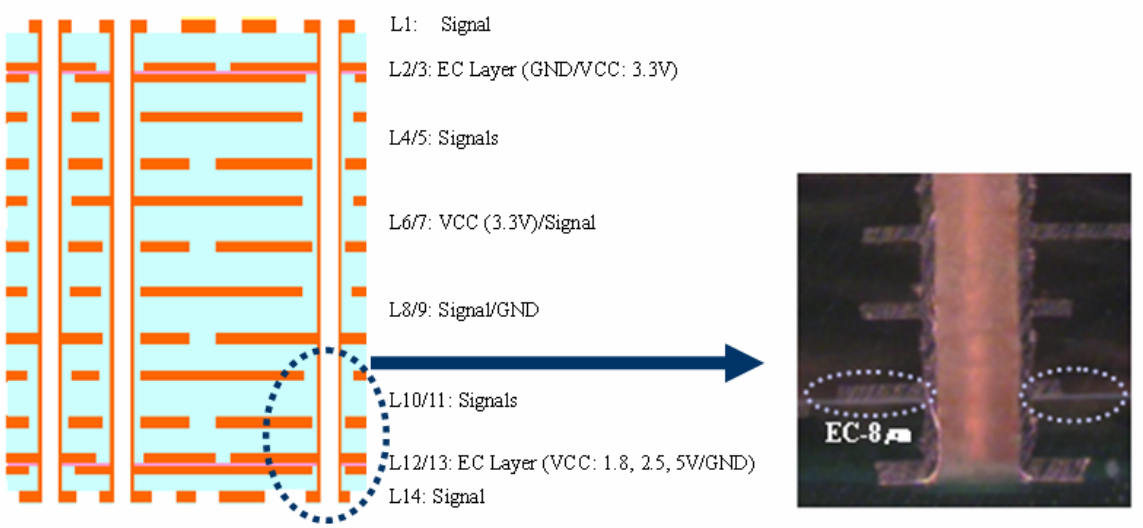

Figure 5 - Schematic of 14-Layer Board and the Cross-Section of the Part (10~14 layer)

We substituted the two general power/ground cores with very thin power/ground cores (8μm) and high capacitance ceramic-loaded material (10nF/in^2) by inserting them into layer 2~3 and 12~13 to replace the 529 ea discrete decoupling capacitors Description: C-CERAMIC, CHIP, 100NF, 10%, 50V, X7R, TP, 2012) on the conventional 12-layer board. The replaced capacitance by the very thin and high Dk embedded capacitor is 78% (52,900 nF) of the total discrete chip capacitors as listed in Table 3.

Table 3 - Discrete Capacitors vs. Thin Film Embedded Capacitor

Powers	12-layer System Board (Discrete Capacitance)	14-layer EC System Board (EC Capacitance)	Remarks (De-cap:EC)
1.8 Volt	10,800 nF (108ea)	271 nF	2.5%
2.5 Volt	6,300 nF (63ea)	330 nF	5.2%
3.3 Volt	33,800 nF (338ea)	962 nF	2.8%
5.0 Volt	2,000 nF (20ea)	406 nF	20.3%

Total	52,900 nF (529ea)	1,969 nF	Chip Cap:EC = 100:3.7

After assembling the conventional 12-layer system board with about 1,340 SMT parts including discrete chip capacitors and the 14-layer embedded capacitance (EC) system board without them, we did the EMI test respectively as shown in Figure 6. The EMI behaviors are almost similar below 600MHz. However, the 14-layer EC board has lower EMI by about 10dBμV/m compared with the conventional 12-layer board with SMT ceramic chip capacitors especially in the higher frequency range over 1GHz up to 4GHz. These results illustrate that the thin film embedded capacitors have better electrical performance as investigated in the test vehicle studies earlier.

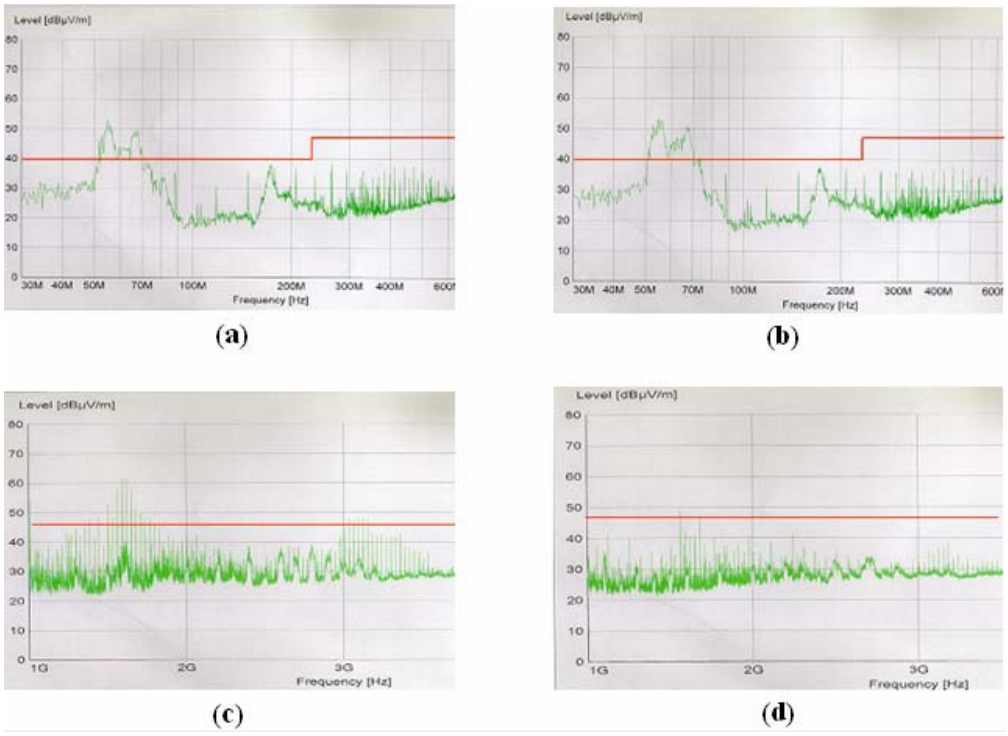

Figure 6 - EMI Noise (a) 12-Layer (b) EC 14-Layer at 30~600MHz Respectively and (c) 12-Layer (d) EC 14-Layer at 1~4GHz Respectively

Conclusion

In this paper, the electrical performance of various thin film embedded capacitor PCB's in terms of power-ground impedance and simultaneous switching noise (SSN) has been discussed. From the test vehicle study, thin film embedded capacitor has exhibited significant improvement of the power/ground impedance and consequent suppression of SSN over GHz. Also, we have confirmed experimentally the various thin film embedded capacitance materials are fairly reliable for the real applications. Furthermore, we successfully demonstrate the effect of thin film embedded capacitor board that has lower EMI noise over GHz than that of the conventional board despite the smaller capacitance. Due to its low inductive property, the thin film embedded capacitors will be exceedingly required as the speed of system increase continuously.

Acknowledgement

The authors would like to thank Changhyun Nam who is author's colleague and supported the 14-layer EC system board evaluation.

Background

This work has performed by help of the Terahertz Interconnection and Package Laboratory (Tera Lab.) in KAIST (Korea Advanced Institute of Science and Technology) with the supports from some material suppliers which have developed thin film type embedded capacitance materials. The purpose of this study is to examine the effect of embedded capacitance materials as R&D.

References

1. Yoshihiko Imanaka, Takeshi Shioga, and John D. Baniecki, “Decoupling Capacitor with Low Inductance for High-Frequency Digital Applications”, FUJITSU Sci. Tech. J., vol. 38, no. 1, pp 22-30, June 2002.
2. An Madou, and Luc Martens, “Electrical Behavior of Decoupling Capacitors Embedded in Mutilayered PCBs”, IEEE Trans on EMC, vol. 43, no. 4, November 2001.
3. Larry D. Smith, Raymond E. Anderson, Douglas W. Forehand, Thomas J. Pelc, and Tanmoy Roy, “Power Distribution System Design Methodology and Capacitor Selection of Modern CMOS Technology”, IEEE Trans on AP, vol. 22, no. 3, August, 1999.
4. Istvan Novak, “Reducing Simultaneous Switching Noise and EMI on Ground/Power Planes by Dissipative Edge Termination”, IEEE Trans on AP, vol. 22, no. 3, August, 1999.
5. M. Xu, T.H. Hubing, J. Chen, T.P. Van Doren, J.L. Drewnial, and R.E. DuBroff, “Power-Bus Decoupling with Embedded Capacitance in Printed Circuit Board Design”, IEEE Trans on EMC, vol. 45, no. 1, pp 22-30, February 2003.
6. JH Kim, BK Choi, HS Kim, WH Ryu, and JH Kim, “Separated Role of On-chip and On-PCB Decoupling Capacitors for Reduction of Radiated Emission on Printed Circuit Board”, IEEE International Symposium on EMC, vol. 1, pp 531-536, August, 2001.
7. HS Kim, YC Jeong, JB Park, SK Lee, JK Hong, YS Hong, and JH Kim, “Significant Reduction of Power/Ground Inductive Impedance and Simultaneous Switching Noise by Using Embedded Film Capacitor”, Electrical Performance of Electronic Packaging, pp 129-132, October, 2003.
8. Figure 1 Courtesy: Tera Lab.