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Design for Manufacture – Ceramic Thick-Film Embedded Capacitors

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Abstract
Embedding discrete capacitors right into printed circuit boards (PWB), although not new, is part of a pivotal technology for the PWB industry. For example, the ability to locate decoupling capacitors within a couple hundred microns of semiconductor I/Os can greatly improve response time and signal integrity. One crucial packaging need, however, is high capacitance density. High capacitance density can only be readily achieved by ceramic capacitor technology. Therefore, the focus of this work has been to develop materials and methodologies to embed high capacitance ceramic capacitor layers inside the layers of the printed wiring board.

Most research in embedding high capacitance ceramic capacitors layers directly into printed wiring boards has focused on forming capacitors on metal foil at high temperatures. It has generally been assumed that demonstration of good properties of these "fired-on-foil" capacitors is all that is necessary to be successful. However, in our experience, the greatest challenges to reliably embedding ceramic capacitor layers inside printed wiring boards reside in the design of the circuit containing embedded capacitors and the PWB embedding process. Not only does the PWB process have to contend with additional tolerance issues but, depending upon design, the capacitor may be subjected to aggressive processes and chemicals that may affect its mechanical or chemical integrity. It is, therefore, incumbent upon the designer to design circuits that can be reliably made by a PWB shop. This paper discusses these issues and gives some guidelines for design for manufacturing.

Introduction
The current work began as part of the Advanced Embedded Passives Technology (AEPT) consortium and was co-funded by the National Institute of Standards and Technology of the U.S. Government and industry participants[1]. Objectives included the development of a process and materials system that would allow ceramic components with high capacitance density to be buried inside PWBs. A ceramic thick-film approach was chosen for embedding ceramic capacitors. The capacitor material system is based on a doped barium titanate and glass composition and works together with a cofired copper electrode paste. The system has a dielectric constant of approximately 3000 and achieved a capacitance density of approximately 1.5 nF/mm.[2]

The process flow for embedding ceramic passives has been documented elsewhere.[2-5] In brief, it uses the fired-on-foil approach. A thick-film capacitor dielectric and electrode paste is screen printed on to copper foil in the locations desired in the circuit and fired in nitrogen at approximately 900°C to form the fired-on-foil components. Following this, the foil may be treated to improve adhesion to prepreg and then it is bonded component face down, into a laminate structure used to fabricate innerlayers for a multilayer printed wiring board (MLB). This innerlayer is then etched to form the capacitor electrodes from the copper foil and any associated circuitry and revealing the capacitors inside the organic matrix. Following this, the inner layer may receive additional treatments before it is incorporated inside a multilayer printed wiring board. The MLB may also be subject to additional treatments, such as plating, after multilayer lamination. Figure 1 illustrates a typical process flow for making and incorporating an inner layer into an MLB.

Manufacturing Processes Effects on Capacitor Design Processes
Since the designer has to design the embedded capacitors rather than pick them from a supplier's catalogue or library of standard parts, more work is required. It would have been an impossible task if, at the introduction of SMT resistors and capacitors, for the designer to design (for manufacturing) every SMT resistor or capacitor to be placed on a board. To do that, the designer would have to have developed a good level of understanding of resistor and capacitor manufacturing processes. Fortunately, the part suppliers developed and provided the information on properties, dimensions, foot print requirements and part libraries. CAD providers later incorporated this information into the CAD systems including libraries, placement and routing.

Designing embedded capacitors today requires a lot of manual design work as CAD tools are not readily available. The capacitance density value of the dielectric allows for capacitor dimensions to be easily calculated but additional items issues exist. The following is a discussion of some of those issues.

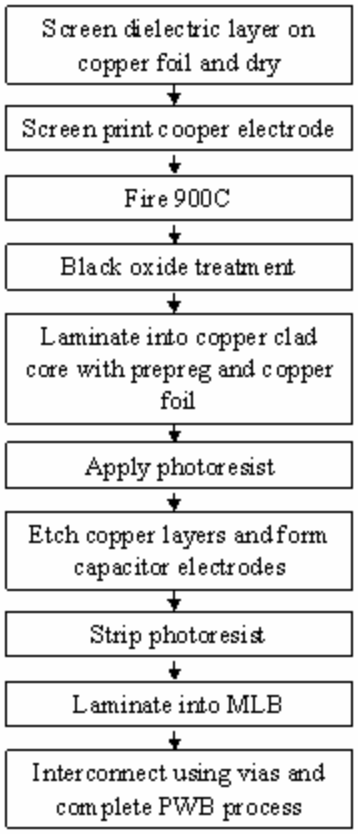


Figure 1 - Typical Process Flow for Embedding Ceramic Capacitors into PWBs

Tolerances

When electro-deposited copper foil is fired at 900°C, it increases in density and undergoes shrinkage. The amount of dimensional change depends on dielectric coverage and the number of firings. Figure 2 shows the data taken from three replicate measurements on four identical foils taken through four firing steps for an Oak-Mitsui PLSP grade copper foil. It is important to understand the effect of these dimensional changes as in the merging of the fired-on-foil and the PWB process they establish and limit the design guideline for size, positioning and termination of the ceramic embedded passives.[5]

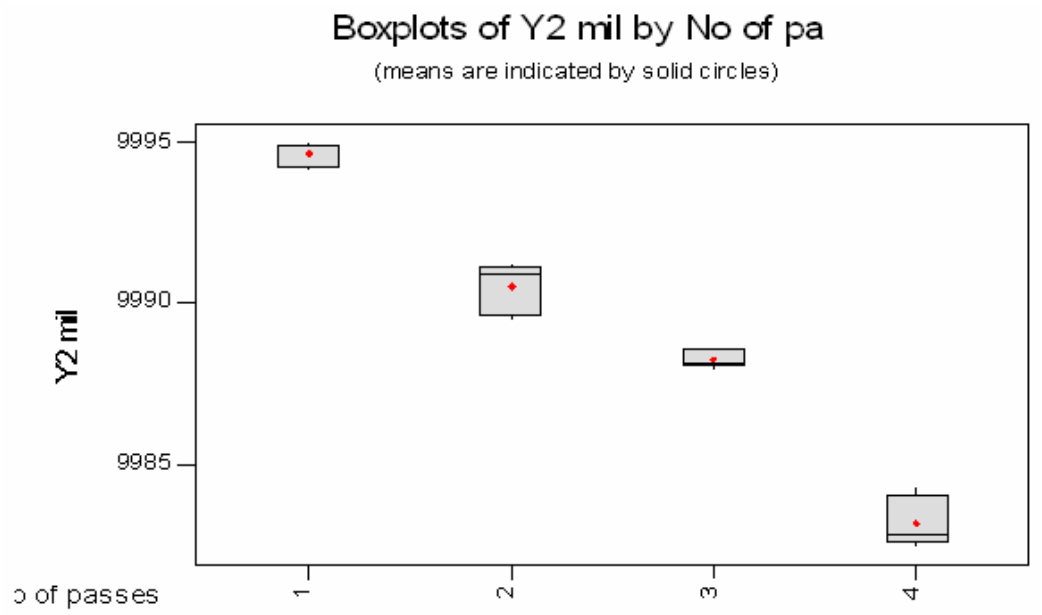


Figure 2 - Movement in One Direction (Y2 Is Shown Here) Upon Successive Firings at 900°C

In the PWB manufacturing process, there are 9 primary operations that have dimensional tolerances associated with them. These are shown in Table 1.

Table 1 - PWB Dimensional Tolerances

Well established processes	Mfg. tol. (+/-µm)
CAD inputs and conversion	Virtually perfect
Laser plotter accuracy	6
Mylar film stability	25
Inner layer side-to-side	10
Outer layer photo-tool punching	13
Post etch laminate shrinkage	75
Post etch tooling hole punching	13
Lamination pinning error	13
Laminate instability during press cure	63

Without going into the details of each one of these steps, the sum of the nominal tolerances is over +/-200µ. The largest contributor is post etch laminate shrinkage which alone can be up to +/-75µ. Shrinkages can be as much as 1mm across a 60cm panel or as little as 50µ across a panel. To complicate matters, some constructions can grow rather than shrink. Without exception, all PWB manufacturers scale artwork based on the predicted shrinkage/growth of the laminate material after etch and lamination. Scaling transfers a larger/smaller image to the copper clad laminate such that, after etch, it will shrink/grow to size. Once the laminate material is characterized, its shrinkage/growth behavior is reasonably predictable. The reality is that tolerances do not all go in one direction so, statistically, any point of the image (after scaling) will fall within +/-75µ of where we want it. This is consistent with IPC 2221 Complexity Level C, High Design Complexity – Reduced. Level B, Moderate Design Complexity – Standard, is +/-100µ.

In the ceramic thick-film process, there are several operations that have dimensional tolerances associated with them. These are shown in Table 2.

Table 2 - Thick-Film Dimensional Tolerances

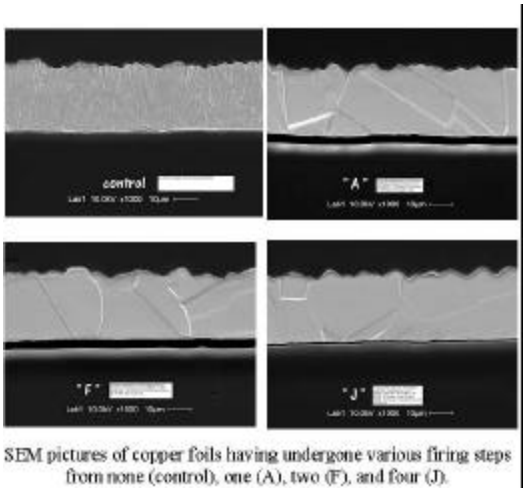
Not as well established	Mfg. Tol. (+/- µm)
CAD inputs and conversion	6
Laser plotter accuracy	25
Mylar film stability	75
Screen preparation	25
Screen print dimensional variation (foil 1 to foil n)	25
1st value print to 2nd and subsequent value prints	25
Foil stability during firing	50
Foil stability during lamination	75

The sum of these thick-film tolerances is over +/-225µ but, like the PCB image tolerances, the ceramic position tolerances do not all go in one direction so, statistically, any point of our image will probably fall within +/-100µ of where we want it.

The next step is to register the circuit pattern to the ceramic capacitor electrode termination pattern. The board manufacturers' ability, therefore, to register the copper circuit image to the electrode termination image using x-ray and optical registration tools is the sum of the PWB process and the thick film process tolerances or approximately +/-175µ. This means that, to be sure that the circuit pattern aligns to the ceramic electrode termination pattern, features sizes to be merged must be 350µ or larger[6].

Other Copper Foil Issues

During firing, the copper foil also becomes annealed. Figure 3 shows scanning electron microscope cross-sectional pictures of grain sizes of copper foil before and after up to three firings. Significant grain growth has occurred in the copper after the first firing. Such large grain sizes cause two issues. The copper foil becomes very soft and handling becomes quite difficult. Any damage that occurs during handling leads to an apparent "shrinkage" much greater in magnitude and more variable than the real shrinkage.



SEM pictures of copper foils having undergone various firing steps from none (control), one (A), two (F), and four (J).

Figure 3 - Copper Foil Before and after Firing

Thinning processes often used in the PWB industry to reduce the thickness of the copper foil also becomes very uneven. When copper foil with such large grains is thinned using hydrochloric acid based etching solutions, preferential dissolution of the copper along the grain boundaries occurs. If copper is excessively thinned, the etching solution can punch through the copper to the dielectric in areas where grain boundaries run entirely across the foil.

Effects of PWB Chemicals On Capacitor Properties

Table 3 lists the various processes and the associated chemicals used in fabricating PWBs. The foil containing the fired-on-foil ceramic capacitors may be required to have an adhesion treatment to improve its adhesion to the laminate structure it is bonded to. A popular method to improve adhesion is to expose the copper foil to a "black oxide" bath to roughen the copper. This insures that the epoxy prepreg will have good adhesion to the copper foil after lamination. However, we have established that the black oxide process, while not appearing to physically damage the capacitor dielectric, reduces the insulation resistance of the capacitor by an order of magnitude, presumably due to creation of a low resistance, surface film on the dielectric surface. If such process is required to improve adhesion, the capacitors should be protected from the black oxide bath. Alternatively, foils that do not need adhesion promotion can be used instead.

After lamination, photo resist is applied to the copper foil of the laminate structure and the foil is etched to create the capacitors electrodes and associated circuitry. This process may expose the capacitor dielectric to the etching solution and the photoresist stripper.

Thermodynamic analysis of the effects of etching solutions on the capacitor dielectric were undertaken to see what effect we might expect.[7] $FeCl_3$ /HCl and NH_4Cl/NH_4OH baths were chosen for the analysis. The analysis predicted the barium titanate and the glass composition were unstable in both baths, reacting to form $BaCl_2$, TiO_2 and chlorides of the glass components. A kinetic evaluation wherein the dielectric was soaked in the etching solutions for various periods of time and then analyzed for weight loss revealed that the HCl baths are much more aggressive. Within a similar timeframe, the HCl based bath dissolved 6-7 times more than the alkaline bath.

Table 3 - PWB Processes and Chemistries

Copper adhesion treatment	Hydrogen peroxide in dilute sulfuric and alkali based cleaners
Copper etching	Ferric chloride in hot hydrochloric acid
	Cupric chloride in hot hydrochloric acid
	Cupric chloride in hot ammonium hydroxide
Photoresist stripper	Hot potassium hydroxide
Microetch/MEC etch	Dilute hydrochloric or sulfuric acids
Plating	Sulfuric pre-treat plus nickel sulfates and chlorides, etc.

PWB inner layer panels were then made using ferric chloride in 2.4 N HCl at 70°C as the PWB etching solution. The resulting capacitors in the PWB exhibited very low insulation resistance and a high level shorting. A cross-section of a double layer capacitor at this inner layer stage is shown in Figure 4. The micrograph shows where the etching removed the copper foil from the dielectric. The dielectric was exposed to the etching solution for a short period of time after the copper foil was etched away. As indicated by the arrow, preferential dissolution of the glass binder occurred leaving behind the barium titanate grains. This result was consistent with our kinetic studies.

Making inner layers using an ammonium hydroxide based etchant, resulted in less visible damage to the dielectric consistent with the kinetic study. The electrical properties were also acceptable. A similar cross-section to Figure 4 but after the dielectric was exposed to the alkaline etch bath is shown in Figure 5. The surface of the dielectric has not lost any of its mechanical integrity. The porosity in the dielectric was evident prior to etching and is not an effect of the etching bath.

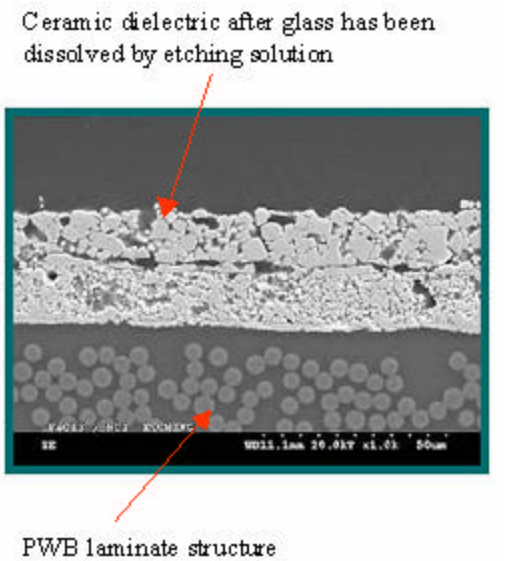


Figure 4 - Effects on Capacitor Dielectric of Ferric Chloride in 2.4N HCl

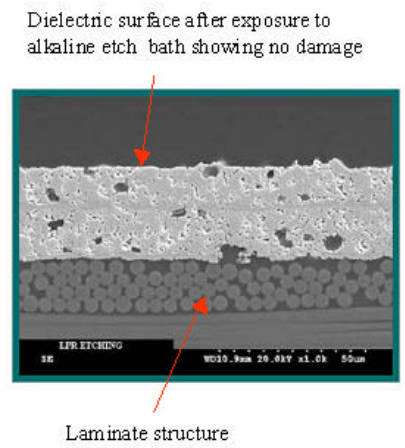


Figure 5 - The Effect of Cupric Chloride In 20% Ammonium Hydroxide on the Dielectric Structure

Subsequent work has focused on the other various process chemistries used in the making of printed wiring boards and their effects on this first generation ceramic dielectric composition. It has been ascertained that many of the standard process chemistries have, at least, a minor deleterious effect on insulation resistance of the dielectric and the effects can be accumulative.

Summary

The advantages of embedded capacitors make it a very attractive technology. However, the greatest challenges to adoption lie with the designer and the PWB fabricator. CAD tools are not available to handle embedding ceramic capacitors and all designs must be made manually. Embedding these ceramic capacitors with high yield requires the use of feature sizes that take into account the tolerances of the thick-film process. Designs that minimize the exposure to the aggressive chemicals used in the PWB process have also been shown to be important. If chemical exposure to the dielectric is necessary, avoidance of hydrochloric acid based solutions is recommended. The more benign chemicals, such as alkali based solutions have been proven to provide an acceptable approach.

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