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Designers Summit 05

FVSS (Free Via Stacked up Structure)

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Abstract
The miniaturization of mobile electronic devices continues, market trends toward lighter and thinner printed circuit boards (PWB) have been accelerating. At the same time, the demand for increased functionality of mobile devices has required the PWB to realize higher density patterning to accommodate more and narrower pitch CSPs on a smaller and thinner PWB. In order to meet these market demands, IBIDEN has developed a stacked-via structure PWB called "FVSS" (Free Via Stacked-up Structure). This structure is achieved by filled-via technology, a core technology that fills a laser-drilled hole with copper plating. The mass production of this technology started in 1st quarter of 2004, and it has proved that, compared to a conventional type of PWB, design flexibility and total board thickness can be significantly improved. More details regarding the design flexibility, electric characteristics, and reliability will follow.

Introduction
A brief overview: FVSS is defined as a PWB with a stacked-up via structure manufactured using our own filled-via technology. Figure 1 shows board structures of the conventional offset type and Free Via Stacked structures 1 and 3. On conventional boards, it is observed that wiring space is restricted by the presence of inner via holes and through holes, and also wiring flexibility is limited due to the via's offset structure. As for the Type 1, the core layers include mechanical drilling to form inner via holes just as conventional type, but build-up layers are constructed with stacked-up structure by filled-via technology. When the stacked-up structure is applied to all layers, it becomes Type 3. (Standard dielectric material for stacked-up layers is glass-epoxy, thickness 60um.) With this full-stacked type, there is no space devoted for inner via holes and through holes, thus no constraint on via placement. These features realize highly improved wiring density.

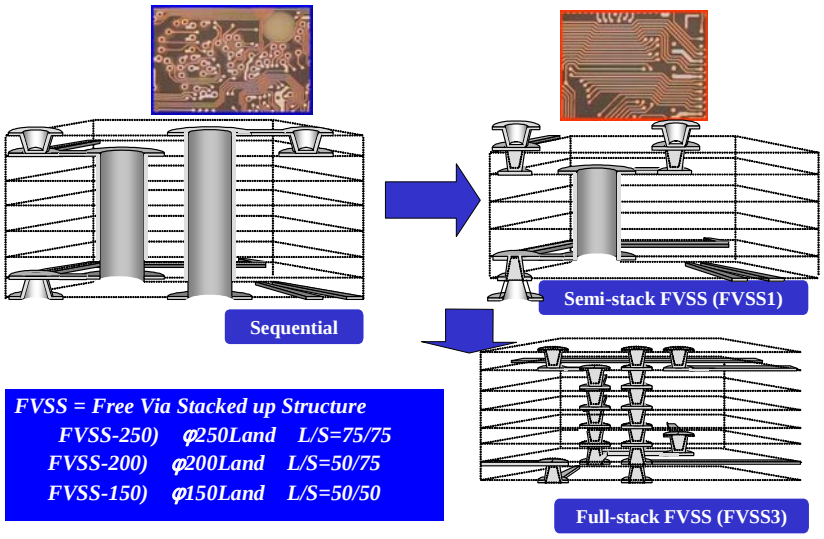


Figure 1 - Layer Structure from Sequential to Stacked-up

As described later on, the manufacturing process takes the form of a sequential lamination method. Forming vias and patterns in alignment with the inner layer completes a build-up layer. With this method, it is possible to assure alignment accuracy, and consequently it is possible to reduce via diameter.

Free Via Stacked Structure 1 with 250um (10mil) via land diameter is called "FVSS1-250", and 200um (8mil) and 150um (6mil) are "FVSS1-200" and "FVSS1-150" respectively. (* In the space after "FVSS", either number "1" or "3" will appears to specify construction type.) The technology's wiring density is achieved not only by layer construction but also by decreasing via land diameter.

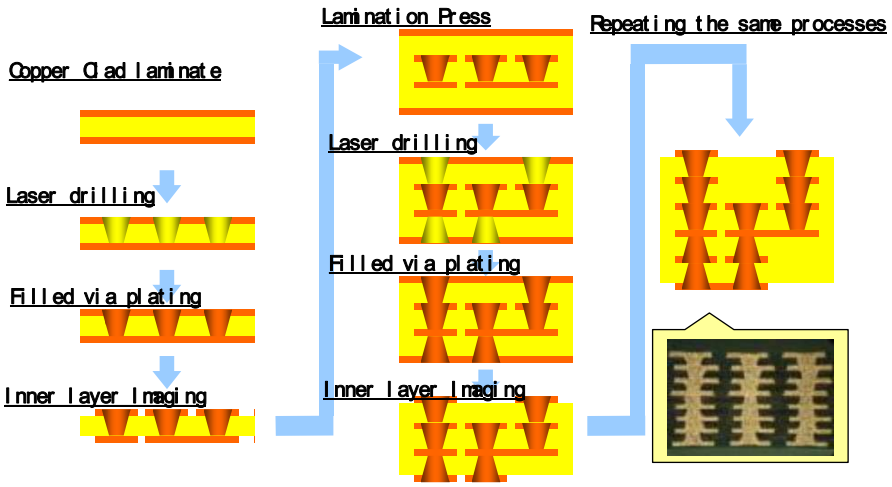


Figure 2 – FVSS (Free Via Stack up Structure) – Manufacturing Process Flow

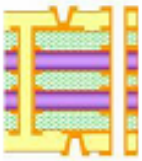
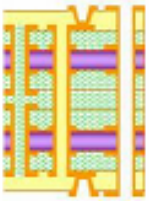
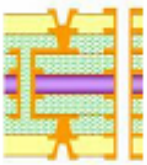
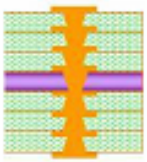
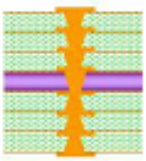
Figure 2 illustrates the basic manufacturing process flow. First, glass-epoxy core material is prepared and non-through holes are formed by laser to the Cu foil on the backside. The holes are filled by copper plating, which is proved to have high reliability and low electrical resistance, and patterning and lamination continued.

By repeating processes after lamination, a full-stack Type 3 structure with high density wiring, excellent electric characteristics and a highly reliable connection can be manufactured.

Analysis of Characteristics

High Density Wiring

As mentioned, high density wiring is one of the greatest benefits of this technology. Figure 3 shows the result of auto wiring rate by design rules. The wiring rate here is the rate which auto-wiring by CAD is successful when a mobile phone's base band area with the conventional components is reduced to the 2/3 the normal size.

	1-6-1	1-4-4-1	FVSS1-250	FVSS3-250	FVSS3-150
Layer structure					
Line/Space	75/75	75/75	75/75	75/75	50/50
IVH Land diameter	500	500	500	-	-
LVH Land diameter	250	250	250	250	150
Auto design route level	66.6%	68.7%	77.3%	88.4%	100%

Unit: micron meter

Figure 3 – PWB Design Comparison

With conventional 1-6-1 offset type, the wiring rate is 66%, 68% with 1-4-4-1, but it is increased to 77% with FVSS1-250, 88% with FVSS3-250, and 100% auto wiring is achieved with FVSS3-150.

Figure 4 describes the case of layer count reduction from an 8 layer PWB using other via stacking technology (design rules are land size of 300um and line/space 100/100um) to a 6 layer PWB using FVSS3-150. This proves that the technology is capable of meeting cost reduction requirements by reducing number of layers.

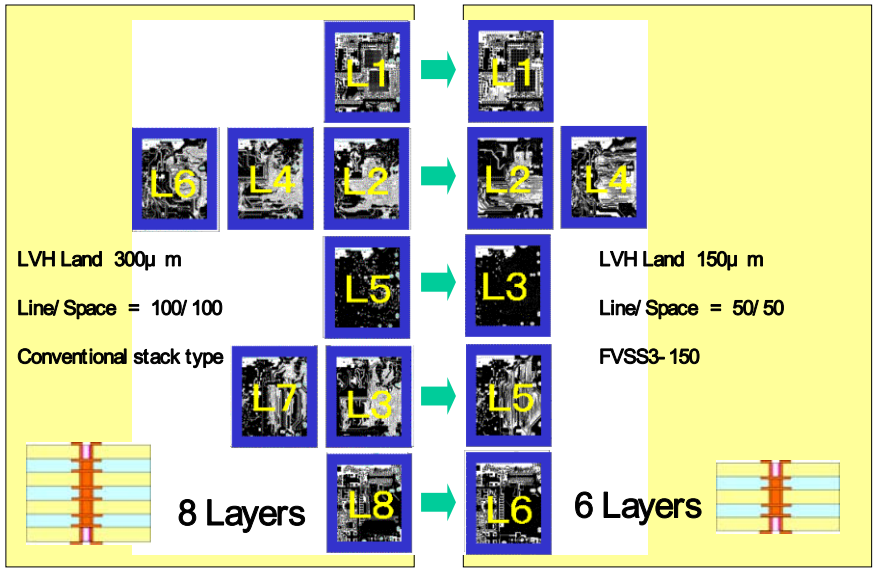


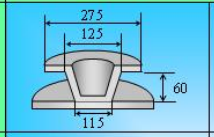
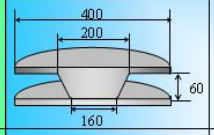
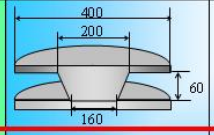
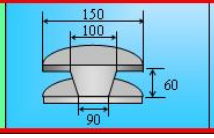
Figure 4 – Reducing Layers

Electrical Characteristics

Table 1 shows resistance value per via by via type. Compared to conformal via technologies, filled via has the same volume resistance (ρ;Ω m) since both are plated with copper, but the resistance value is smaller because cross-section area is larger due to being fully filled with copper.

R=ρ*l/S
[l (length);m S (cross-section area);m2]

Table 1 - Resistance Value by Via Type

	Structure		Resistance/hole
Conventional LVH <Reference>		TH Continuity:Cu plating Volume resistance : $1.724\times10^{-6}\Omega\cdot cm$	0.27(mΩ)
Conductive paste A		TH Continuity :Cu past Volume resistance : $2\times10^{-4}\Omega\cdot cm$	4.72 (mΩ)
Conductive paste B		TH Continuity :Ag past Volume resistance : $3\times10^{-4}\Omega\cdot cm$	7.08 (mΩ)
Copper Filling		TH Continuity:Cu plating Volume resistance : $1.724\times10^{-6}\Omega\cdot cm$	0.16 (mΩ)

There are Cu paste and Ag paste methods that can be used to fill vias for the same stacked-up structure PWB as FVSS. Compared to these 2 options, the new technology has lower volume resistance and a lower resistance value per via because the copper within a via is more pure conductor. As a result, allowable current per via becomes larger.

When it is necessary to run high current and supply it by several vias, via count is reduced by using this technology and here merits arise in terms of both cost and productivity.

The next focus is on S-parameters. Figure 5 illustrates a model of FVSS and of Ag paste and Cu paste vias next to a graph of S-parameter simulation. Vertical axis of the graph is S21-parameter and horizontal axis is frequency. As a whole FVSS shows highest and more stable S21-parameter value followed by Cu paste and Ag paste.

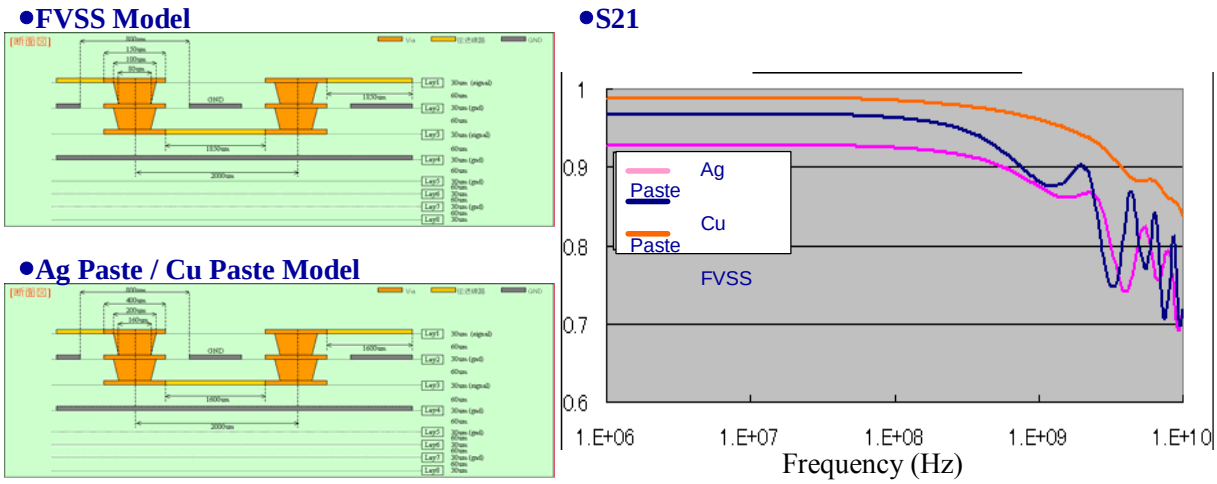


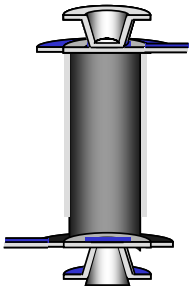
Figure 5 – S-Parameter Simulation

These excellent results achieved are due to a lower resistance value per via than other technologies as stated before. In addition, at higher frequencies wave disorder is observed on Ag and Cu paste, but that is minor for Free Via technology. This is attributed to a smaller annular ring than that of standard design rules for paste vias. This advantage is achieved by higher accuracy alignment for Free Via technology. The annular ring is a so-called stub that is unnecessary in electric transmission, so a smaller annular ring shows less wave disorder.

Thermal Stress

For miniaturization, it is desirable to remove mechanically drilled holes because they reduce wiring area. Laser via & IVH sequential structure will change to stacked-up via structure as Table 2.

Table 2 - Comparison of the interconnect method

Technology	Sequential		FVSS
Hole Type	Via on IVH		Stacked Via
Method	Laser & Mechanical Drill		Laser Drill
Nominal Diameter	Via :100um, IVH : 250um		100um
Cross Section Drawing		⇒	

In a Free Via Stacked Structure design, it is possible to reduce the hole-to-hole pitch while maintaining the same function as a mechanical drilled hole by via stacking on all layers.

When the size of a hole is reduced, there is concern that thermal stress may increase per each hole. Therefore we compare the thermal stress for both types of holes using simulation software. For this study, **ANSYS Mechanical** is used as simulator and simulation parameter is as follows:

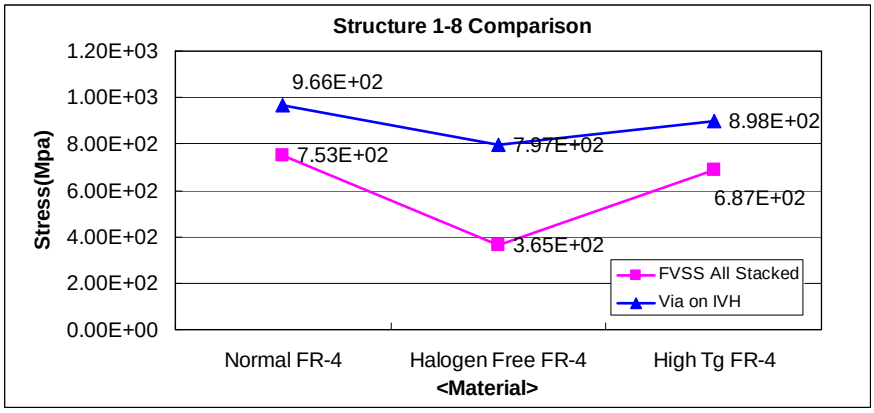
- This simulation is performed for three kinds of CCL (Copper Clad Laminate)
- The test condition of a -55 to 125°C thermal cycle is used.

Table 3 - Simulation Parameter for Thermal Stress

Material		Parameter				
		CTE (ppm)			Young's Modulus Gpa(α1)	Poisson's Ratio
		X	Y	Z		
Copper		16.6	16.6	16.6	123	0.3
Solder Mask		57	57	57	3.5	0.42
IVH Filled		42	42	42	49	0.41
CCL	Normal FR-4	12	14	65	22	0.2
	Halogen Free FR-4	12	14	40	23	0.2
	High Tg FR-4	14.5	14.5	50	24	0.17

Table 4 shows the results of thermal stress simulation by CCL material and design.

Table 4 Comparison with Thermal Stress by material and design



The value of thermal stress for the new structure is lower than that of a via on an IVH structure in all three materials. There is a 22 - 54% reduction in thermal stress by changing layer structure from vias on IVH to a Type 3 structure. Figure 6 and 7 show the thermal stress distribution for each design.

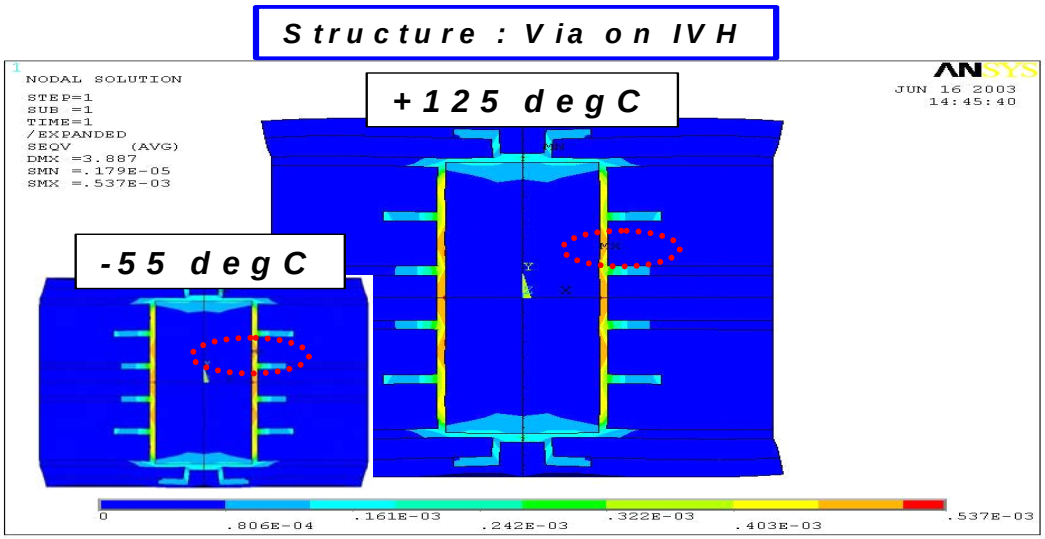


Figure 6 - Drawing of the equivalent distribution for Thermal Stress (Via on IVH Structure)

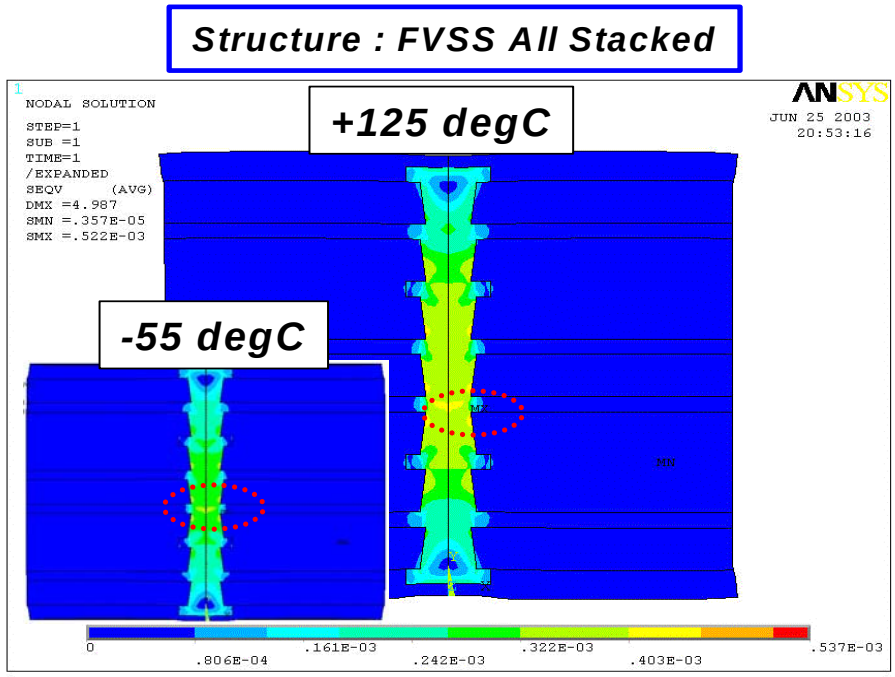


Figure 7 - Drawing of the Equivalent Distribution for Thermal Stress (Via on IVH Structure)

As these simulation results indicate, the new structure is superior to Via on IVH structure for any material type. Therefore it can be concluded that this technology possesses an effective structure to curb some kinds of failures in areas where vias are concentrated because of its lower stress.

Reliability - Environmental Test

A test board was designed for reliability test of continuity and insulation resistance. The board has daisy chain and via/via insulation patterns for both evaluations.

Figure 8 and Figure 9 show the cross-sectional view of the evaluation patterns and Table 5 shows the design rules and specifications. The table contents show the via/land diameter, via/via pitch, dielectric thickness of each material and layer counts.

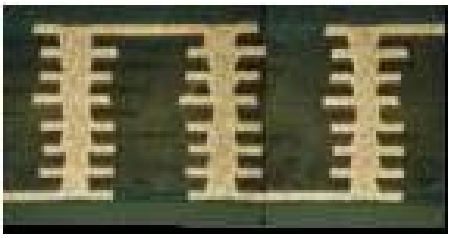


Figure 8 - Daisy Chain Pattern

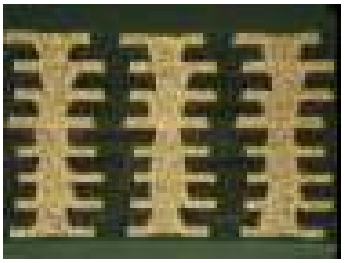


Figure 9 - Insulation Pattern

Table 5 - Specification of Evaluation Board

Material	Halogen Free FR-4	Normal FR-4	Low-CTE Halogen Free
Via Hole [um]	80	80	80
Via Land [um]	250	250	250
Via/Via Pitch [mm]	0.3, 0.35, 0.4	0.3, 0.35, 0.4	0.3, 0.35, 0.4
Dielectric Thickness [um]	60	60	60
Layer Counts	8	8	8

AATC Evaluation

To evaluate the reliability of via continuity, an AATC (**A**ir to **A**ir **T**hermal **C**ycle) test is conducted. The test condition used was the IPC-TM-650 standard. Figure 10 shows the summary of evaluation results.

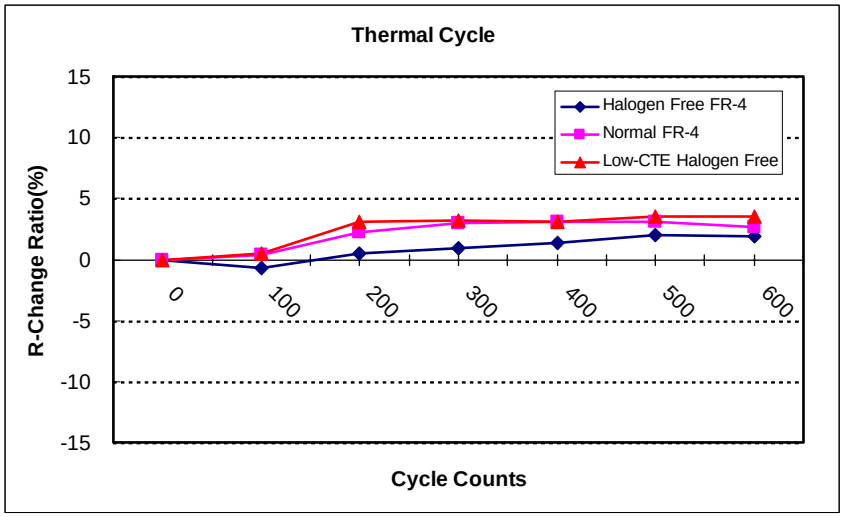


Figure 10 - Relation between cycles of AATC and Resistance change of via connection

After 500 cycles, the resistance change is less than 10% from initial value on all samples. Also no failure is found in the via chains from any samples. It is verified that there is no problem for interconnect reliability in AATC.

HHBT Evaluation (Insulation)

<**H**igh **H**umidity **B**ias **T**est>

To achieve the high-density design with smaller pitch CSP (0.4mm, 0.3mm…), via/via insulation becomes an important factor.

To evaluate the small pitch insulation, 0.3, 0.35 and 0.4mm via/via pitch patterns were placed on an evaluation board.

Test boards are held in the constant temperature and humidity chamber for 1000 hours with 24V bias. For the test the conditions in the IPC-TM-650 standard were followed.

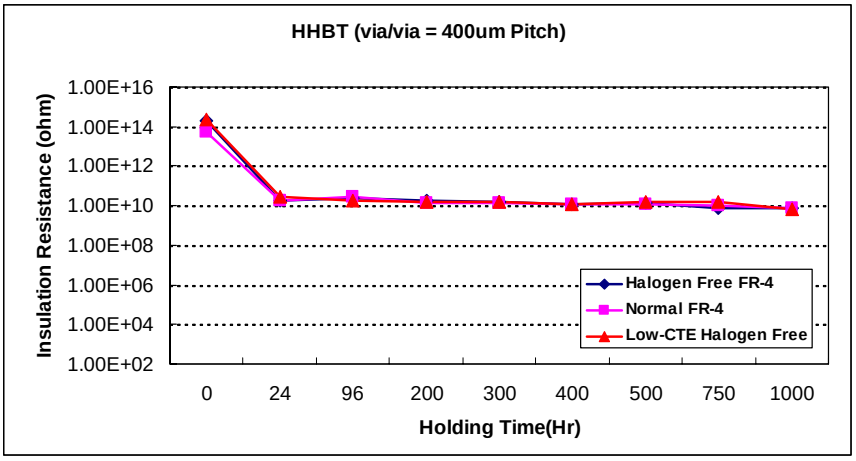


Figure 11 - Insulation Resistance (via/via 400um Pitch)

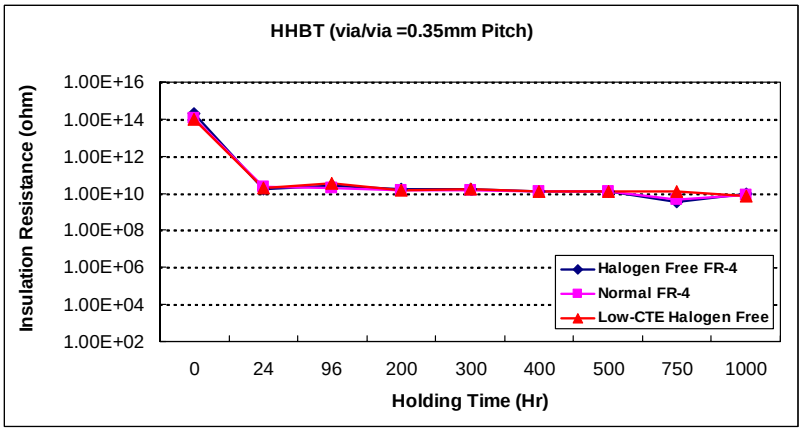


Figure 12 - Insulation Resistance (via/via 350um Pitch)

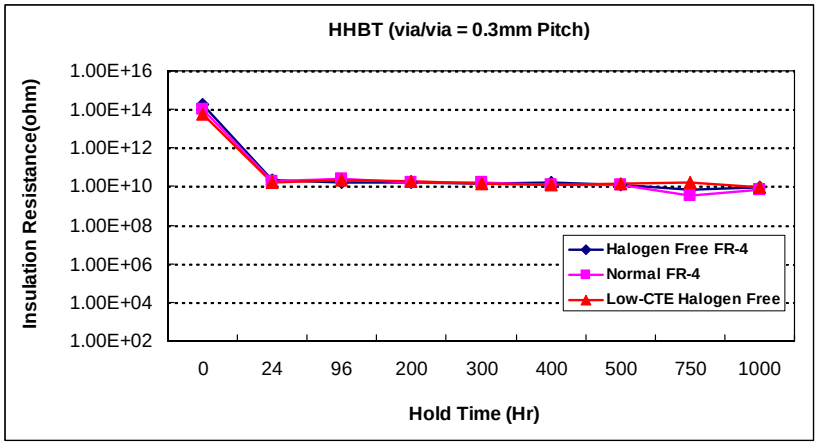


Figure 13 - Insulation Resistance (via/via 300um Pitch)

As shown in Figure 11, 12 and 13, insulation resistance is stable even after 1000 hours. There is no effect for insulation resistance down to at least 0.3mm via pitch. From this result insulation resistance is concluded to be sufficient.

Conclusion

Through this study and evaluation, our free via stacked technology, which applies filled-via technology, has been shown to display high reliability and electrical performance level.

Currently this technology has been applied to high density and small pitch design for mobile electronic devices such as those represented by mobile phones.

References

1. Clyde F. Coombs, Jr. “PRINTED CIRCUITS HANDBOOK” - Fourth Edition – pp.35.35
2. IPC-TM-650 Test Methods Manual 2.6.6 Temperature Cycling, Printed Wiring Board (AATC)

FVSS
(Free Via Stacked up Structure)

Characteristic of FVSS for the Solution of Design Subject

February 23rd ,2005

Michimasa Takahashi

IBIDEN CO.,LTD

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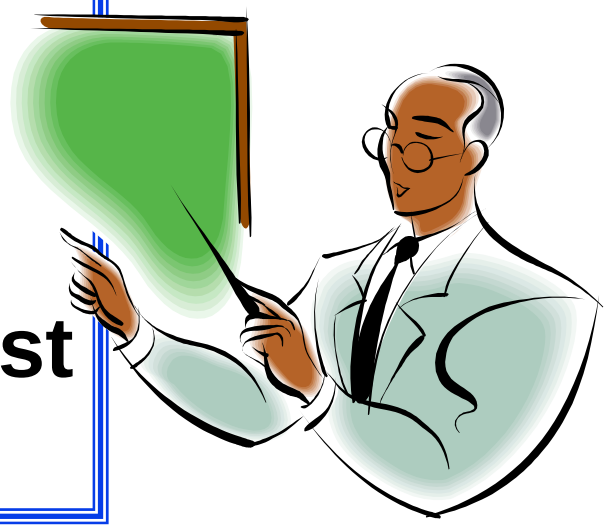
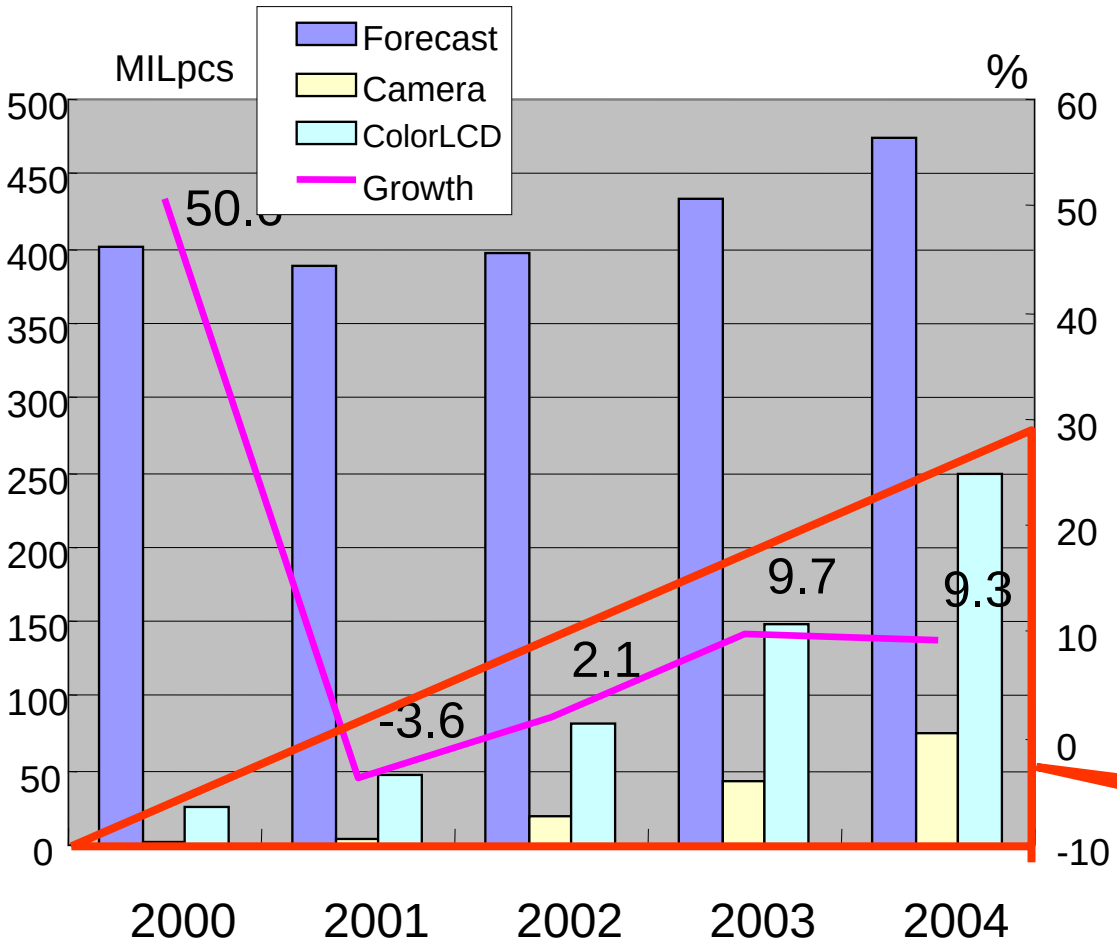


Introduction

<Mobile Phone Market>



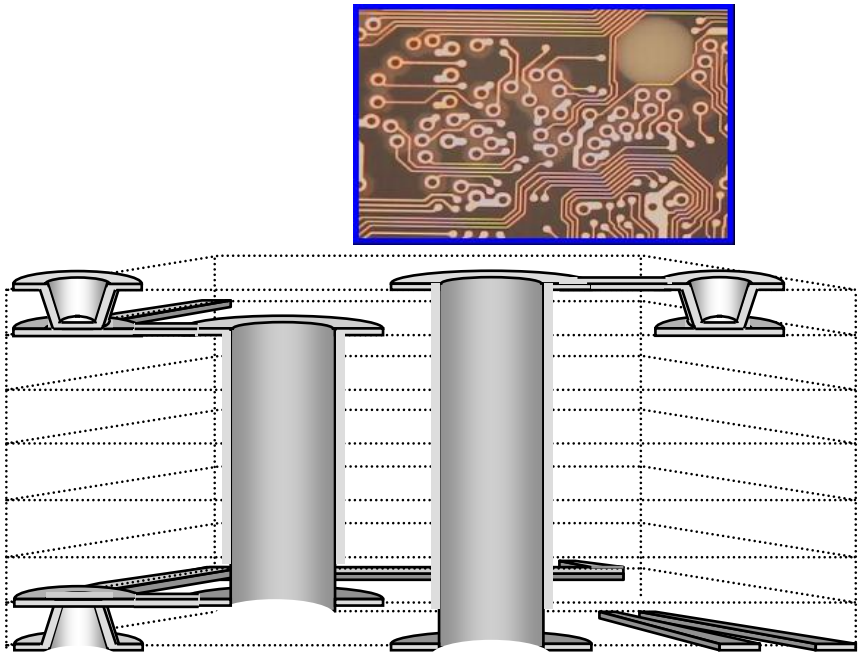
- Growth is expected up to 10%
- Phone with Color LCD will be popular in global market.
- Camera device will follow combined with Color LCD
- In Japan more than 81% of phones sold has Camera

Potential Market for Smart Phone

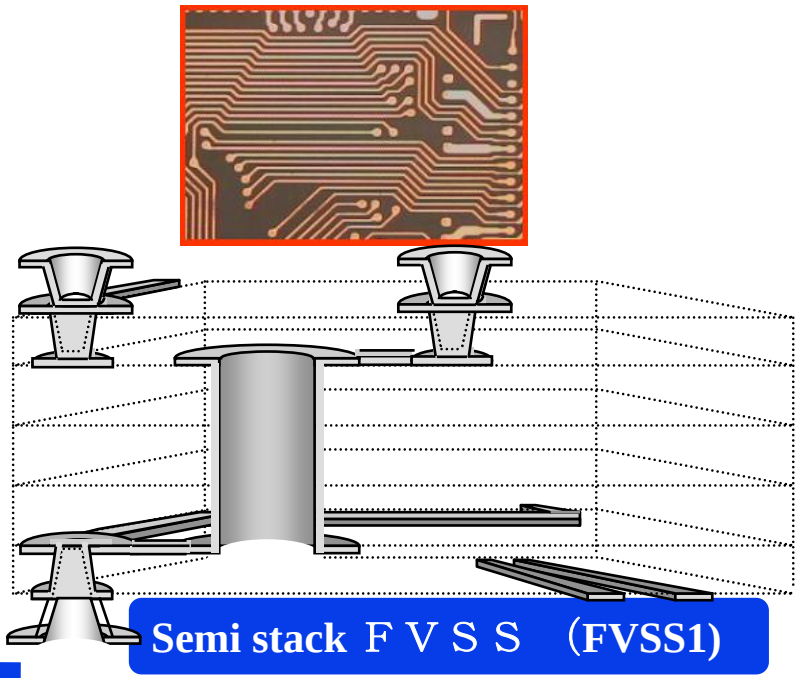
Introduction

<FVSS's overview>

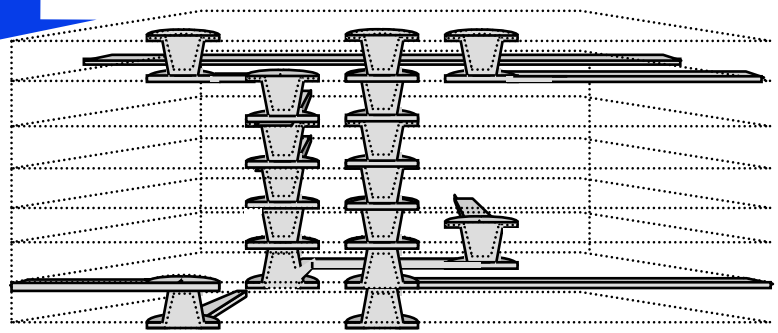
Layer Structure from sequential to stacked up



Sequential



Semi stack F V S S (FVSS1)



Full stack FVSS (FVSS3)

FVSS = Free Via Stacked up Structure

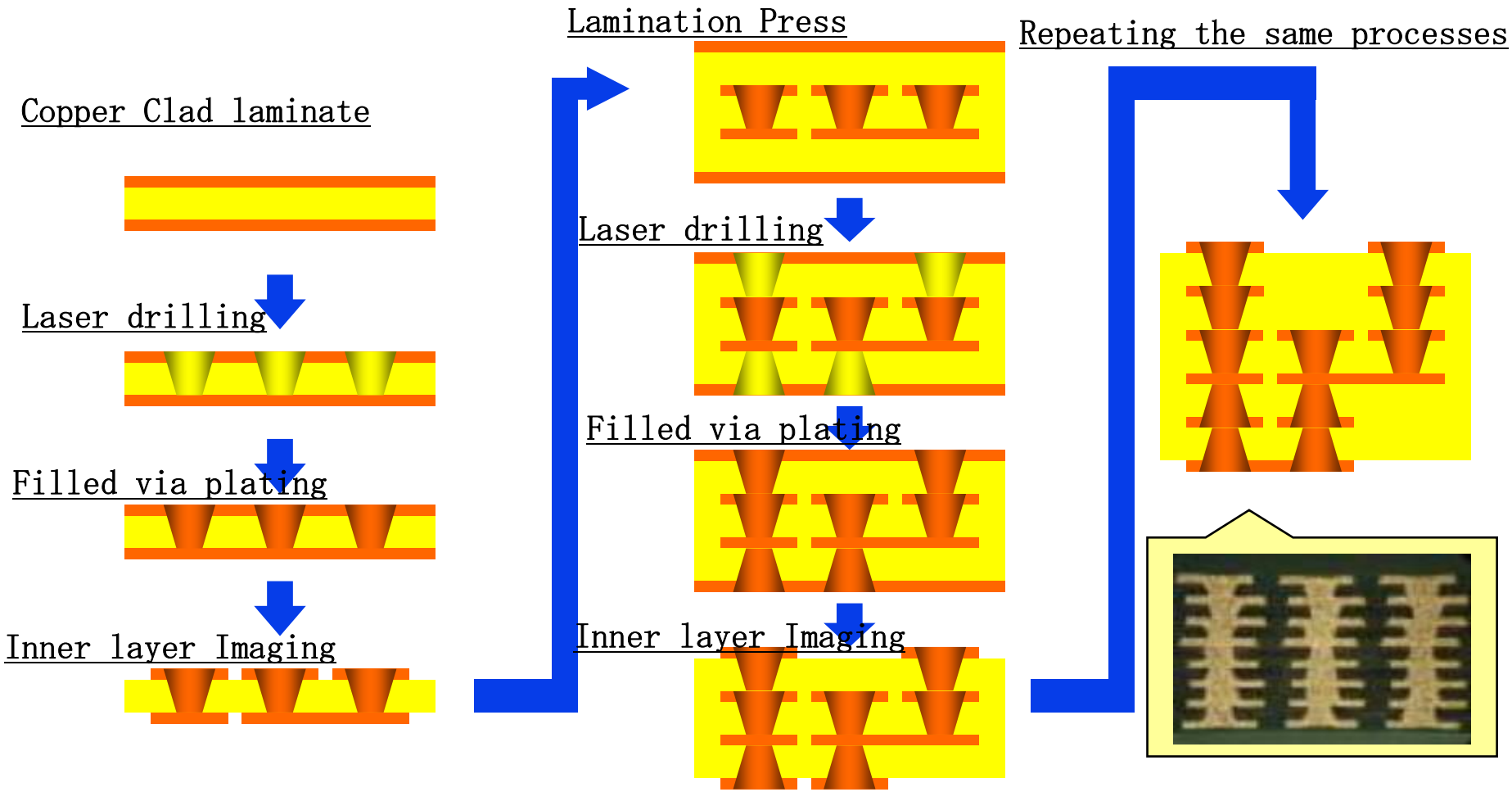
FVSS-250) φ250Land L/S=75/75

FVSS-200) φ200Land L/S=50/75

FVSS-150) φ150Land L/S=50/50

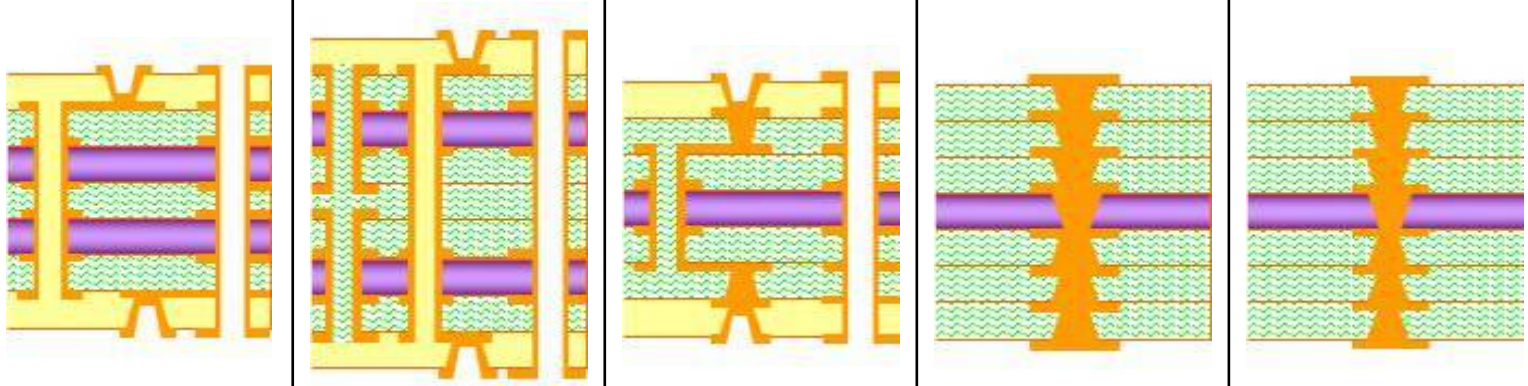
Introduction

<Manufacturing Process Flow>



Analysis of characteristics <High density wiring >

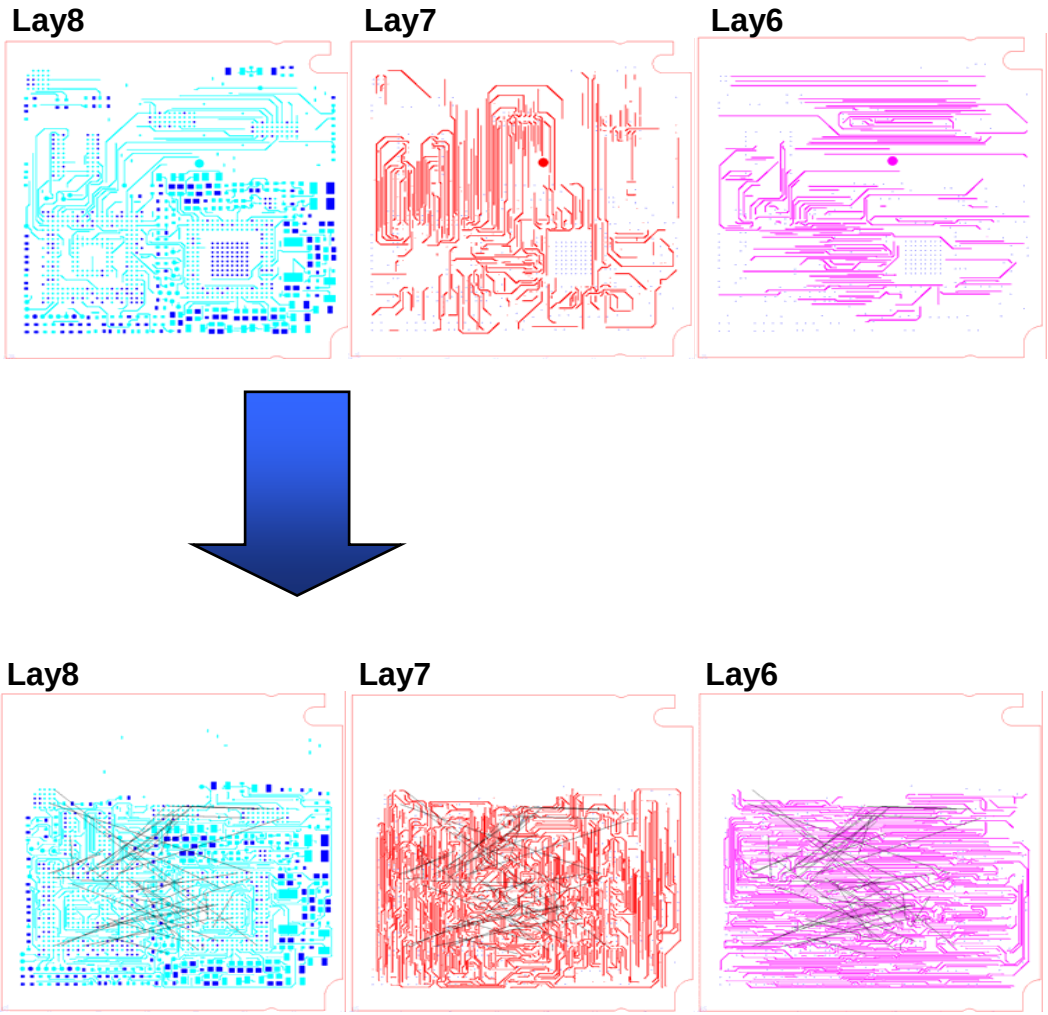
PWB Design (Auto design route level) Comparison

	1-6-1	1-4-4-1	FVSS1-250	FVSS3-250	FVSS3-150
Layer structure					
Line/Space	75/75	75/75	75/75	75/75	50/50
IVH Land diameter	500	500	500	—	—
LVH Land diameter	250	250	250	250	150
Auto design route level	66.6%	68.7%	77.3%	88.4%	100%

Unit: micron meter

Analysis of characteristics <*High density wiring*>

Auto design route level

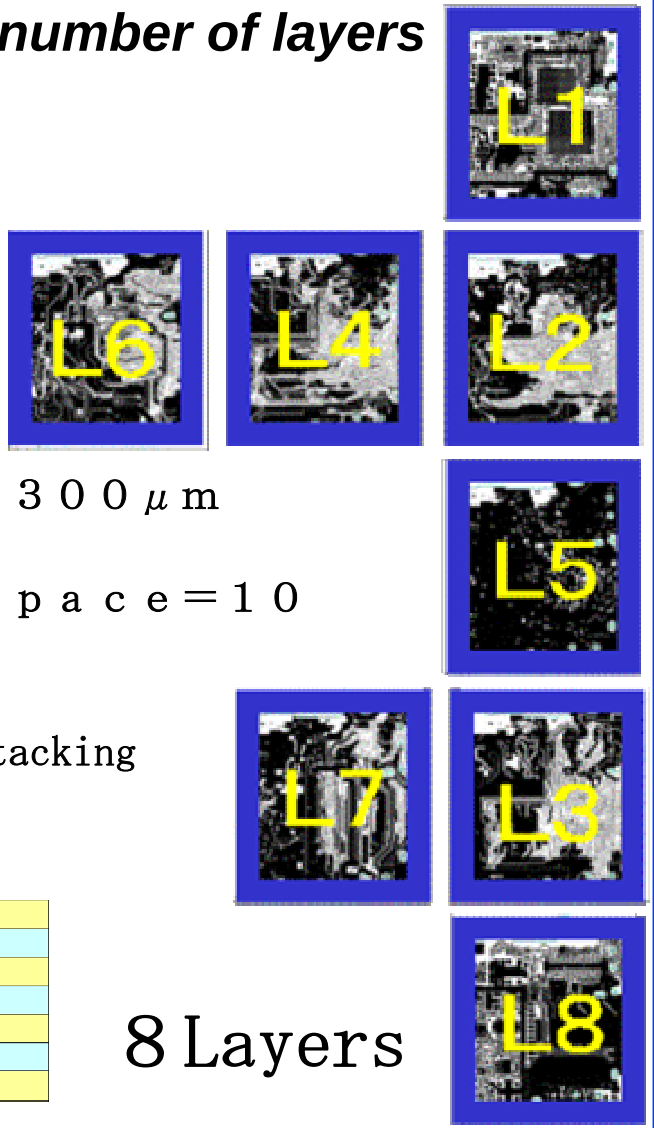


•The auto design level here is the rate which auto-wiring by CAD is succeeded on 2/3 size of mobile phone's base band with the conventional components on.

Analysis of characteristics

<High wiring density>

Reducing number of layers



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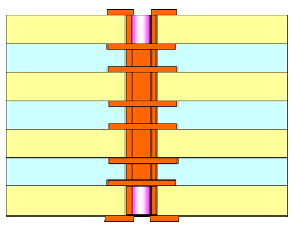
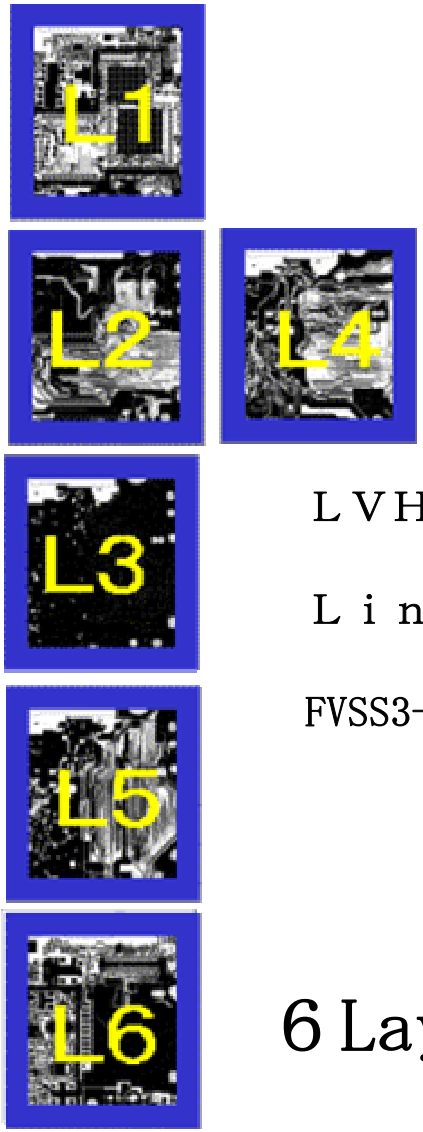
Other via stacking technology



8 Layers



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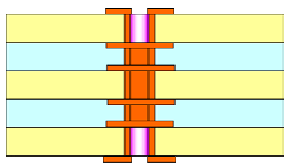
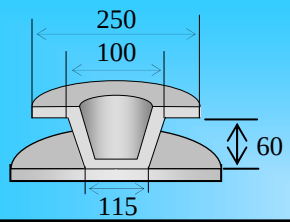
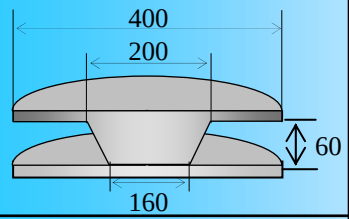
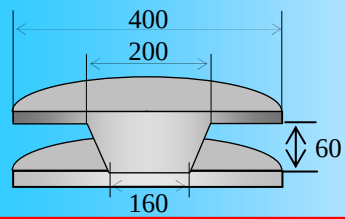
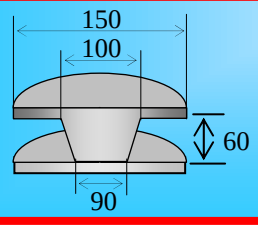
FVSS3-150

6 Layers



Analysis of characteristics <Electric characteristics>

Comparison of Type of Via Hole

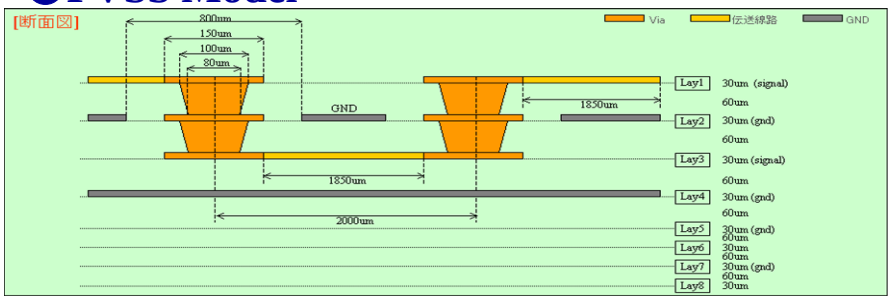
	Structure		Resistance/hole	Allowable Current	Via quantity/1(A)
Conventional LVH		TH Continuity:Cu plating Volume resistance : $1.724\times10^{-6}\Omega\cdot cm$	0.27(mΩ)	0.105(A)	10
Conductive paste A		TH Continuity :Cu past Volume resistance : $2\times10^{-4}\Omega\cdot cm$	4.72 (mΩ)	0.031(A)	32
Conductive paste B		TH Continuity :Ag past Volume resistance : $3\times10^{-4}\Omega\cdot cm$	7.08 (mΩ)	0.037(A)	27
Copper Plating		TH Continuity:Cu plating Volume resistance : $1.724\times10^{-6}\Omega\cdot cm$	0.16 (mΩ)	0.176(A)	6

When it is necessary to run high current and supply it by several vias, via count is reduced by using FVSS and here merits arise in terms of both cost and productivity .

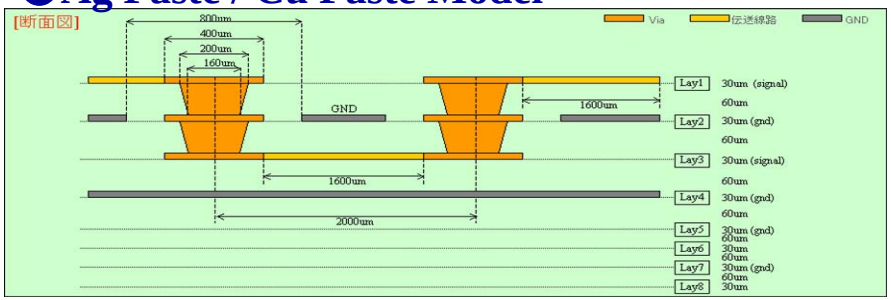
Analysis of characteristics <*Electric characteristics*>

S21-Parameter Simulation

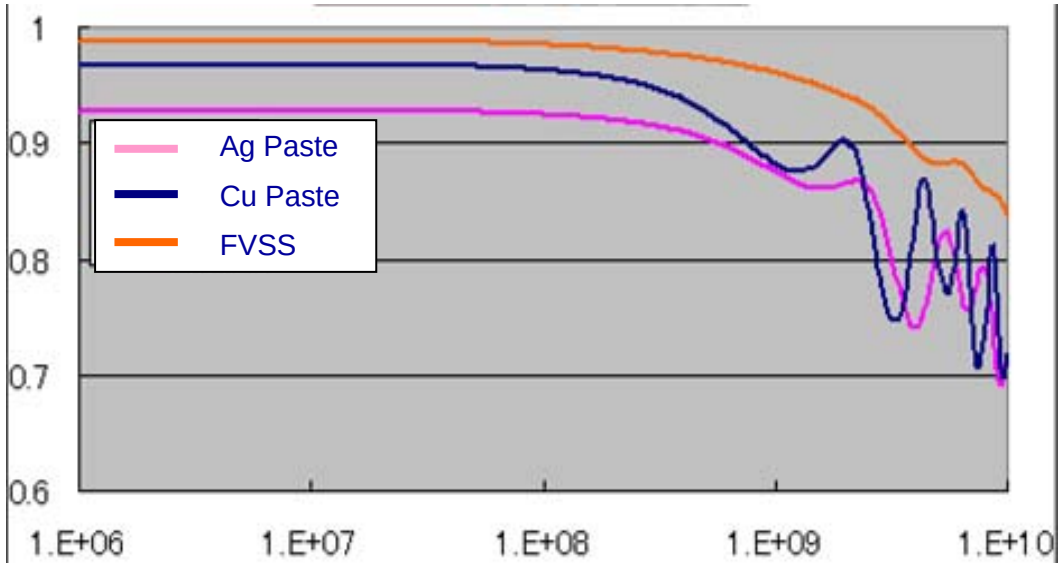
●FVSS Model



●Ag Paste / Cu Paste Model



●S21



As a whole FVSS shows highest and more stable S21-parameter value followed by Cu paste and Ag paste.

Analysis of characteristics <Thermal stress>

To analyze thermal stress for interconnection, we simulated thermal stress with using ANSYS Mechanical as a simulator tool.

***Condition of Simulating**

1. Thermal Stress Condition

➔ -65 to 125C-deg Thermal Cycle (IPC-TM650 Standard)

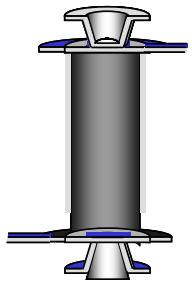
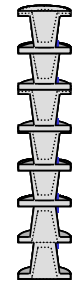
2. Material

Normal FR-4 (Halogenated)
Halogen Free FR-4
High Tg FR-4 (Halogenated)

3. Layer Structure

8Layer full stacked up by FVSS
8Layer Via on Inter Varied (Mechanical Drill) Hole

Layer Structure and Spec Draw in this Simulating

Technology	Sequential		FVSS
Hole Type	Via on IVH		Stacked Via
Method	Laser & Mechanical Drill		Laser Drill
Nominal Diameter	Via :100um, IVH : 250um		100um
Cross Section Drawing		⇒	

Material Parameter for Simulation

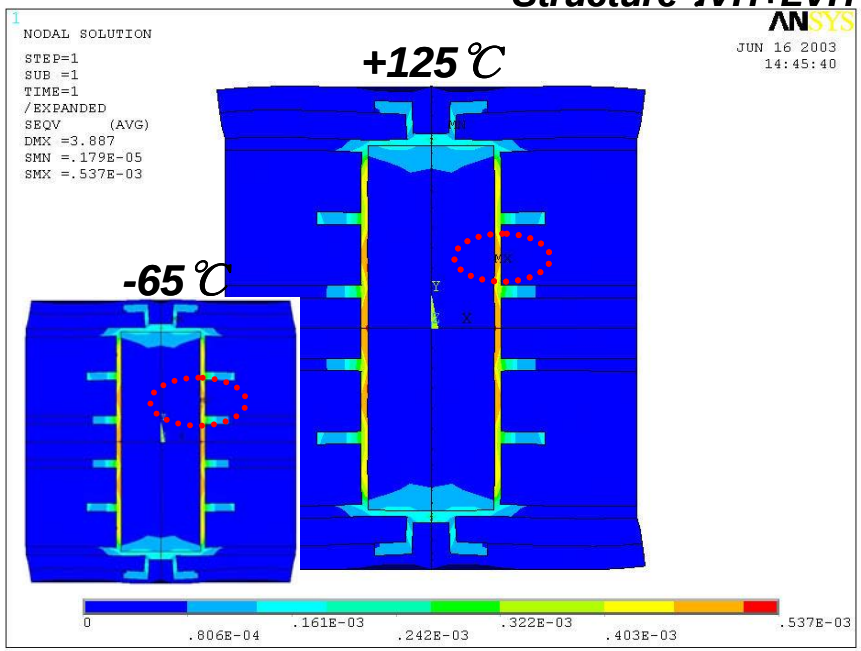
Material		Parameter				
		CTE (ppm)			Young's Modulus Gpa(α1)	Poisson's Ratio
		X	Y	Z		
Copper		16.6	16.6	16.6	123	0.3
Solder Mask		57	57	57	3.5	0.42
IVH Filled Resin		42	42	42	49	0.41
CCL	Normal FR-4	12	14	65	22	0.2
	Halogen Free FR-4	12	14	40	23	0.2
	High Tg FR-4	14.5	14.5	50	24	0.17

Analysis of characteristics

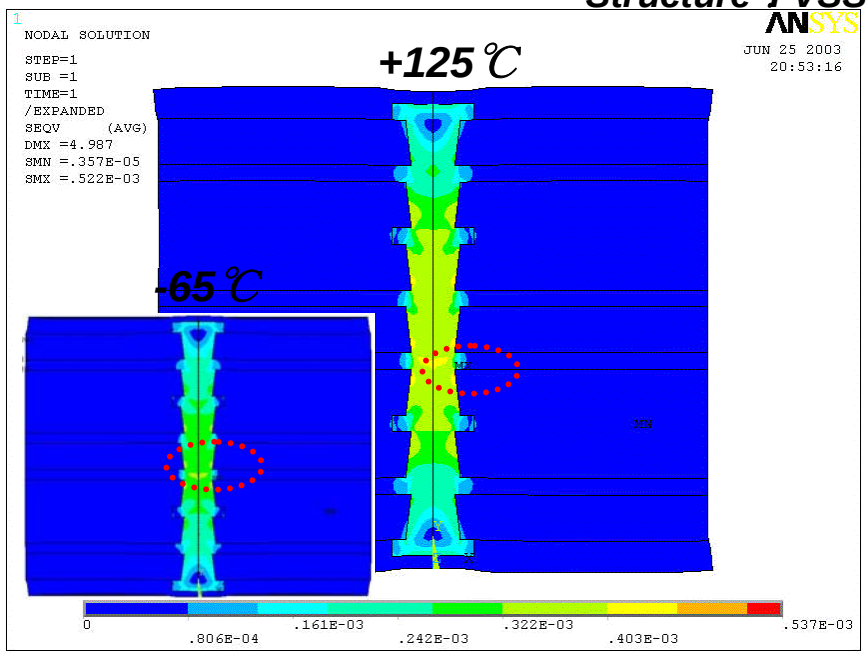
<Thermal stress>

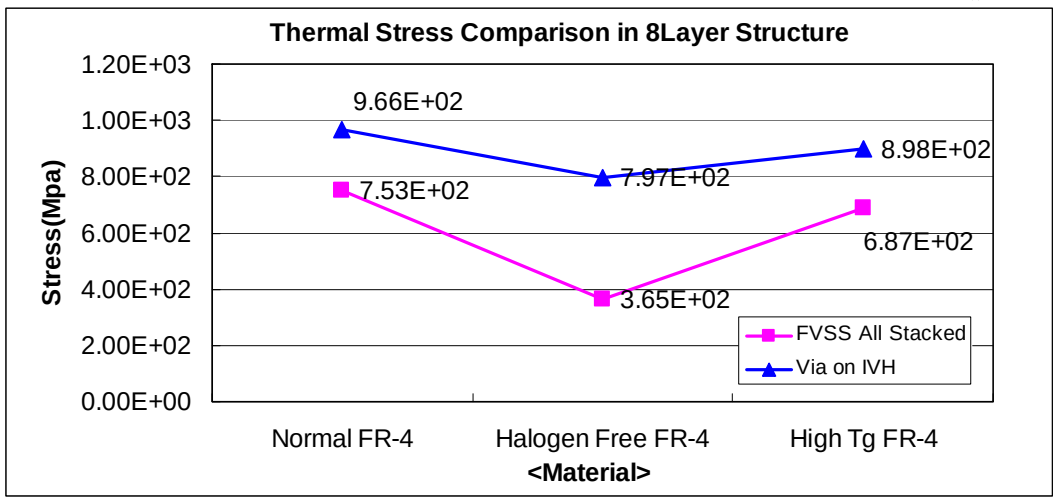
Thermal Stress Comparison by Layer Structure and Material

Structure IVH+LVH



Structure FVSS





Point of the Maximum Stress

54% of thermal stress can be prevented by FVSS structure compare with other layer construction such as IVH+HDI.

This means that, any defective problems around HDI can be solved using FVSS.