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Optimised Vertical Process for Microvia Filling and Through Hole Metallization Under Production-like Conditions

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Abstract
This article summarises how a copper metallization process for simultaneous via filling and through hole plating was developed on a laboratory scale and the challenges encountered by scale-up to larger industrial like electrolyte volumes. Uniform filling and through hole plating on large PWBs was successfully achieved by combining various technologies for achieving uniform current distribution, hence good via filling efficiency and PTH metallization, independent of sizes and location on the board surface. Both panel and patterned boards were treated.

Introduction
Increasing performances and miniaturisation of high density interconnect (HDI) substrates for portable products demand innovative solutions to each step involved in the board manufacturing. The conventional copper plating concepts for electronic interconnects (IC) cannot without modification, ensure high filling efficiency of microvias and sufficient through holes metallization.

Monitoring and replenishment of "super-filling" processes containing carriers, activators and levellers is made difficult by the increased bath complexity and requires advanced control systems. In addition an optimised chemistry tailored toward the different feature sizes also requires well defined and stable hydrodynamic conditions in order to provide acceptable metallization for the smaller interconnect features.

This paper describes how the development and optimisation of a first generation vertical copper process for both microvia filling and through hole metallization of HDI boards, was successfully scaled up from laboratory level to production conditions. Through the combination of

- select carriers and activators,
- design of well-defined bath hydrodynamics
- and appropriate current adjustment,

The filling efficiency was demonstrated to be independent of size and location in large boards (450 x 550 mm). Via fill was found to be high and throwing power for through hole plating higher than 85%. In addition, all boards processed under optimised conditions passed thermal cycling testing and additive maintenance was easily controlled by CVS.

Experimental
The metallization process was optimised during various DOEs in 5 litre plating cell experiments, using test vehicles with two rows, each counting 6 vias (diameter 80 µm, depth 60 µm) appropriately located on a 50 x 50 mm board. The via filling and PTH efficiency of the developed process, was also investigated using small-sized test vehicles, with different via aspect ratios, through holes and inner layer connections.

Finally processing conditions and filling efficiency as well as through hole plating on 58 dm^2 ML-boards (FR4, 140 Tg, 0.8 mm thick), was optimised in a 300 litre R&D-Pilot Line in Langenfeld, Germany.

The Via Fill Yield (VFY) and through hole metallization (PTH) were calculated as shown in Figure 1. The VFY takes into account not only the percentage of fill of the microvia, but also the thickness of the plated copper on top of the board and (in case of incomplete fill) the fill angle. The smaller this fill angle the easier it will be to fill the via with solder or resin without entrapment of air. Typically yield values over 5 represent good fill.

As for the through hole requirements, the objective was PTH > 80%. In addition the boards must pass both solder float (MIL P5510) and thermal cycle testing (10 x 255ºC ± 5º molten salt 30s // RT water 15s // dry 15 s), hence no corner cracking.

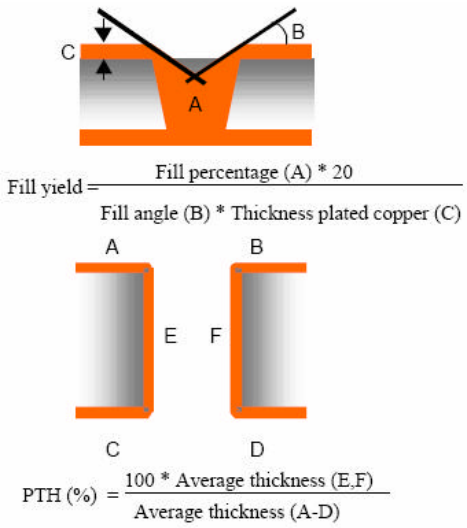

Figure 1 – Calculation of Via Fill Yield (VFY) and Plating Through Hole distribution (PTH)

The copper electrolyte utilised for this experiment does not contain any activator. However prior to metallization the test samples were pre-dipped at RT in a proprietary activator (500 ml/l TPB).

A detailed description of the overall process sequence is summarised in Figure 2. Type of agitation and the strength as well as anode:cathode ratios were also part of the process optimisation.

Process Sequence		
Cleaner/Etch	5min.	RT
Rinse		
Acid Dip	30sec.	RT
Rinse		
Pre-dip	5min.	25°C
Copper plate	90min.	25°C
Rinse		
Hot air dry		

Figure 2 – The Developed Process for Via Fill and Through Hole Metallization

Results

The optimum concentration of both sulphuric acid and copper was identified by defining VFY with concentrations of H_2SO_4 and Cu^{2+} from 50 – 200 g/l and 15 – 75 g/l. Added a proprietary inhibitor (TPA), very good filling efficiency at room temperature (RT) and direct current, was achieved in:

- 100 g/l H_2SO_4
- 50 g/l Cu^{2+}
- 70 mg/l Cl^-
- 1.0 ml/l CVF TPA (inhibitor)

Having optimised and investigated various possibilities for influencing the via fill efficiency and the through hole metallization, small test boards with various via aspect ratios were plated under DC conditions at 1.5 A/dm^2 . The via fill for both sizes was very good (Figure 3). The metallized boards passed both solder float and thermal cycles. Large boards metallized in a 300 litre R&D pilot-line with initial tank configuration revealed poor current distribution, hence bad via filling (Figure 4).

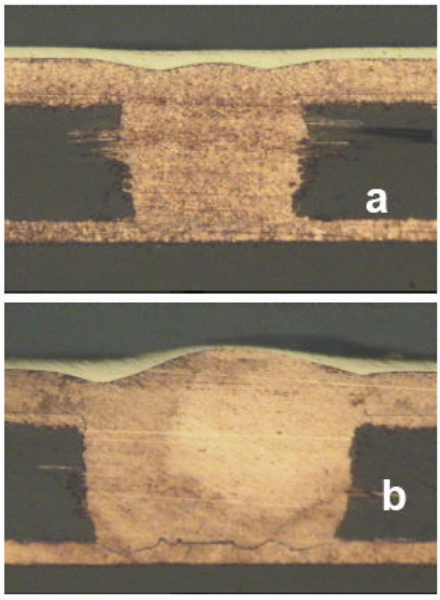

Figure 3 – Copper Metallization under Laboratory Conditions – Via size: (a) 95 µm Diameter, and (b) 140 µm Depth: 74 µm

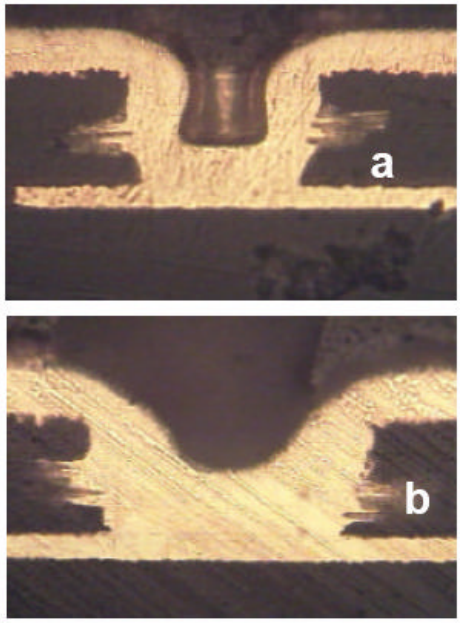

Figure 4 - Copper Metallization of Large Boards with Inappropriate Current Distribution
(Via size: (a) 95 µm diameter, and (b) 140 µm. Depth: 75 µm)

Prior to optimising the existing tank set-up, the thickness variation (current distribution) showed large variation over the entire board surface (Table 1).

After redesigning the anode cathode ratio by sizing Ti-basket according to the board size and introducing partial shielding together with a small cathodic copper current thief, (Figures 5 and 6) the thickness uniformity on the board surface was improved significantly (Table 1).

Table 1 - Average Copper Thickness on the Board Surface (n > 50) Prior to and after Optimising Tank Configuration

	Average	St. Dev.	Max.	Min.	Tank Set-up
Dummy 1	46.0	4.9	64	41	Initial
Dummy 2	42.6	1.7	46	40	1st adjustment
Dummy 3	41.2	1.5	44	38	Final adjustment

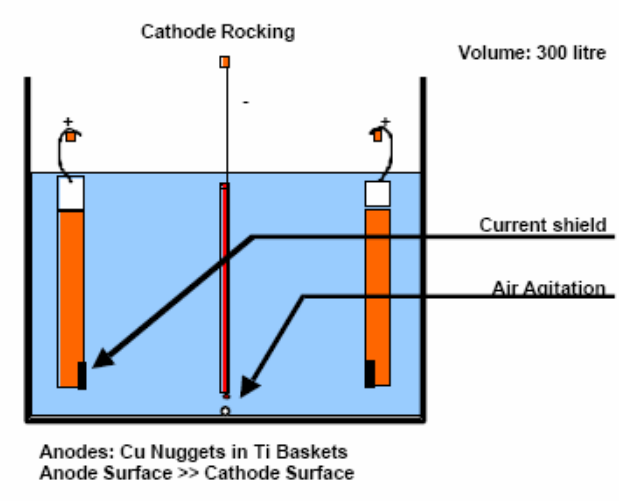

Figure 5

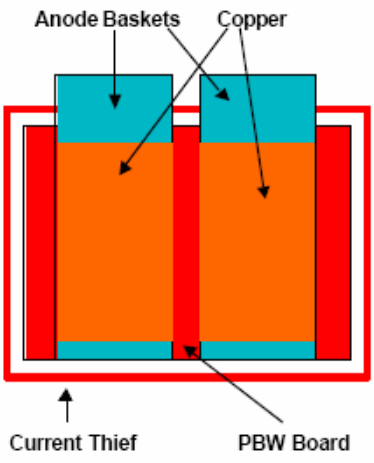

Figure 6

A large board was plated at 1.5 A/dm^2 for 90 minutes in the adjusted plating environment and the via filling yield was complete for all smaller vias of identical dimensions and independent of location on the board surface. However the yield was reduced when the dimension of the vias was altered, as shown in Figure 7 (7a: VFY= 2, 7b: VFY = 4). Under these conditions the through hole metallization was > 80%.

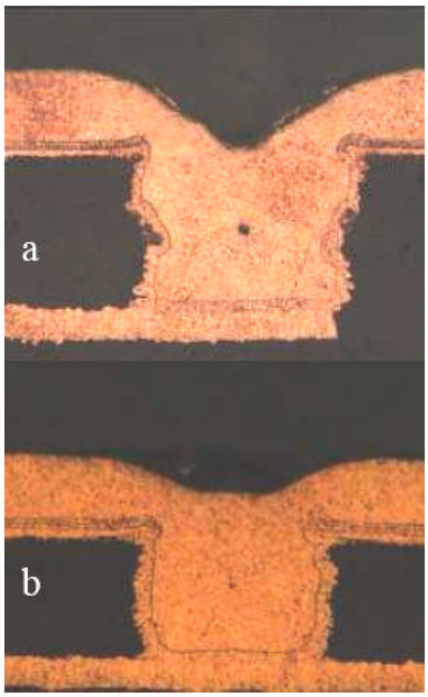

Figure 7 – Via Fill Efficiency for Boards Plated under Optimal Conditions with 1.5 A/dm^2 DC

(Via size: (a) depth 70 µm, diameter 100 µm at the bottom and 110 µm at the surface, (b) depth 60 µm, diameter 100 µm at the bottom, 125 µm in the middle and 100 µm at the surface.)

A second FR-4 board was plated with an average current density of 1.4 A/dm^2 for 100 minutes and of 9 randomly sampled vias of different sizes, the fill yield was identical for via sizes, higher than 10 (Figure 8). The through hole metallization was increased to over 85 % (Figure 9). The board passed thermal cycle testing, with no corner cracking (Figure 10).

Under the same plating conditions, Figure 11 shows a well-filled microvia (140 µm diameter) even with 20 µm overhang.

Next patterned boards (600 x 550 mm) were plated at 1.5 A/dm^2 for 60 minutes. Thickness distribution over the boards was good as was the via fill and the through hole copper distribution (Figures 12a, 12b and 13).

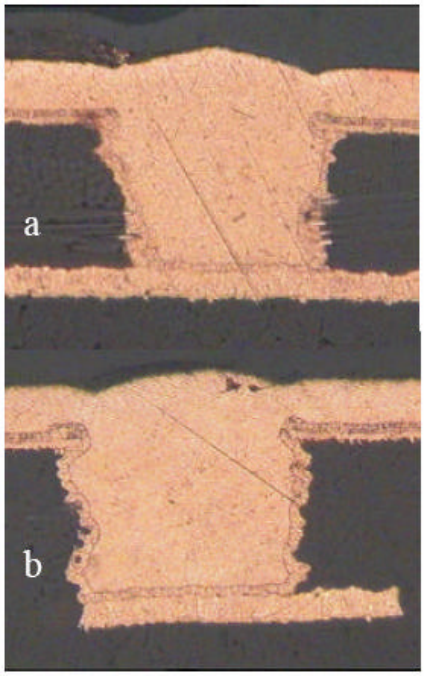

Figure 8 - Via fill efficiency for boards plated under optimal conditions with an average current density of 1.4 A/dm^2 DC

(Via size: (a) depth 65 µm, diameter 100 µm at the bottom and 115 µm at the surface, (b) depth 75 µm, diameter 115 µm at the bottom, 125 µm in the middle and 125 µm at the surface.)

Figure 9 - Through Hole Metallization of Panel Board with PTH > 85 % using an Average Current Density of 1.4 A/dm^2 for 100 Minutes (Hole diameter: 0.2 mm)

Figure 10 - After Thermal Cycle Test (10 cycles: 255° C +/- 5° Molten Salt 30 Seconds // RT Water 15 Seconds)

Figure 11 - Copper Metallization of Microvia (Diameter 140 µm) with Strong Overhang (20 µm)

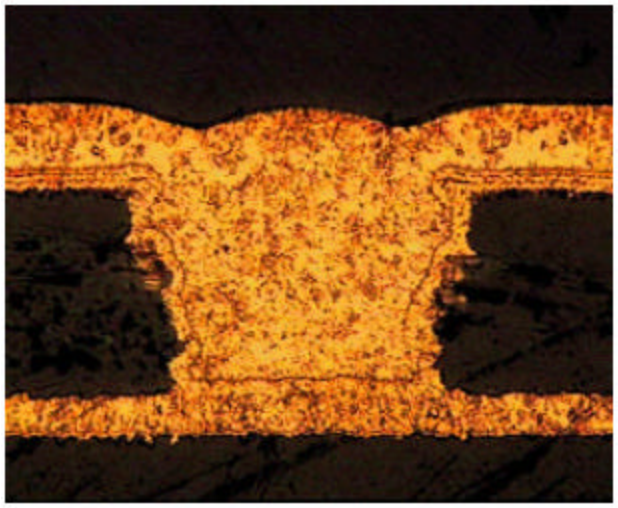

Figure 12a - Copper Metallized Microvia of a Patterned Board

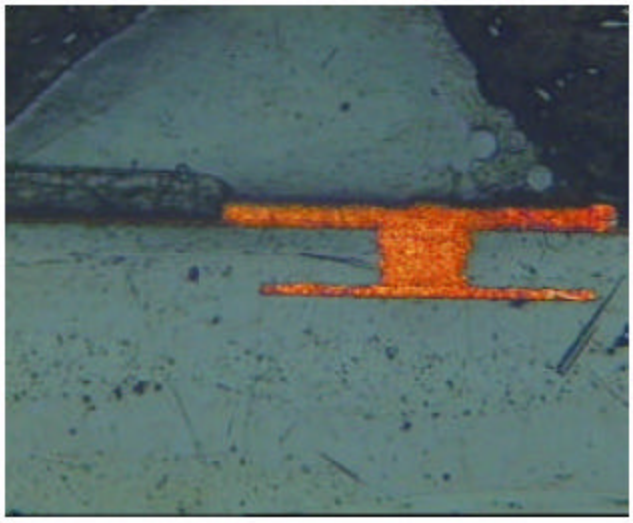

Figure 12b - Copper Metallized Microvia of a Patterned Board

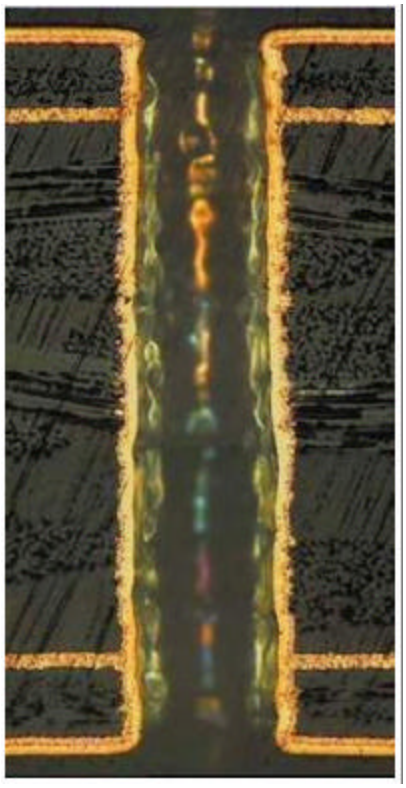

Figure 13 - Through Hole Metallization of Patterned Board with PTH > 85% using a Current Density of 1.5 A/dm^2 for 60 Minutes (Hole diameter: 0.2 mm)

Discussion

Differences between the plating environment under laboratory conditions, compared to larger sized volumes in industrial applications is significant; tank dimensions and distances, hydrodynamic uniformity and strength, anode:cathode ratios, all influence the uniformity of the current distribution.

However, by appropriate utilisation of a variety of processing techniques available today, it's possible to create stable and uniform plating conditions under industrial conditions, hence reproducing results from laboratory experiments.

In the efforts to metallize large boards with both vias and through holes, air agitation, bar rocking, vibration, anode shielding, cathodic current thieves, anode:cathode ratio and current design was combined appropriately and as the results presented shows, the process capability identified in the early R&D project stage was reproduced after volume scale-up.