Presented in the ECWC 10 Conference at IPC Printed
Circuits Expo®, SMEMA Council APEX® and
Designers Summit 05

Advanced Filled Via Plating Methodology

Takayuki Haze, Seungchul Kim, Changhyun Nam, Seokwon Ahn,
Jung Hwan Park, and Sujin Kim
Samsung Electro-Mechanics Co., LTD
Chungnam, South Korea

Abstract
This paper describes Advanced Filled Via Plating Methodology for stacked via technology. In this paper, via bottom crevice, via bottom land etching and electroless copper plating coverage is focused to achieve filled via plating enhancement.

Introduction
Requirement for Flip Chip Packaging Substrate links to high density, high speed trend and semiconductor performance in the electronics market and there are several technical challenges such as fine patterning, higher electric characteristics, higher reliability, higher frequency and multi functionality. For examp le, 10um/10um of line/space, 100um of bump pitch, less than 3.0 of Dk, 16ppm of CTE, all stacked via structure and embedded passive are shown in the technology trend for Flip Chip Packaging Substrates. To realize such requirements, development for core technology of fine pattern fabrication, new process and new material are demanded. For stacked via fabrication, there are two typical methods in the industry. One is to build a filled via on a filled via sequentially. Another is to connect via posts by parallel lamination using solder plating, Indium plating, metal paste or nothing in the interface.

This report describes new methodology of filled via fabrication for stacked via technology enhancement. Filled via is fabricated by electroless copper plating and electrolytic copper plating. Recently, new plating chemical and current control for electrolytic plating has been found to easily fill inside vias. However, via bottom connection to via bottom land is important to insure reliability and stability of any via filling capability. I have found other important elements such as via bottom structure and electroless plating through the analysis of filled via mechanisms.

This report is an analysis of the filled via mechanism and a new plating methodology using electroless plating and electrolytic plating to resolve unstable plating problem caused by via bottom crevice, via land etching and poor electroless plating coverage at the via bottom area.

Micro Via Fabrication Method
Photo Via Hole Fabrication
There are two typical fabrication methods for via holes in the industry. One is a Photo Via Hole fabrication method. Initially micro via technology started with photo via holes because photo via holes were fabricated by the existing exposure/develop technique with photosensitive material. Figure-1 shows an example of the manufacturing process flow.

The advantage of this method is it allows one to make many via holes at the same time by exposure and develop. The larger work size provides higher productivity. In making via holes with a larger work size, optical alignment exposure and glass masks are required to keep good registration.

Segment type or projection types of exposure have better than +/-10um registration capability. Table 1 shows material and tools for fabrication of photo via holes.

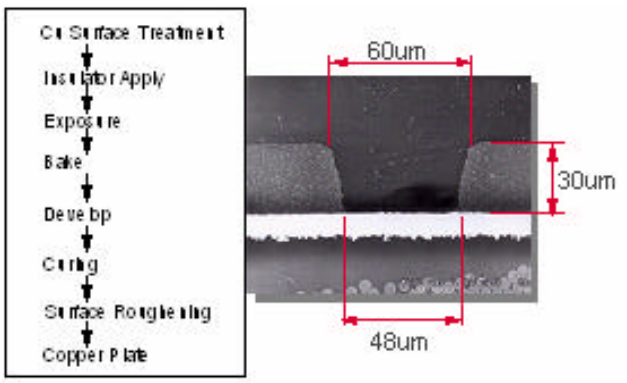

Figure 1 – Process Flow of Photo Via

Table 1 Material & Tools for Photo Via

Process	Tools	Material
Copper Surface Treatment	Vertical Dip Type machine	Chlorite treatment or Etching type treatment
Insulator Apply	Slot coater or Curtain Coater	Photo sensitive epoxy resin
Dry	Continuous Oven or Batch type Oven	NA
Exposure	UV Exposure with optical alignment	NA
Bake	Batch type Oven	NA
Develop	Horizontal type machine	Solvent or Alkaline
Cure	Batch type Oven	NA

In this case, cleanliness of process environment and tools are very important to keep yield up because the photosensitive material can cause insulator voids by contamination during insulator applying and exposure process.

Therefore both the facility and tools for photo via holes are expensive. Other concerns are the material properties. To achieve better resolution for micro via holes and better reliability, material development is necessary. PCB makers do not have this capability and material makers need a huge investment. Therefore Photo Via resolution is currently staying at a minimum of 60 microns shown at the top in Figure 1. This is an infrastructure hurdle preventing the increase of the photosensitive material's capability.

Laser Via Hole fabrication

Another Fabrication Method is Laser Via Hole. Many PCB makers have introduced laser via hole fabrication technique as an advanced method that is based on infrastructure of laser drill capability. Figure 2 shows an example of manufacturing process flow.

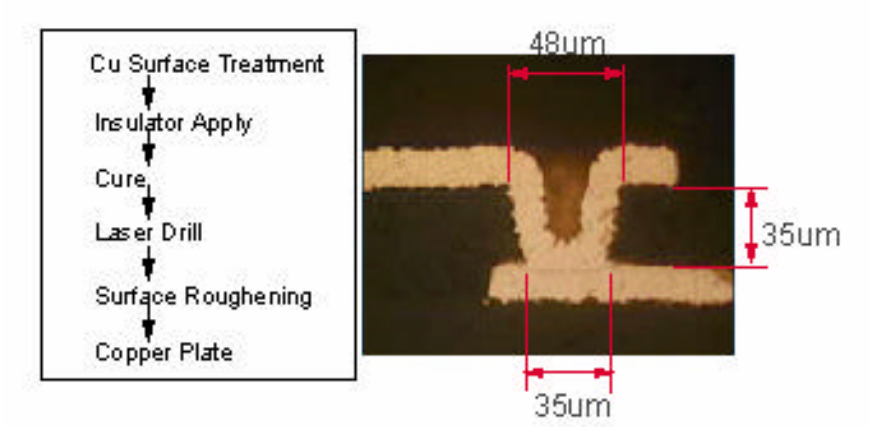

Figure 2 – Process Flow of Laser Via

Table 2 – Material & Tools for Laser Via

Process	Tools	Material
Copper Surface Treatment	Vertical Dip Type machine	Chlorite treatment or Etching type treatment
Insulator Apply	Vacuum Laminator	Thermal Cure type Epoxy Resin (Dry Film Insulator)
Dry	Batch type Oven	NA
Laser Drill	CO2 Laser Drill or YV Laser Drill	NA

The advantage of this method is that many via holes can be made easier than the photo via method that requires special photo sensitive material and special techniques such as exposure/develop. Insulator materials have no requirement of photosensitive properties and this provides us with a lot of opportunity to select insulator materials based on product requirements. Processes steps are also less than complex than the photo via method. Laser via holes are made by drilling each hole so that drill speed of Laser Drill Machine is the most important parameter from the view point of productivity. Alignment accuracy and via hole diameter is also an important capability when we choose to use a Laser Drill Machine. Table 2 shows material and tools for laser via hole fabrication.

In this case, tool sets are described based on dry film resist that is the most popular material for Laser Via Technology in the industry. There are two key tools for this method. One is the Vacuum Laminator that is used to laminate the dry film insulator on a board and to make a flat surface. Another is the Laser Drill Machine that is used to make via holes on the dry film insulator. In the industry, both CO2 Laser Drill Machines and UV YAG Laser Drill Machines are available, and their capability for drill speed and minimum via diameter are increasing significantly. Physically, CO2 Laser Drills can make minimum 50 micron via holes and UV YAG Laser Drill can make minimum 25 micron via holes. Therefore, Laser Drill methodology is generally applied to IC Packaging Substrates and High Density Substrates that require smaller via holes.

Stacked Via Fabrication Methodology

Laser Drill and Via Filling Plating

There are two typical methodologies for Stacked via fabrication in the industry. One is to fabricate Stacked via structures by repeating the via fabrication by Laser drill and the via filling by copper plating. Figure-3 shows an example. With this method it is possible to integrate the Sequential Build-Up Process with the existing Laser Drill technology and Via Fill Plating technology. Many PCB makers apply this method to IC Package Substrate. This method easily realizes finer pattern and multilayer, however it needs a longer manufacturing lead time and unstable via filling and unstable reliability of the via connections are a concern. This paper describes a methodology to improve via filling and via connection reliability for Via Fill technology of Stacked Via fabricated by Laser Drill and Via Fill Plating.

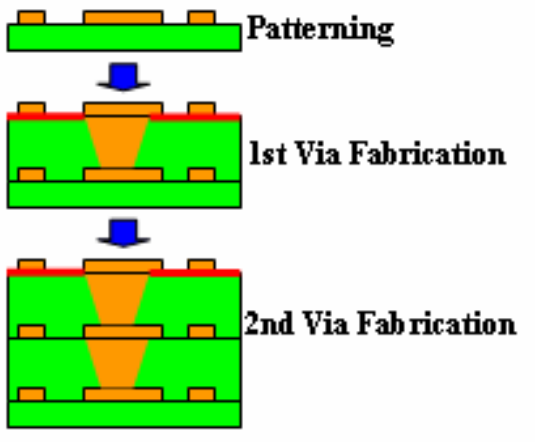

Figure 3 - Stacked Via Fabrication by Laser Drill and Plating

Via Post and Parallel Laminate

Another method to fabricate Stacked Via is to fabricate the layer with Via Post by the Pattern Plating method and to fabricate a stacked structure by parallel laminating these layers. Figure-4 shows an example. Since this method dominates the technology to fabricate Via Post and to connect between Via Post and Via Post, few PCB makers apply this method to High Density PCBs. Shorter manufacturing lead time by parallel process is this methods merit, but the applicable technology is limited because of the difficulty of obtaining good reliability of the Via-Via connection and alignment between layers. However, due to higher productivity, this method has the potential to become main stream with future technology innovations.

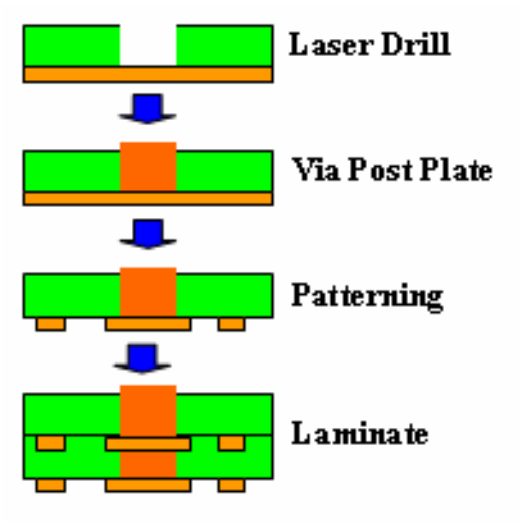

Figure 4-Stacked Via Fabrication by Parallel Laminate

Plating Mechanism for Filled Via Fabrication

To fabricate Stacked Vias by Laser Drill and Via Fill Plating, Filled Vias should be fabricated with uniform Via Fill Plating and high reliability of the via-via connection. A Semi Additive Plating process is also required to fabricate high density patterns so that a High Density IC Package Substrate requires the fabrication process capable of fabricating both Fine Pattern and Filled Via by the Semi Additive process at the same time. Pattern thickness has to be controlled by setting the plating speed and the plating time to fabricate pattern using the Semi Additive Plating process. Shown in Figure 5 above is the concept of pattern fabrication and Via Fill Plating by Semi Additive Plating. Here the via inside should be filled during the plating time for pattern fabrication. However, via filling is often insufficient and reliability problems occur because of insufficient via connections. This technology is not an established process, yet.

Therefore, further technology innovation is required for future finer pattern and smaller micro vias. To investigate ways to solve these concerns, the mechanism of Via Fill Plating is analyzed by measuring plating thickness during pattern fabrication and via filling by the Semi Additive Plating process. The design of the test vehicle and measuring points are shown in Figure 6. Figure 7 shows the copper plating thickness of each measurement point with an increase in electrolytic plating time up to Plating Time-E after electroless plating. As a result of this experiment, we see that plating speed at the via bottom is slow until plating time C. But the plating speed becomes faster after about time C for the via bottom plating thickness.

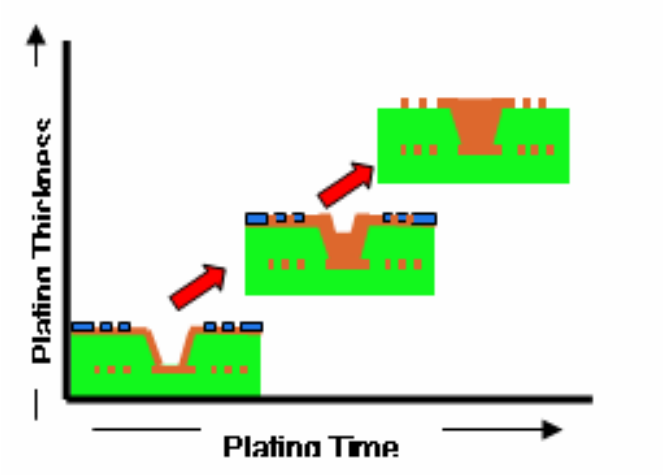

Figure 5 – Plating Concept

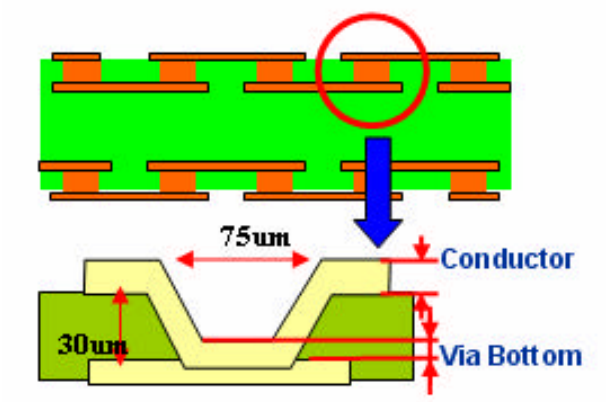

Figure 6 – Measurement Point

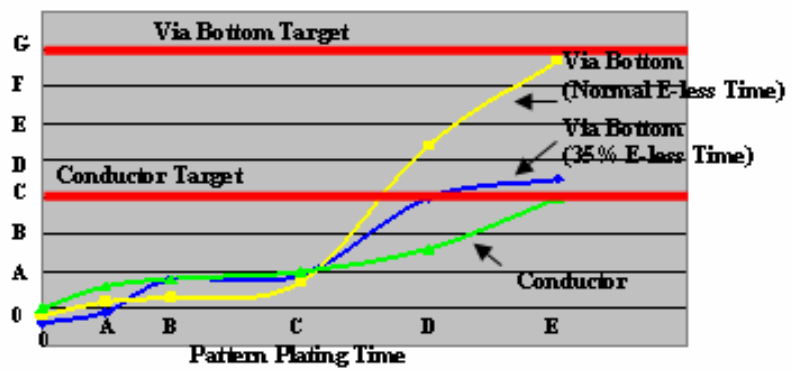

Figure 7 – Plating Thickness

Then, the via bottom with the thicker electroless plating shows a faster plating speed. To investigate the cause of this result, Figure 8 shows the cross-section of the via showing via fill plating at each plating time. As shown in this cross-section, the via connection between via wall and via bottom seems to be insufficient and the resistance of via connection seems to be high. This could be caused by the low plating speed at time B of plating. However, after time B, the resistance of via connection caused by the increase via of the wall thickness and via connection area could cause the plating speed to increase. The problem with this mechanism is that via inside is not sufficiently filled within plating time E, because the plating speed at via bottom increases after time B out until plating time E. Figure 9 shows this suspicious model.

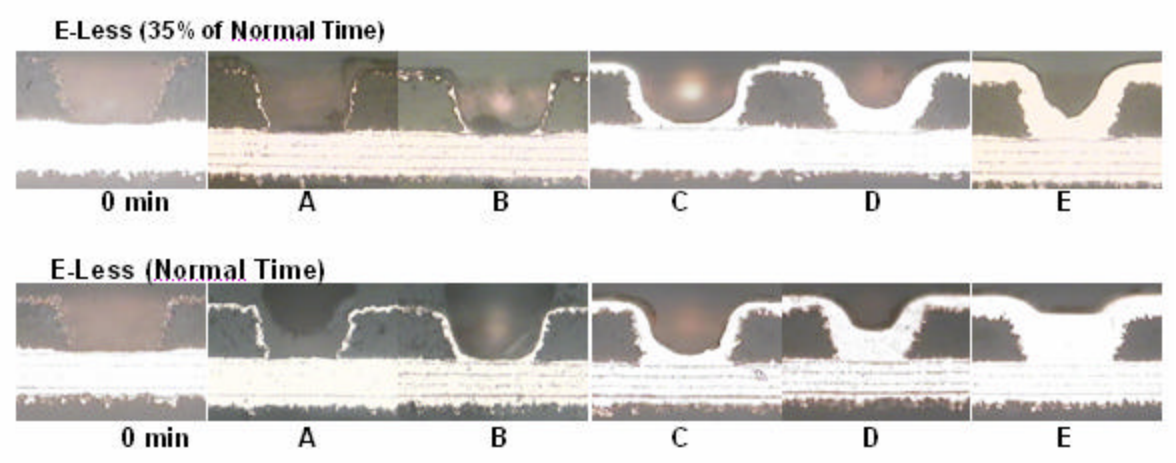

Figure 8 – X-Section of Plated Via

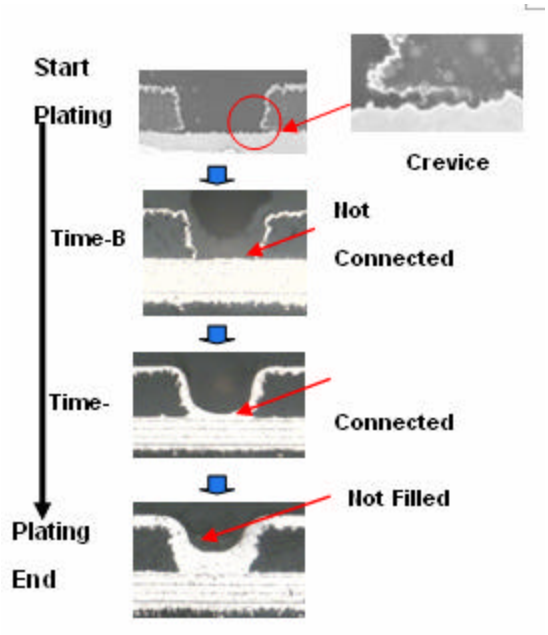

Figure 9 – Insuffient Via Fill Model

Via Bottom Feature Analysis

As the cross-section shows, the reason why the connection between via wall and via bottom is insufficient until plating time B appears to be that a sufficient connection is not achieved until the electrolytic plating increase giving poor electroless plating coverage of the crevice at via bottom. To verify this estimation and to investigate the cause of the crevice at via bottom, the resistance between via wall and via bottom is measured after electroless plating for vias drilled by UV YAG Laser and CO2 Laser. The intent is to measure the resistance of the via connection using m-ohm meter after Laser Drill, Desmear, Electroless Copper Plating and cut the surface pattern shown in Figure-10.

The resistance of UV YAG Laser is 20 times higher than CO2 Laser. X-sections of each via are shown in Figure-11. UV YAG Laser shows about 2X longer crevice than the CO2 Laser. In addition, SEM photos of via bottom after Laser Drill were used to investigate the cause of this process. No crevice is observed at via bottom drilled by CO2 Laser, but a crevice is observed at via bottom drilled by UV YAG Laser. To investigate the cause why UV YAG Laser makes a longer crevice at via bottom, the wave length of energy absorption is compared for the UV YAG Laser and CO2 Laser. As shown in Figure-12, UV YAG Laser shows a higher energy absorption for FR-4 material, copper and glass. CO2 Laser shows higher energy absorption for FR-4 material, but low energy absorption for copper and glass. Therefore, it can be postulated that the cause of crevice is that energy of the UV YAG Laser is absorbed by copper of the via bottom during Laser Drill, then this energy impacts the interface formation between dielectric and via bottom copper. As a summary of the above experiment and observations, we can say that when vias are fabricated by UV YAG Laser, the connection between via wall and via bottom is insufficient after electroless copper plating due to crevice formation. As a result via filling is insufficient within the

electrolytic copper plating time for patterning using Semi Additive Plating process due to slow electrolytic plating speed. CO2 Laser has only a low risk of causing this type of problem. However a UV YAG Laser is required to fabricate future smaller vias and this concern has to be solved to fabricate finer patterns and smaller micro vias at the same time using Semi Additive Plating process.

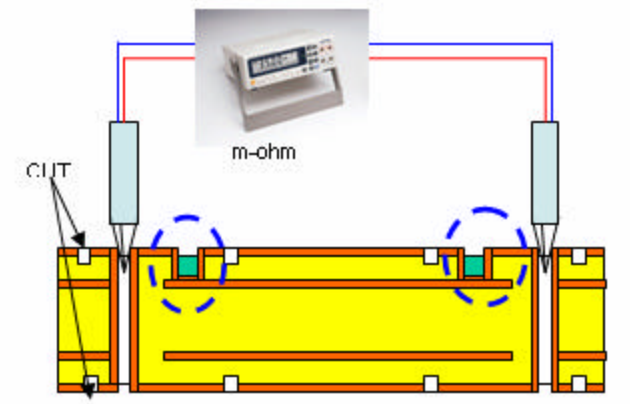

Figure 10 – Electrical Resistance Measurement

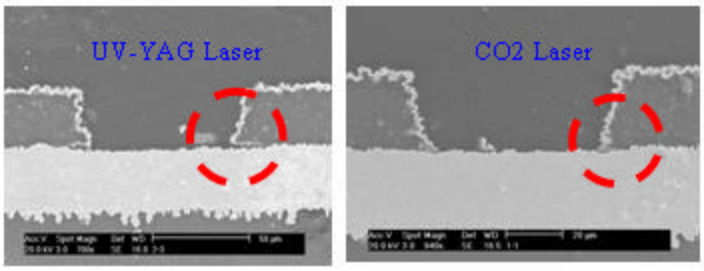

Figure 11 – X-Section after E-Less Plate

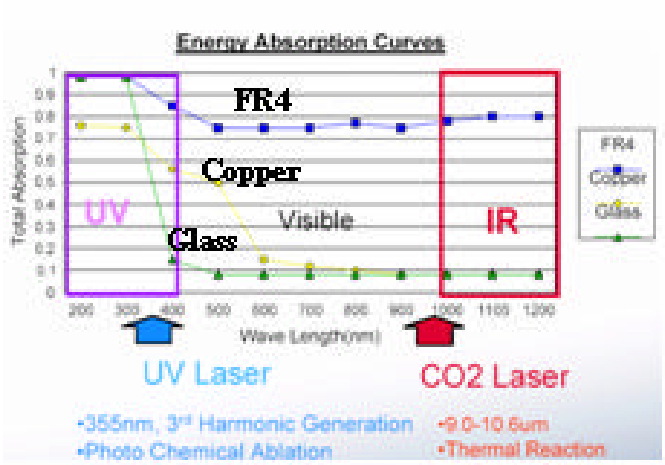

Figure 12 – Energy Absorption

New Concept of Filled Via Plate

As a result of via bottom feature analysis, it is confirmed that via filling is not easy if there is via bottom feature like a crevice at the via bottom connection area. There is another possible cause for process variation, i.e. via bottom etching by soft etching of pre-treatment for electroless copper plating and insufficient electroless plating thickness. Therefore, a new concept to fabricate stable filled vias is needed. Figure 13 shows the new model. The key point of this concept is to plate only the via bottom after Laser Drill and Desmear and before electroless copper plating of the seed layer for the Semi Additive Plating process. Via bottom plating thickness should be more than 3um as the analysis result of Figure 7 shows. After this pre-plating on the via bottom, finer patterns and smaller filled vias are fabricated by electroless copper plating of the seed layer for Semi Additive Plating process, Resist Patterning, Electrolytic Plating and seed layer remove and resist strip. Pre-plating on via bottom is possible using both the self catalyst type of electroless plating shown and the Pd catalyst type of electroless plating shown in Figure 14 and electrolytic plating in the case of via bottom connected to electricity supply conductor.

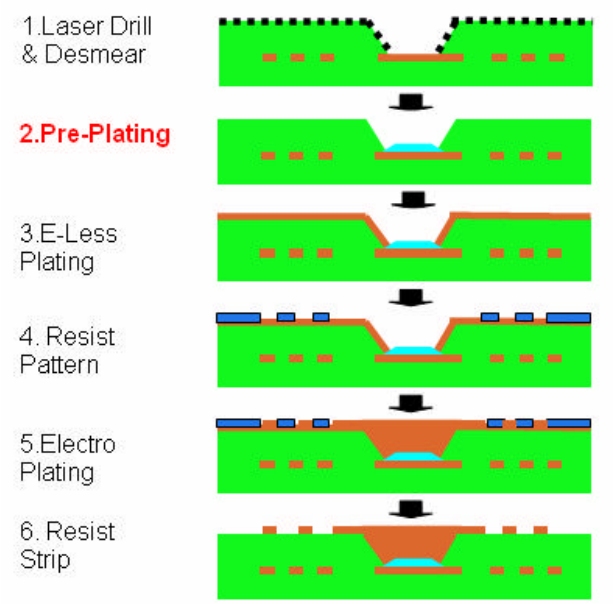

Figure 13 – New Model of Filled Via Plating

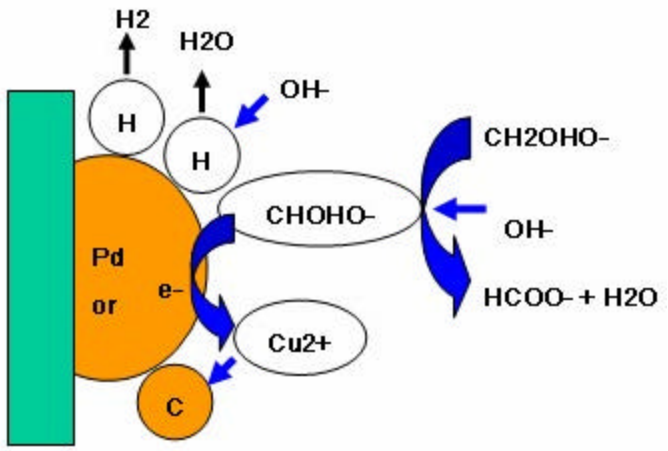

Figure 14 – Electroless Cu Plating

Feasibility of Via Bottom Pre-Plate by Electroless Copper Plate

As shown in Table-3, three plating methods were tried for this experiment: self catalyst type of electroless copper plating, electroless copper plating with catalyst for electroless Ni plating and electroless copper plating for full additive plating. As a result, Pre-Plating on Via Bottom has been confirmed using all three methods as shown in Figure 15, Pre-Plating using the existing Electroless Plating shows unstable plating thickness. On the other hand, Full Additive Plating shows stable plating thickness. Also, Pre-Plating has been confirmed to fill the crevice inside. Based on the above, the feasibility of the new concept shown in Figure 13 has been confirmed.

Table 3 – Pre-Plating on Via Bottom

	Test-1	Test-2	Test-3
Plating Type	Electroless Plating for Pattern Plating		Full Additive Plating
Catalyst	Pd	Cu	Pd

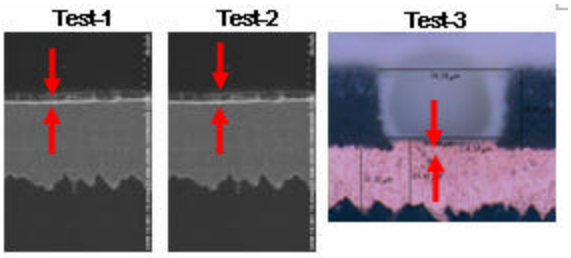

Figure 15 – Pre-Plating on Via Bottom

Trial of Filled Via Fabrication with Via Bottom Pre-Plate

In case B of Pre-Plating thickness on the Via Bottom, reference the plating speed data in Figure 7, Via Filling is possible to achieve by about 60% of the current Electrolytic Plating time and the process window for this is kept within the current plating time of Electrolytic Plating shown in Figure 16. Also, future fine patterns with less than 15um Cu thickness can be fabricated, because Via Filling is possible to achieve by Pattern Plating time reduction.

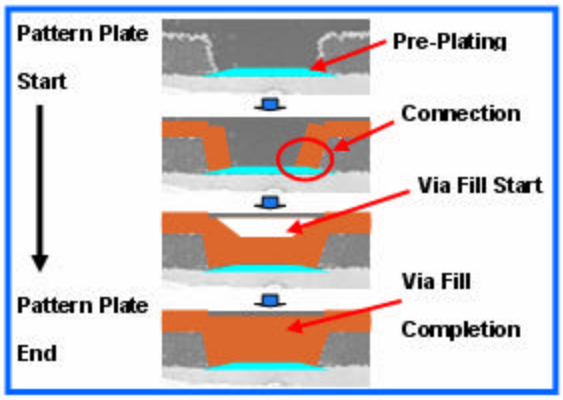

Figure 16 – Via Fill Plating With Pre-Plate

Summary and Recommendation

Vias should be filled within the plating time for pattern fabrication to fabricate both Filled Via and Fine Pattern using a Semi Additive Plating process. Plating time for Via Filling is related to the electro resistance between via bottom and via wall after Electroless Plating.

The electro resistance between via bottom and via wall is related to the crevice at the via bottom and the thickness of Electroless Plating. Pre-Plating on via bottom by Electroless Plating is effective to get lower electro resistance between the via bottom and via wall. Pre-Plating provides benefits such as pattern plating time reduction and thinner conductor thickness for fine pattern fabrication.

References

- Minoru Toyonaga “Plating Technology for Printed Circuit Board in 1999”
- Samsung Electro-Mechanics Co., Ltd, “Micro Via Reserch Report in 2004”
- C.Uyemura & Co., Ltd, “Information of Copper Plating in 2004”
- Manabu Yamada “The technology of simultaneous of formation of fine pitch patterns and filled via holes by a new semi additive process in MES2002 ”
- Takayuki Haze “Via Hole Fabrication Methods and Productivity for Micro Via Technology” in ECWC9