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### **High Power LED and Thermal Management**

### Dr.-Ing. Dipl.-Phys. cand. habil. Adrian O. H. Mahlkow Optotransmitter Umweltschutz Technologie (OUT) e.V. Berlin, Germany

#### Abstract

A high-power-SMD-LED (HL-LED) outline 3,3 x 2,9 mm<sup>2</sup> was developed, with chip-size up to 1 mm<sup>2</sup> and power dissipation up to 1.500 mW (400 mA for UV-InGaN) in a corresponding thermal ambient. The thermal resistance is 12 K/W. For high integrated applications (spotlights, general lighting) special PCBs with isolating layers thinner than 10  $\mu$ m (commercial solutions: 75  $\mu$ m) was developed also. Modules on 1 mm copper, area 40 x 40 mm<sup>2</sup> with 100 HL-LEDs, P<sub>tot</sub> = 50 W, P<sub>opt</sub> = 8 W in amber (592 nm) and thermal resistant 6 K/W were demonstrated.

#### Introduction: The High-Power LED

A High-Power LED (HL-LED) for the spectral region 405 to 980 nm covered today from commercial available semiconductor chips was developed. This device allows bias current up to 1000 mA, in comparison to 70 mA until now. The HL-LED outline is  $2.9 \times 3.3$  mm<sup>2</sup>. The goal of the device is a very low thermal resistance less than 12 K/W due to a core made of copper. Thus the chip as light emitter can operate with very high performance. The actual chip size is in the range of 200 to 1000 µm in square. In conventional surface-mounted LEDs (SMD-LEDs) power dissipation up to 150 mW at room-temperature is possible, therefore a maximum current of approximately 70 mA emerges for most chips. The High-Power LED can handle power dissipation up to 1500 mW, thus cw-operating with 1000 mA and more becomes possible. Because of the 10-times higher current 10-times higher light flux with a semiconductor chip is possible. The chip size can be increased to reduce the current-density (meaning the current per chip-surface) to minimize the aging of the semiconductor-material also.

For mechanical base of the LED standard PCB-substrate (FR4, FR5, Caplan, etc.) is used.<sup>3</sup> New in the comparison to conventional devices is that a thick inner layer<sup>2</sup> added to the upper<sup>5,8</sup> that lower layers<sup>1,4</sup>. So an excellent contact with very low thermal resistant to the peripheral PCB is established and the heat emitted by the LED-Chip<sup>7</sup> is taken away. For conventional constructions this is the main limiting point for power dissipation and current. The chip sits in a cavity<sup>9</sup> that serves as reflector and as heat sink. It serves as back contact too. Thus a very good electric and thermal contact is formed. Upward, a clear or toned potting compound forms the mechanical conclusion of the device made of epoxy.<sup>6</sup> See Figure 1. Important for an operating lifetime of 100.000 hours and more is a secure derivative of the heat at the mechanical boundary of the LED where it is soldered on the PCB. By selection of the walls and/or the depth of the sack-hole and the thickness of the metallization, the optical features can be adapted to the chip in its expansion, thickness, emission-wavelength, shape, aspect-relationship, position of the transition-layer, splendor-description, etc. and the external splendor-behavior is influenced positively. For operating at maximum ratings of the LED a good thermal conduction via the solders of the device to a fitting periphery is essential. Almost universal soldering (iron, reflow, ...) established an effective binding with low thermal resistance and very good conductivity. The Figures 2a/b depicts the temperature distribution in top view for a LED operating at 1000 mW in comparison to a microscopy image for orientation.



Figure 1 - Principal Construction of a High-power LED (HL-LED)



## Figure 2a, b - Left a Microscopy Image in Top view, on the Right with Same Magnification a Micro Thermal Image taken with a Resolution of 20 μm - The Chip (Red Rectangle) Operates at 1000 mW, the Maximum Temperature Appears is 54°C.

#### **Simulation of Heat-Distribution**

To investigate the principle limits of this design we simulated the thermal distribution with a complex 3D-model with some million lines and a professional software solution *CFX RC*. Some results are shown in Figure 3:



#### Figure 3 - 3D-Image of Results in a Thermal Equilibrium (Top). Cut Parallel to X-axes through the Data-Matrix (Bottom) Thermal - Resistance from Chip (White Area) to Pad (Dark Grey) is about 24 K/W (P<sub>disp.</sub> = 1000 mW)

With the results of the simulation we redesigned the basic-material and the mechanical structure to optimize the thermal resistance. The resistance of the pure device is 12 K/W, in the simulation the resistance of the chip substrate is added with also 12 K/W. For InGaN on sapphire we get in total less than 14 K/W. These results correspond with our measurements.

#### **Measurements of Thermal Distribution**

We measured the thermal distribution with a spatial resolution of about 50  $\mu$ m first to optimize the material parameter used for simulation and second to check the results of the simulation. The simulation matches with reality better than 5 % for different dissipation power and ambients. The Figure 4 shows the experimental setup we used for pictures like Figure 2b.



Figure 4 - Experimental Setup for Thermal Imaging

(On the right hand the liquid nitrogen cooled camera with macro optics made of CdS mounted on an optical bank. The High Power LED is soldered on a copper plate.)

All thermal images in this paper are taken with this setup. To get a realistic thermal equilibrium even at lower power a thermal management is very important and for good results the total ambient resistance should be lower than 2 K/W. To drive the High Power LED at their limit and get the maximum output using the advantage of the small size we developed also efficient thermal management for this device.

### **Thermal Management**

There are a lot of ideas and technical solution for heat spreading, dissipation and cooling for devices with high power in the region of some dozens of watts, e.g. processors, power diodes, These techniques are active solutions with fans and/or water flow. We have tried to find solutions that are all passive have and no moving parts. The basic idea is based on metal core PCBs of some ten years ago but the commercially available products are not satisfactory. So we have optimized them. First layer is a sheet of metal (copper, aluminum) followed by a electrical is olating layer. To reduce the normal thermal resistance the thickness is reduced as much as possible. This is done with commercially available materials giving a thickness in the region of 75  $\mu$ m. On this isolating layer follows the structured layer or layers with the power dissipaters soldered or glued on the top. The isolating is necessary for a structured board with different electrical potentials. There are to ways to reduce the thermal resistance of the isolating layer: First is the use of materials with excellent thermal conductivity, e.g. diamond or sapphire. Second is the use of normal materials and the reduction of thickness. The first way is very expensive and not useful for big scale industrial production. The High Power LED is a device driven with some volts so the dielectric breakdown cannot be lower than some tens of volts. The goal was to reduce the thickness drastically by one order of magnitude. Figure 5 shows a cross section of our material with a LED on top:



Figure 5 - Cross section of metal core PCB on an aluminum-cooler and single LED on top. The isolating layer is about 10 μm, one order of magnitude thinner than other comm. materials.

#### Simulation of different designs

A second idea for efficient cooling (entwärmen) involves thermal through-hole platings (THP). With simulation we compare these concepts with real models and prepare design rules for both. The Figure 6 shows in a simulated and a measured heat distribution picture of the same structure:



Figure 6 - Results of Thermo-Simulation (First, Inset: Microscopy Image) in Comparison to the Measurements (Second)

The solder pad for the LED shows 72 through-hole platings ( $\emptyset$  0,2 mm) in a very narrow array. Figure 7 shows a bottom view. In the cross section the heat distribution through all important structures is shown (right). The comparison to the results for metal core PCBs shows the expected fact that the equilibrium temperature is much lower than for thermal THP:



Figure 7 - Simulated Thermal Distribution of a LED with P<sub>tot</sub> = 1000 mW on a Metal Core PCB with Isolating Layer Thickness 10 µm - Right is depicted the Density of Weight for Clarification of the Structure

#### **Thermal Imaging of Optimized Structures**

With different design rules for optimized structures different LED-modules where constructed. First a linear module with thermal THP with a normal density of devices and second (described here) a high integrated LED-spot with 100 devices nearest to each other on an area of (4 cm).<sup>2</sup> (See Figures 8 and 9.)



Figure 8 - Thermal Image of a Light-Line with LED and Thermal THP - The Max. Temperature is about 37° C



Figure 9 - Image taken from a 100 LED-Spot with Maximum Density

(The max. temperature is 42°C and the total power dissipation about 80 W (400 mA per LED) with a optical flux 2900 lm (AlInGaP,  $\lambda_P = 595$  nm))

With the developed thermal management one has industrial scalable techniques to construct LED-based lamps for general lighting.

# High-Power LED and Thermal Management

## Dr. Adrian Mahlkow OUT e.V. Berlin

Wednesday, February 23, 2005 in 213AB (11<sup>30</sup> -12<sup>00</sup>)

# Principal construction



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## **Thermal Characterisation**



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## Thermal Management



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## Thermal Management



### Thermal through hole platings (THP)

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## Calculations



### Metal core PCB with high-power LED

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## High power LED and thermal management Moduls (with thermal THP)



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## Moduls (with IMS-PCB)



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