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Lead-Free Product Transition: Impact on Printed Circuit Board Design and Material Selection

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Abstract
Electronic products are being stressed by increasing operating temperatures and higher assembly temperatures. Silicon and product power consumption are increasing as the silicon densities and signaling frequencies increase. And, the transition to lead-free solders is resulting in higher thermal excursions during assembly. Both of these conditions are impacting material selection during product design and are having an impact on product qualification, and influencing long term via reliability.

This paper details the results of an Intel investigation of printed circuit board materials, fabrication processes, and design variables and the resulting impact on board reliability after lead-free assembly. Results were baselined against standard tin-lead assembly for purposes of comparison. Printed circuit board process and design variables examined included via size, layer count, board thickness, and laminate material. Also examined were the variation within an individual supplier and the variation across multiple suppliers using the same materials. The paper details the test board configurations used in the study, the lead-free and tin-lead assembly profiles to which the boards were subjected, and the test methods employed to collect the data. The test data highlights key trends in the reliability data as a function of changes in the variables tested.

Introduction
Global environmental legislation is dictating the transition from current Sn/Pb assembly processes to Pb-free components and assembly processes with many recycling and disposal statutes in place today to limit the use of lead in electronics. A major influence in the conversion from Sn/Pb to Pb-free processing is the European Union's Restriction on Hazardous Substances (RoHS) legislation that is due to take effect July 1, 2006. There are many component and assembly challenges that result in meeting the lead content requirements of the legislation and still have product that works reliably. The primary challenge with Pb-free assembly is the higher temperatures required to melt the alternative alloys (see Figure 1). The SnAgCu alloy family has a melting point 34C higher than standard Sn/Pb and a process temperature range that is at least 25C higher than standard Sn/Pb solder paste (see Figure 2). The impacts of a higher assembly temperature to the printed circuit board include both the components and board materials both of which must be qualified to ensure that the impact on their performance is manageable.

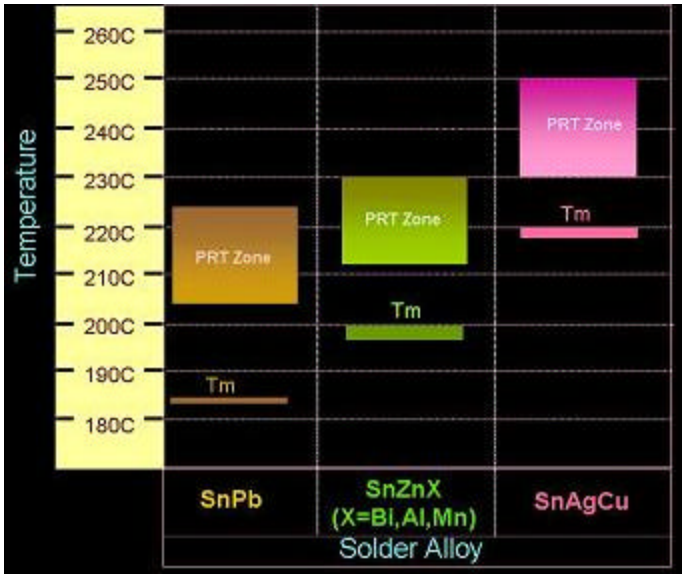


Figure 1 - Melting Temperatures and Reflow Process Temperatures for Solder Alloys

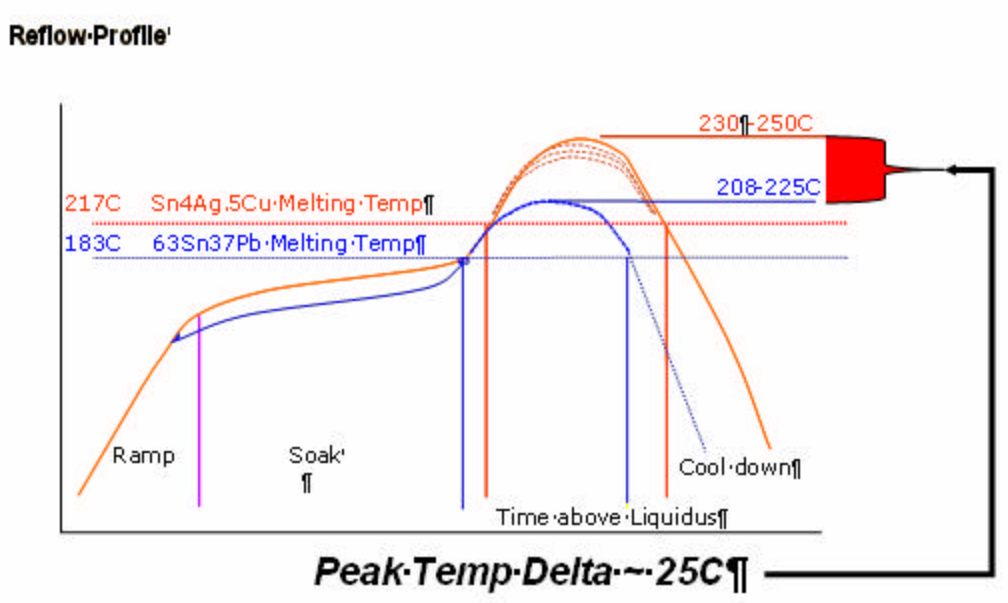


Figure 2 – Differences in Reflow Profiles for Sn/Pb and SnAgCu Alloys

Test Vehicle Descriptions

Data was collected from 3 different test board designs. The test boards were similar in that they utilized a common working panel of 18"X24" and contained test structures to quantify multiple aspects of the supplier's process capability and the board material's characteristics.

The first board was a 4 layer, 0.062" thick design focused mainly on supplier capability. The design was similar to the current IPC PCQR^2 4 layer test board design, in that it used Conductor Analysis Technology (CAT) test modules for the majority of the panel's design, but also included a set of Interconnect Stress Test (IST) coupons to look at via reliability. All the test board via structures were through hole vias with sizes ranging from 10 mils to 35 mils as drilled.

The second test board was an 8 layer, 0.062" thick design that combined elements of a supplier capability board with a test board focused more on material capability. The design still contained all the standard IPC PCQR^2 CAT modules, but added a wide variety of electrical test structures to study the Dk, loss, impedance tolerance, and frequency response of the materials being used. The board design also included multiple sets of IST coupons to look at via reliability. Again, all the test board via structures were through hole, and the sizes ranged from 10 mils to 35 mils as drilled.

The final test board studied was a true material capability board. The design was modular, with 4 versions of layer count and thicknesses investigated for this test. The thinnest version was an 8 layer, 0.040" thick design. It incorporated multiple via structures (through hole, buried, and microvias) as part of its suite of IST coupons. A 0.062' and a 0.077" thick version of the same 8 layer design were also built. A 16 layer design was also built at a thickness of 0.093". In all builds the through hole vias ranged from 10 mils to 35 mils as drilled. All the buried vias were from layer 2 to layer n-1 and were 10 mils as drilled. And the microvias were from layers 1 to layer2 and from layer n to layer n-1. The suite of IST coupons contained both 4 mil and 5 mil diameter, as drilled, microvia test structures on all 4 versions.

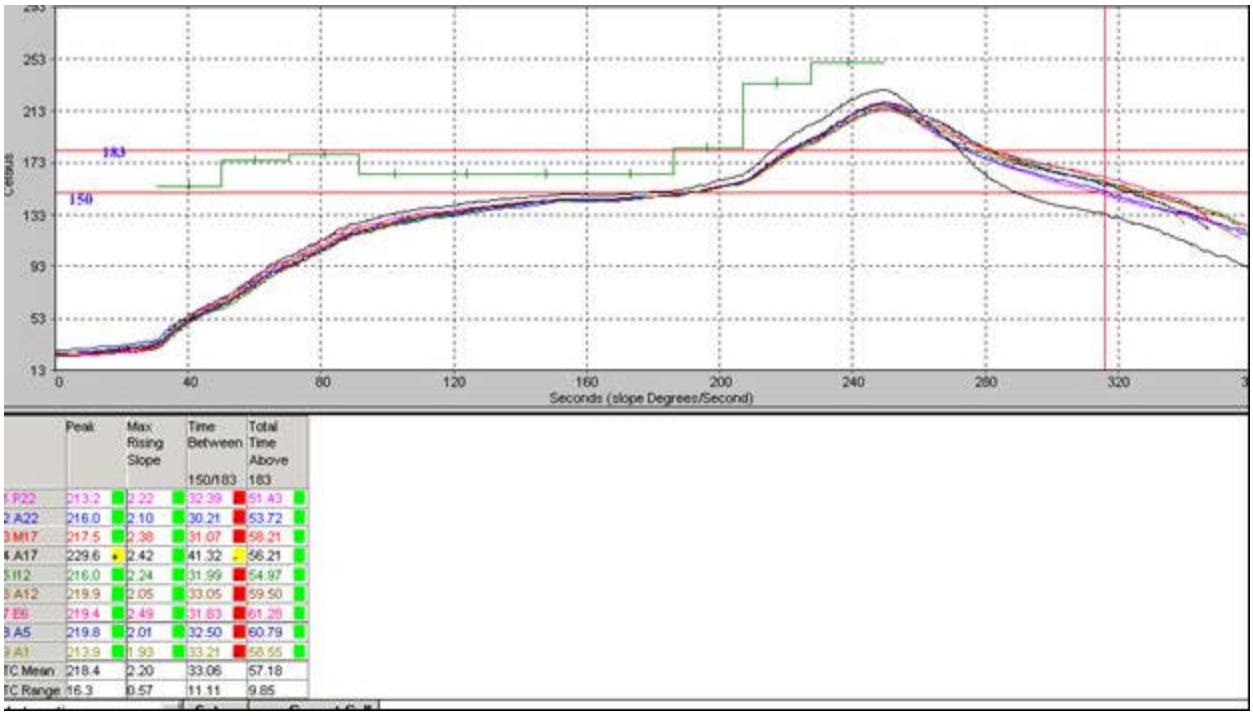
The primary objective of all three test boards was to challenge the supplier's high volume capabilities in all aspects of the board fabrication process, and capture limits of both the supplier's capability and the material performance through the test results. All boards were instructed to be built to IPC class 2 copper thickness requirements for each of the via structures. Material selection and stack-up were varied by design, but were dictated to the suppliers for each build. Three lots of 10 panels each were built for each of the supplier builds tested. The three lots were instructed to be from different raw material lots and built at three distinct intervals through the factory to capture as much material and process variation as possible. A summary of the test board conditions is listed below in Table 1.

Table 1 – Summary of Test Board Conditions

Supplier	Layers	Material Type	Thickness (mils)	Material Tg (in C) (TMA)
A	16	170 Tg FR4	0.093	158
B	4	FR4	0.062	144
B	8	FR4	0.062	130
B	8	FR4	0.062	135
B	8	FR4	0.062	139
B	8	FR4	0.077	145
C	8	FR4	0.062	125
C	8	FR4	0.062	123
C	8	FR4	0.04	129
C	8	FR4	0.077	138
C	8	170 Tg FR4	0.077	153
C	16	170 Tg FR4	0.093	151
D	4	FR4	0.062	146
D	8	FR4	0.062	139
D	8	170 Tg FR4	0.062	156
E	4	FR4	0.062	146
E	8	FR4	0.062	136
E	8	FR4	0.062	127
E	8	FR4	0.062	125
E	8	FR4	0.077	121
E	8	170 Tg FR4	0.077	156
E	16	170 Tg FR4	0.093	153
G	4	FR4	0.062	141
H	8	FR4	0.062	124
H	8	170 Tg FR4	0.062	152

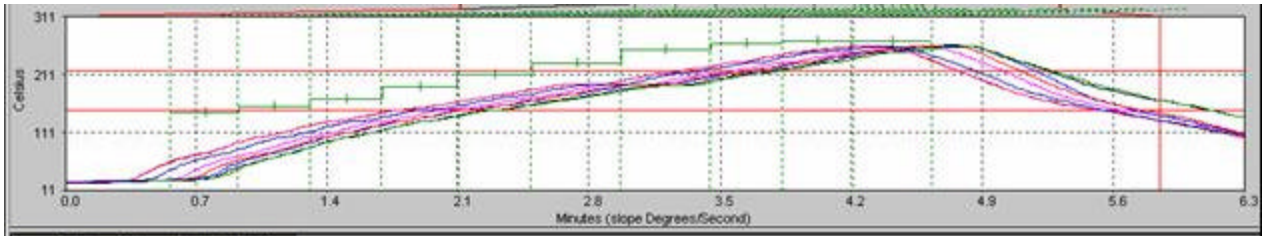
Assembly Conditions

The assembly test conditions were based on high volume consumer product processing. A 220C peak reflow temperature and 60 second time above liquidous (TAL) assembly profile was used as a SnPb baseline for the study. Two Pb-free reflow assembly conditions were used in the testing to simulate different Pb-free process conditions. The first Pb-free assembly reflow profile had a 240C peak reflow temperature and 90 second time above liquidous. The second Pb-free assembly reflow profile increased the peak reflow temperature to 260C and maintained the 90 second time above liquidous condition. Figures 3 and 4 show the 220C and 260C reflow profiles used in this study. Each board was subjected to 3 reflow processes, the top side of the board was alternated between each reflow. The choice of three passes through reflow was based on typical high volume assembly conditions for consumer type products. The three passes were not intended to simulate a worst case assembly condition that may arise on some products due to complexity and/or excessive rework.



	Peak	Max Rising Slope	Time Between 150/183	Total Time Above 183
1 P22	213.2	2.22	32.39	51.43
2 A22	216.0	2.10	30.21	53.72
3 M17	217.5	2.38	31.07	58.21
4 A17	229.6	2.42	41.32	56.21
5 I12	216.0	2.24	31.99	54.97
6 A12	219.9	2.05	33.05	59.50
7 E6	219.4	2.49	31.83	61.28
8 A5	219.8	2.01	32.50	60.79
9 A1	213.9	1.93	33.21	58.55
TC Mean	218.4	2.20	33.06	57.18
TC Range	16.3	0.57	11.11	9.85

Figure 3 – SnPb 220C Peak Reflow Temperature Profile



	Peak	Max Rising Slope	Rising Time Between 150/217	Total Time Above 217
1 P22	259.5	2.69	91.60	87.43
2 A22	262.2	2.80	91.72	91.35
3 M17	261.6	2.71	89.34	87.91
4 A17	259.7	2.33	87.66	89.36
5 I12	258.8	2.57	89.56	88.81
6 A12	261.2	2.70	90.24	89.41
7 E6	259.9	2.87	89.25	89.30
8 A5	258.5	2.89	87.95	88.11
9 A1		0.00	0.00	0.00

Figure 4 – Pb-Free 260C Peak Reflow Temperature Profile

At least 2 boards from each of the 3 lots of 10 boards provided by the supplier were subjected to the three reflow conditions. All boards were examined after each reflow pass for signs of blistering or delamination. Two of the individual supplier-material builds exhibited blistering or delamination after the first reflow pass of the 260C profile. The blistering/delamination worsened on both builds with each subsequent reflow pass. Neither build exhibited delamination or blistering during the 220C reflow passes. Both of the builds which exhibited blistering or delamination were high Tg FR4 material. There were other builds using other high Tg FR4 materials which exhibited no blistering or delamination at any of the reflow conditions. Examples of the delamination/blistering condition are shown in Figure 5. After blistering and delamination was noticed, additional boards from the same builds were baked at 105C for 8 hours to remove moisture as a potential cause. Subsequent reflow passes using the 260C profile on the baked boards also resulted in blistering and delamination.

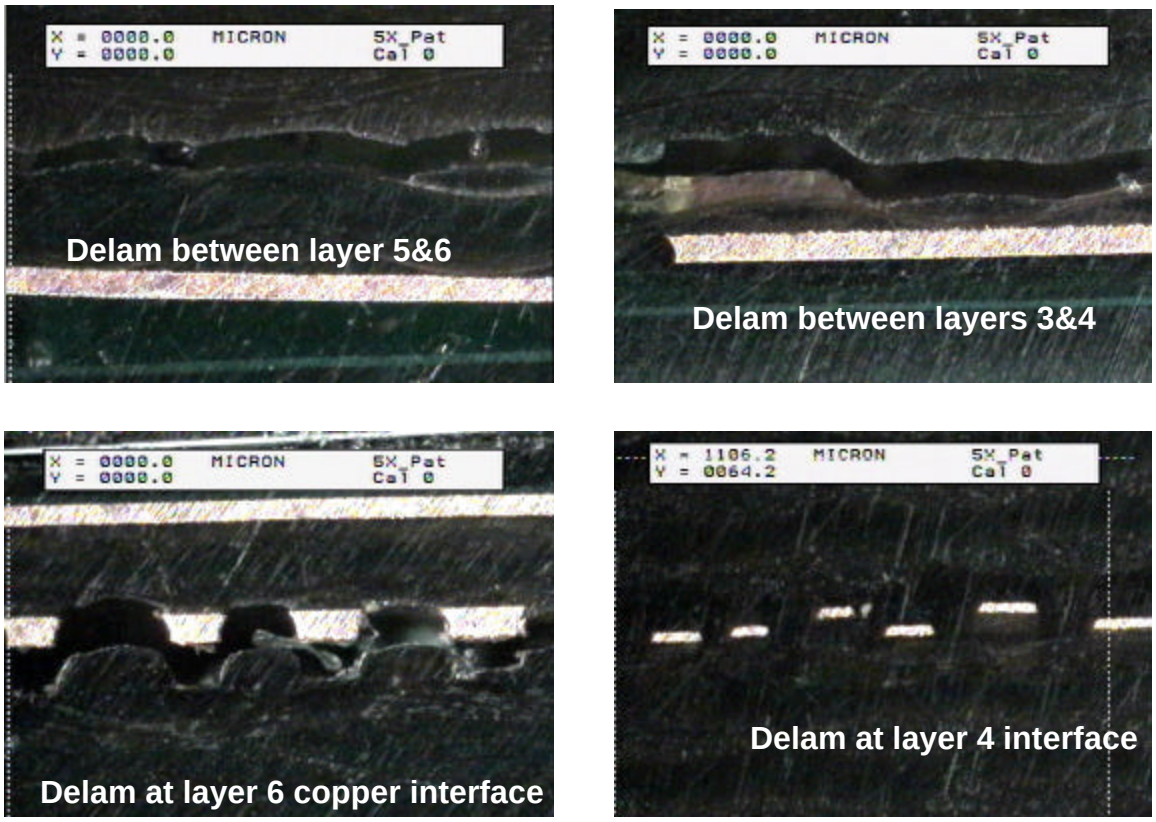


Figure 5 – Examples of Delamination/ Blistering of High Tg FR4 Build after 260C Peak Reflow Assembly Conditioning

Test Method
All IST daisy chain circuits were tested for continuity and initial resistance prior to assembly simulation. Any circuit which showed open prior to assembly was eliminated from further testing. Any circuit which passed the initial continuity check, but failed after assembly was considered to have 0 cycles as its failure level. The Interconnect Stress Testing (IST) method IPC-TM-650 2.6.26 was performed at the conditions listed below.

IPC-TM-650 2.6.26 parameters
Test Temp: 150°C
Max. Resist. Change: 10%
No. of Cycles: 500 cycles or failure whichever comes first
Data Coll. Freq.: 10 cycles
Cooling Ratio: 0.66
Acceptance Criteria: Minimum 150 cycle average and no coupons fail before 100 cycles

The principle of IST testing is to use the resistance of an interwoven circuit to heat the sample through an applied current and to convection cool the sample with forced air. The heating portion of the thermal cycle is fixed at 3 minutes, and the cooling segment is allowed to float based on the size and mass of the sample. A sampling of the failed IST coupons were micro-sectioned for failure mode identification. Multiple failure modes were discovered. The failures can be compiled into 3 categories: 1) Barrel fractures, 2) Knee fractures, and 3) Interconnect separation. Failures in the small via sizes (10, 12, 14, and 16 mil drill) were predominantly barrel fractures. The larger through holes (35 mil drill) exhibited a mixture of all three failure modes. The failure locations on the larger holes were predominantly towards the external layers of the coupon. The failure location on the smaller vias were predominantly towards the center layers of the coupon. Figure 6 shows examples of the failure modes seen on the samples.

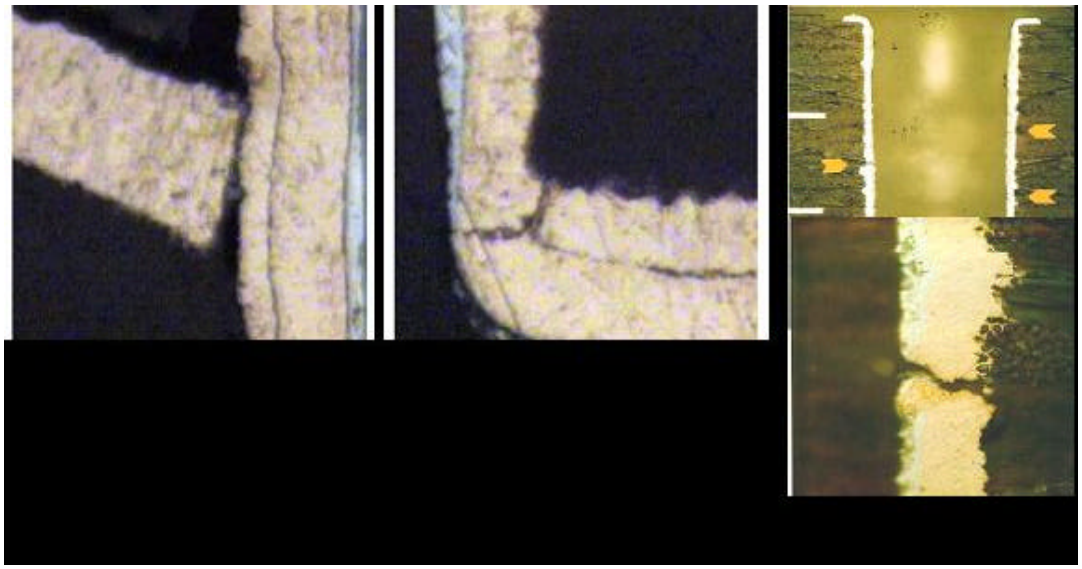
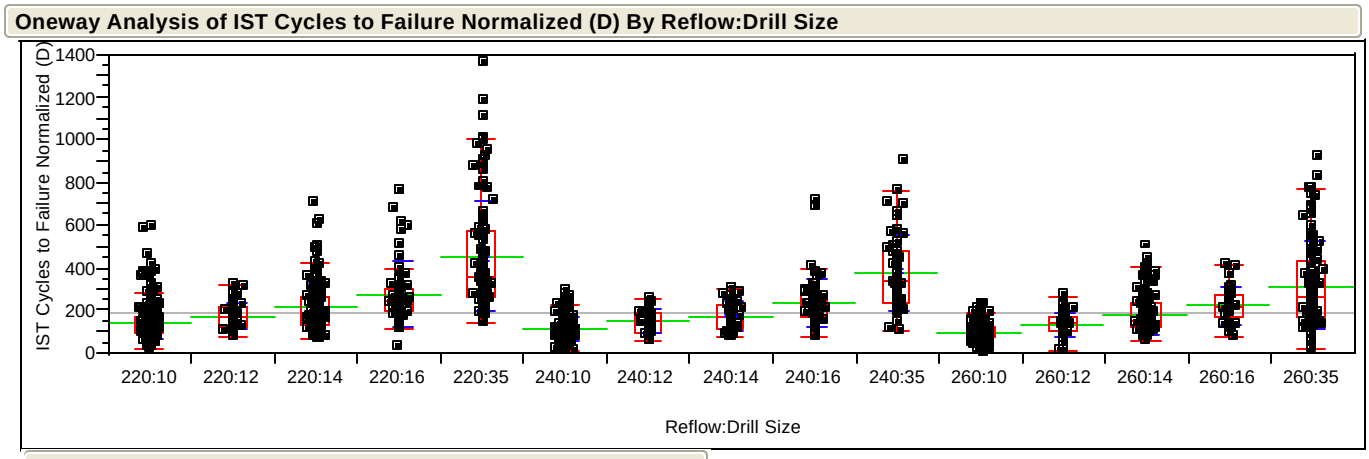


Figure 6 – Examples of IST Test Failure Modes

Via Size Results

Data was collect across 5 different drill sizes for all the builds (10, 12, 14, 16, and 35 mils in diameter). Not all drill sizes were tested on each build, but all builds contained 10 mil drill data. The data within each supplier build was normalized to the average 10 mil drill performance at 260C reflow assembly process for the build with the average scaled to a 100 cycle to failure. This allowed pooling of multiple suppliers builds for cross comparison of data between different reflow conditions and via sizes. The results are charted in Figure 7 below.



Means and Std Deviations

Level	Number	Mean	Std Dev	Std Err Mean	Lower 95%	Upper 95%
220:10	314	144.971	79.001	4.458	136.20	153.74
220:12	43	173.622	63.500	9.684	154.08	193.16
220:14	142	217.105	112.374	9.430	198.46	235.75
220:16	60	279.399	151.963	19.618	240.14	318.66
220:35	99	458.041	259.657	26.096	406.25	509.83
240:10	204	109.655	54.253	3.798	102.17	117.14
240:12	42	149.620	52.976	8.174	133.11	166.13
240:14	42	175.862	69.144	10.669	154.32	197.41
240:16	60	238.675	112.281	14.495	209.67	267.68
240:35	53	374.308	178.480	24.516	325.11	423.50
260:10	255	100.001	40.364	2.528	95.02	104.98
260:12	40	139.180	54.380	8.598	121.79	156.57
260:14	134	185.436	92.164	7.962	169.69	201.18
260:16	30	226.052	88.749	16.203	192.91	259.19
260:35	90	316.615	205.574	21.669	273.56	359.67

Figure 7 – Normalized IST Performance by Reflow Peak Temperature and Via Size

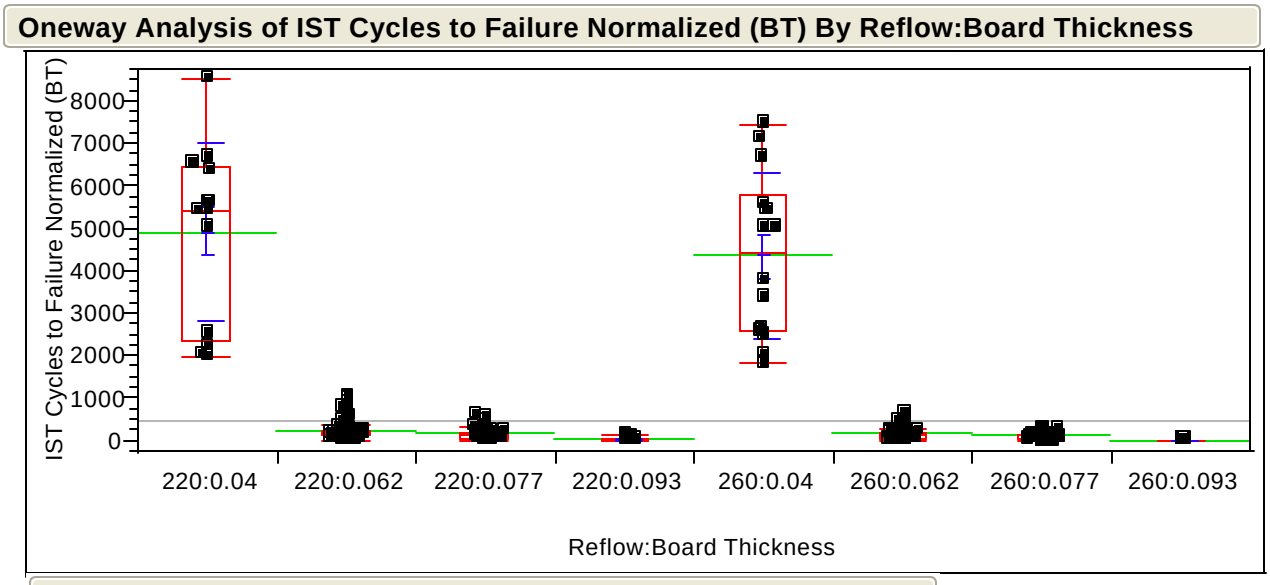
The resulting data is consistent with expected results (via IST cycles to failure decrease as via size decreases, and the increased assembly temperatures reduce the via IST cycles to failure for the same size via). The average reduction, for all the drill sizes, in via IST cycles to failure between the standard 220C Sn/Pb assembly and the 260C Pb-free assembly was 23%. Table 2 contains a comparison of the average IST cycle performance of each drill size and reflow temperature conditions. The data summarized in Table 2 indicates that a shift to Pb-free assembly reflow profiles has approximately the same impact on via IST cycles to failure as dropping via size by 2mil.

Table 2 – Comparison of Cycle performance of Drill Size vs. Reflow Peak Temperature

	Reflow Temperature				
Drill Size	220	240	260	220-240 Delta	220-260 Delta
10	145	110	100	24%	31%
12	174	150	139	14%	20%
14	217	176	185	19%	15%
16	279	239	226	15%	19%
35	458	374	317	18%	31%
			Avg	18%	23%

Board Thickness Results

Four board thicknesses were tested as part of the investigation using the third test board design. An 8 layer version of the design was built at 0.040", 0.062", and 0.077" thickness. A 16 layer version of the design was built at 0.093" thickness. The data comparison for the board thickness parameter was limited to two suppliers which built at least three different thicknesses of the design. The results were normalized to 100 cycle average for the 0.077" thickness versions of each supplier's builds by drill size and material type at the 260C reflow temperature condition. The results are shown in Figure 8.



Means and Std Deviations

Level	Number	Mean	Std Dev	Std Err Mean	Lower 95%	Upper 95%
220:0.04	13	4930.17	2091.14	579.98	3666.5	6193.8
220:0.062	104	210.88	192.03	18.83	173.5	248.2
220:0.077	61	165.27	113.82	14.57	136.1	194.4
220:0.093	9	66.46	24.08	8.03	47.9	85.0
260:0.04	14	4360.40	1943.29	519.37	3238.4	5482.4
260:0.062	99	150.77	107.76	10.83	129.3	172.3
260:0.077	64	100.00	49.36	6.17	87.7	112.3
260:0.093	9	37.57	7.97	2.66	31.4	43.7

Figure 8 – Normalized IST Performance by Board Thickness and Reflow Temperature

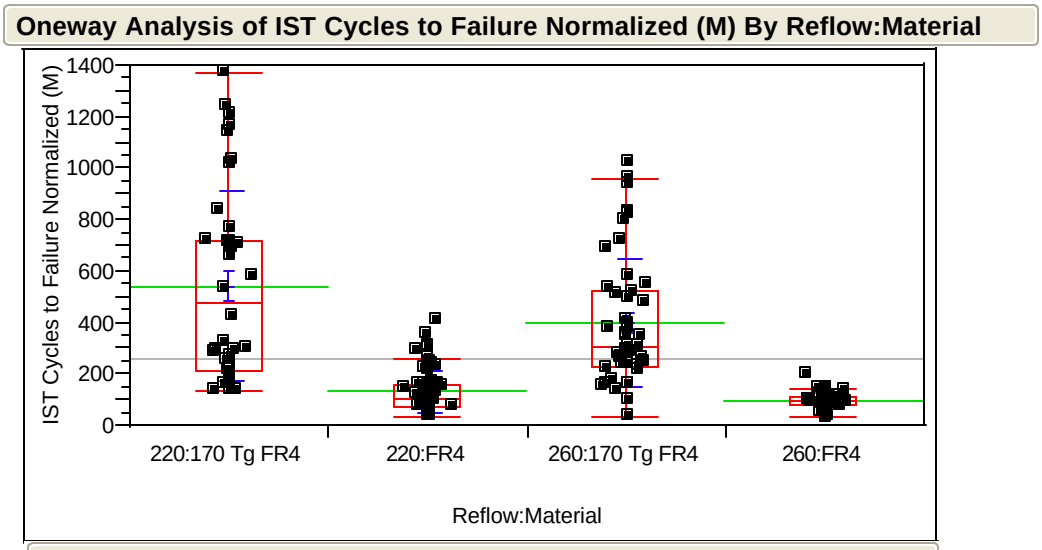
Results of via IST cycles to failure by board thickness vs. reflow temperature follows modeled results in that the thinner boards resulted in higher IST cycles to failure. The percentage reduction in via IST cycles to failure when moving fromthe standard 220C Sn/Pb assembly to the 260C Pb-free assembly increased as board thickness increased. These results show that Pb-free assembly has a greater effect on thicker, higher aspect ratio board constructions. This data also indicates that the concern with via IST cycles to failure as a result of Pb-free assembly is reduced as the printed circuit board is made thinner. Table 3 contains the comparative analysis of the data.

Table 3 – Comparison of IST Cycle Performance of Board Thickness vs. Reflow Temperature

	Reflow Temperature		
Board Thickness	220C	260C	220-260 Delta
0.04	4930	4360	113%
0.062	211	151	140%
0.077	165	108	153%
0.093	66	38	177%

Material Results

Two types of glass reinforced epoxy materials (Standard FR4 with a Tg ~130C and High Tg FR4 with a Tg ~170C) were examined in this investigation. Across the different suppliers of test boards, multiple different laminate manufacturers' versions of each glass reinforced epoxy materials were utilized. The results were normalized to 100 cycle average for the High Tg FR4, 260C reflow condition by supplier, board thickness and via size where the same supplier built both materials at the same conditions. The normalized data is shown in Figure 9.



Means and Std Deviations

Level	Number	Mean	Std Dev	Std Err Mean	Lower 95%	Upper 95%
220:170 Tg FR4	40	544.419	366.048	57.877	427.35	661.49
220:FR4	64	134.462	81.452	10.181	114.12	154.81
260:170 Tg FR4	45	400.507	247.779	36.937	326.07	474.95
260:FR4	57	99.998	27.969	3.705	92.58	107.42

Figure 9 – Normalized IST Performance by Material and Reflow Temperature

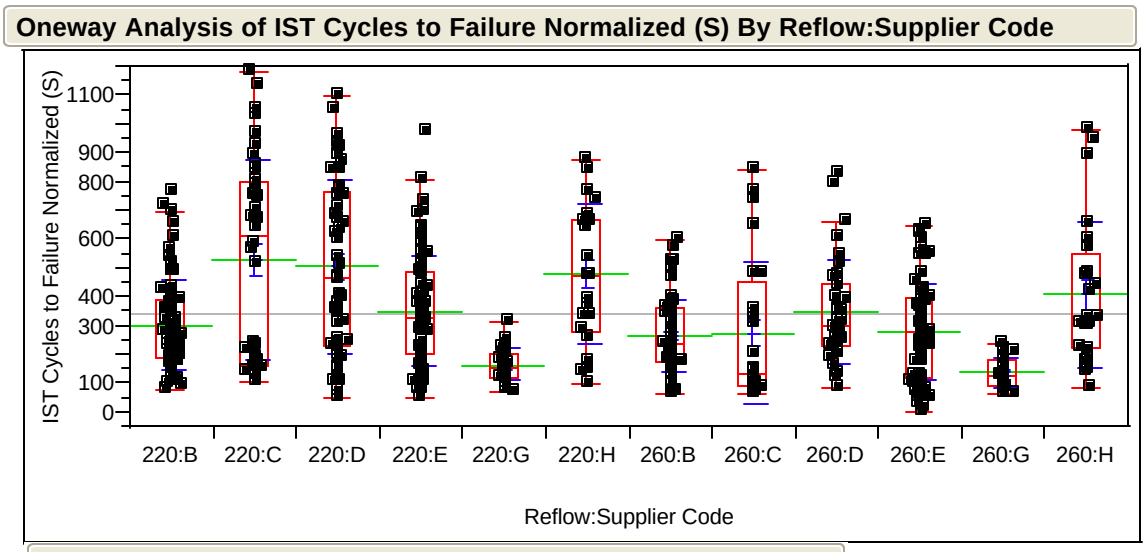
The high Tg (170 Tg) FR4 material's average via IST cycles to failure performance was higher than the standard FR4 material's via IST cycles to failure for both the Sn/Pb and Pb-free assembly temperatures. This data shows that the decrease in the average via IST cycles to failure due to the increased assembly temperature was essentially the same for both the standard FR4 and high Tg FR4. At both the Sn/Pb and Pb-free assembly reflow temperatures, the high Tg FR4 material had approximately a 4x average via cycles to failure increase in performance compared to the standard Tg FR4 material. It is noted that while the difference in average IST cycles to failure performance was significant between standard FR4 and High Tg Fr4, the minimum IST cycles to failure were essentially equal at the 260C reflow temperature condition. Table 4 shows the deltas of the 2 materials vs. reflow temperature

Table 4 – Comparison of IST Cycle Performance of Material vs. Reflow Temperature

	Reflow Temperature		
Material	220C	260C	220-260 Delta
FR4	134	100	134%
High Tg FR4	544	390	140%
		Avg	137%

Supplier Results

The analysis for the supplier-to-supplier comparison and analysis between supplier build lots were limited to the 0.062" thick standard FR4 builds. Six suppliers were analyzed with test board designs built with standard FR4. Four of these suppliers built multiple test board designs and build lots with the same standard FR4 material requirement. These results were normalized to 100 cycle average performance for the C1 supplier build at 260 C reflow condition by drill size. The data shown in Figure 10 is the cumulative IST performance data of multiple builds by supplier. Table 5 shows the difference between the average IST cycle performance of the cumulative builds vs. reflow temperature for each supplier.



Means and Std Deviations

Level	Number	Mean	Std Dev	Std Err Mean	Lower 95%	Upper 95%
220:B	82	303.275	154.182	17.027	269.40	337.15
220:C	42	530.747	347.198	53.574	422.55	638.94
220:D	48	506.572	300.158	43.324	419.42	593.73
220:E	80	352.259	187.345	20.946	310.57	393.95
220:G	24	163.477	60.671	12.384	137.86	189.10
220:H	22	480.640	240.710	51.320	373.92	587.37
260:B	62	267.605	123.330	15.663	236.29	298.93
260:C	28	276.189	248.066	46.880	180.00	372.38
260:D	34	349.890	178.365	30.589	287.66	412.12
260:E	71	279.714	169.492	20.115	239.60	319.83
260:G	24	138.663	52.291	10.674	116.58	160.74
260:H	24	409.333	252.803	51.603	302.58	516.08

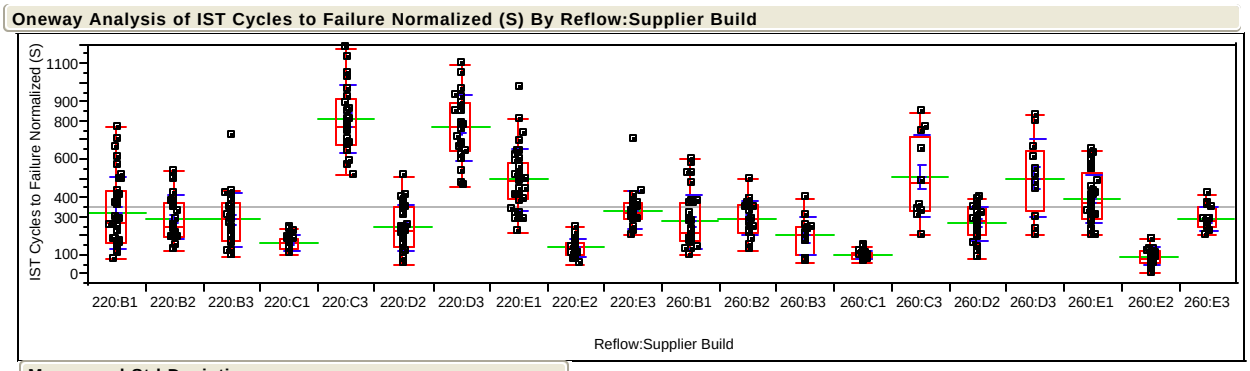
Figure 10 – Normalized IST Performance by Cumulative Supplier Builds and Reflow Temperature

The greatest variation in IST cycle performance seen in this study comparing Sn/Pb and Pb-free assembly processing was the difference between suppliers and the difference between multiple builds at the same supplier. There was a wide range of differences in the average IST cycle performance by supplier vs. reflow temperature, as well as a large spread in the IST cycle performance within a supplier at a particular assembly reflow temperature.

Table 5 – Comparison of IST Cycle Performance of Cumulative Supplier Builds vs Reflow Profile

	Reflow Temperature		
Supplier	220C	260C	220-260 Delta
B	303	268	113%
C	531	276	192%
D	507	350	145%
E	352	280	126%
G	163	139	118%
H	481	409	117%
Max Delta between Suppliers @ 260C			295%

Figure 11 shows the IST cycle performance by individual supplier build and reflow temperature. The average performance and the spread of the data varied greatly from build to build at the same supplier. This data shows that the lot-to-lot difference or supplier-to-supplier difference can overwhelm any performance shift due to via size, board thickness, or material. The large shifts indicate that printed circuit board fabricator controlled parameters will dominate and skew test results if not properly controlled. These parameters include: drilled hole quality, plating quality, plating thickness, and material quality (e.g. over-cured or under-cured). As these variables can have a significant effect on the via reliability, it is essential that proper large sample testing be performed across industry and build lots to assess impact of reflow temperatures on IST via cycles to failure performance. In this study, efforts were made to get consistent plating thickness on all samples by specifying IPC class 2 copper plating thickness, but the thickness was found to still vary as much as 30% from supplier-to-supplier and via size-to-via size.



Means and Std Deviations

Level	Number	Mean	Std Dev	Std Err Mean	Lower 95%	Upper 95%
220:B1	34	322.141	186.570	31.996	257.04	387.24
220:B2	24	294.786	113.715	23.212	246.77	342.80
220:B3	24	285.038	141.060	28.794	225.47	344.60
220:C1	18	164.727	36.910	8.700	146.37	183.08
220:C3	24	805.261	174.355	35.590	731.64	878.88
220:D2	24	246.845	119.055	24.302	196.57	297.12
220:D3	24	766.299	170.736	34.851	694.20	838.39
220:E1	35	491.915	159.954	27.037	436.97	546.86
220:E2	21	137.631	44.943	9.807	117.17	158.09
220:E3	24	336.394	94.739	19.338	296.39	376.40
260:B1	29	277.175	144.776	26.884	222.11	332.25
260:B2	21	292.605	90.479	19.744	251.42	333.79
260:B3	12	200.729	98.978	28.573	137.84	263.62
260:C1	16	99.994	24.387	6.097	87.00	112.99
260:C3	12	511.116	211.824	61.148	376.53	645.70
260:D2	22	265.432	87.546	18.665	226.62	304.25
260:D3	12	504.732	200.967	58.014	377.04	632.42
260:E1	36	396.913	129.342	21.557	353.15	440.68
260:E2	23	89.576	48.458	10.104	68.62	110.53
260:E3	12	292.549	64.515	18.624	251.56	333.54

Figure 11 – Normalized IST Performance by Individual Supplier Build and Reflow Temperature

Table 6 highlights the worst case deltas within suppliers and across suppliers for IST performance by reflow temperature. The max deltas are as high as or higher than most of the design impacts vs. assembly reflow process temperature change.

Table 6 – Comparison of IST Cycle Performance by Individual Supplier Builds vs. Reflow Temperature

	Reflow Temperature		
Supplier	220C	260C	220-260 Max Delta
B1	322	277	
B2	295	293	
B3	285	201	160%
C1	165	100	
C3	805	511	805%
D2	247	265	
D3	766	505	289%
E1	492	397	
E2	138	90	
E3	336	293	549%
Max Delta All Builds @ 260C			571%

The probability plot in Figure 12 illustrates again the supplier variation between multiple build lots. In Figure 12, the C3 build lot at the 260C assembly reflow condition showed higher cycles to failure results than the 220C assembly reflow condition of another build (C1) from the same supplier with the same material, board thickness, and via size. The implication of this variation is to reduce the overall probability that shifting to an alternative material to will improve the aggregate product performance in terms of IST via cycles to failure. Another implication is that monitoring and control of a printed circuit board's IST via cycles to failure performance is required on a continual basis to insure ongoing acceptability.

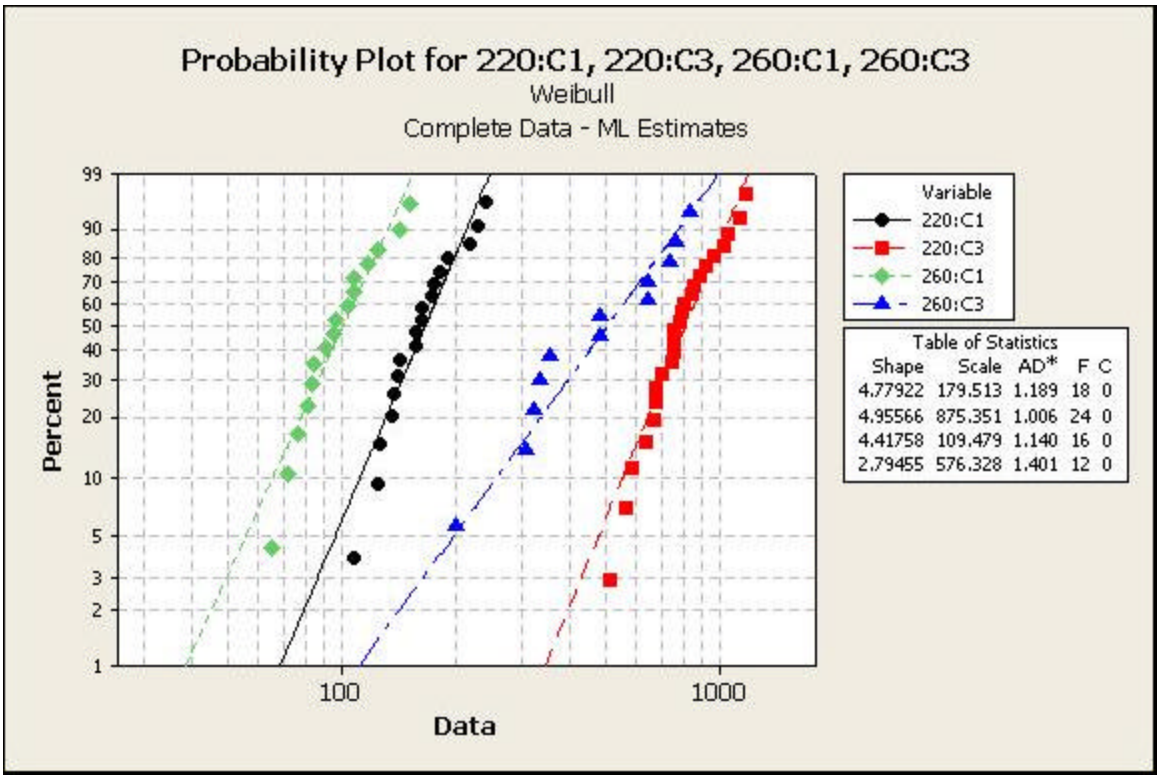


Figure 12 – Probability Plot of IST Cycle Performance of Supplier C Builds vs. Reflow Temperature

Summary
Drill size, material choice, and board thickness are all design variables that can have an impact on IST via cycles to failure test performance of the board. For a given supplier build lot, drill size and material choice have consistent IST via cycle performance differences between Sn/Pb assembly and Pb-free assembly. The IST via cycle to failure performance differences increase as board thickness increases when the assembly reflow temperature is increased. All these design influences can be significantly impacted by supplier variation if not controlled. The common solution to meet IST via cycles to failure criteria when moving to Pb-free assembly is to switch to a more thermally compatible material for the design. This move may result in little or no improvement in IST cycles to failure if the supplier is unfamiliar with the new material and has transition problems with process adjustments. Some materials, even though they are listed as higher temperature materials / higher Tg materials, are unsuited for Pb-free processing by exhibiting susceptibility to delamination/blistering at these process conditions. The primary solution is to know your supply base's variation over time with regards to IST via cycles to failure and how it is impacted by Pb-free process effects. This requires ongoing monitoring and testing because of variation between build lots and between multiple suppliers. Depending on the extent of the existing variation of your product, a design modification or material change may not be required to achieve reliable product with Pb-free assembly processes.

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