

# Low Cost Lead Free Solution Evaluation for Electronic Consumer Applications

Krishna Darbha and Nicoletta Sangalli  
Microsoft Corporation  
Redmond, WA

## Abstract

Lead products are no longer an option if you want to export to the EU market. RoHS regulations requiring the manufacture of lead-free electronic products by July 2006 are pushing the industry to evaluate and find lead free solutions soon. There are several important issues in undertaking a transition to lead free, including: 1) finding PCB materials and plating finishes that can withstand the high reflow and wave temperatures of lead free alloys, 2) selecting lead free alloys that have similar or better quality and reliability characteristics than SnPb, 3) assessing whether the lead-free components can withstand high reflow temperatures, 4) finding a cost effective solution, and 5) understanding and solving the challenges of the lead-free process on PCBs, components and solder joint quality. In this paper we address these issues by evaluating a) two PCB materials - FR1 and FR4, b) PCB plating finish – OSP and Ni/Au, c) lead-free alloy Sn 3.5Ag0.5Cu (SAC) and 58Bi42Sn, and d) the number of reflows (single -sided vs. double-sided). We evaluated 58Bi42Sn eutectic alloy as a solution for those components that cannot withstand the high temperature process of SAC alloy. Our goal is to determine a cost effective solution for a low temperature application. Different reliability tests, warpage measurements, and cross sections were used to evaluate each configuration.

## Introduction

In this paper we consider two main lead free solder pastes for reflow, the most commonly used being SnAgCu (SAC) which has a higher melting point than the Tin-lead eutectic solder, and 58Bi42Sn which has a lower melting point than the tin-lead eutectic solder. The main reason to study the use of a low melting point solder is that certain components that have a package with low T<sub>g</sub> (Glass Transition Temperature) resin cannot withstand 240°C or higher temperature during reflow, therefore SAC cannot be used. In addition, with a low melting point solder, it is possible to continue to use FR1 as used in conventional tin-lead process. We also consider two different PCB materials FR1 and FR4 with two different coating materials, OSP (organic solderability protectants) and NiAu. We want to evaluate whether FR1 can be used with SAC, and if the OSP coating is more or less reliable than NiAu for a commercial application where the maximum temperature does not go above 75°C including shipping conditions.

## Materials and Configurations Studied

In an effort to establish the lowest cost and most reliable configuration for a lead-free PCB assembly in a consumer application, a fractional factorial experiment was conducted on 4 design variables:

- lead-free solder (58Bi42Sn and Sn 3.0Ag0.5Cu),
- PCB materials (FR1 and FR4),
- numbers of reflows (single -sided vs. double -sided) and
- PCB plating finish (NiAu and OSP).

The choice of low temperature lead-free solder was primarily considered due to the low cost materials of FR1 and OSP. The single-sided vs. double -sided reflow was studied to assess the quality of coating as a function of number of reflows. Table 1 indicates the design variables analyzed in this study.

**Table 1 - Test Configurations**

Test Configuration	Alloy	PCB material	PCB finish	# of PCB reflows
1	SnBi	FR1	OSP -Cu	Single -sided
2	SAC	FR1	NiAu	Single -sided
3	SAC	FR1	OSP -Cu	Double-sided
4	SnBi	FR1	OSP -Cu	Double-sided
5	SAC	FR1	NiAu	Double-sided
6	SnBi	FR4	OSP -Cu	Double-sided
7	SAC	FR4	NiAu	Double-sided

Solder alloy Evaluation: 58Bi42Sn 58Bi42Sn was studied as a low melting point (138°C) solder, as less thermal stress is applied to the assembly during reflow and as some components cannot withstand the more common lead free SnAgCu (SAC) reflow temperature. Finally it was considered because of the positive results from a reliability perspective collected in the last 30 years<sup>1,2,3</sup>. Some Japanese companies use this solder in their commercial applications today. Temperature cycling results performed by Boeing with 58Bi42Sn, on LCC20 at high temperature (-40+125 °C), exhibited fewer failures than with PbSn3. The main concern today with using this solder is during the lead free transition where lead and lead free components can coexist. If lead (Pb) is present with SnBi the concern is the formation of ternary phase 16Sn32Pb52Bi with a low melting point temperature of 96 °C. A study done in Boeing demonstrated that the solder joint of a LCC20 will degrade if Pb is present in 58Bi42Sn solder joints<sup>3</sup>. The degradation during temperature cycling was significant in comparison with a situation of no Pb, but the upper temperature used was 125°C which is above the ternary phase melting point (96°C), so a large reduction in solder joint durability is expected. The first failure was detected at 500 cycles. For a consumer application where the maximum temperature is around 75°C, including shipping, the risk of solder joint reliability with Pb contamination seems to be low. We performed push/pull tests on SOIC packages and leadless packages with a SnPb coating on the leads/terminations with 58Bi42Sn solder joints before and after temperature cycling as per Table 4 conditions. The test results between SnPb and pure Sn coating material were similar.

A more realistic temperature for this application was used in this study in an accelerated test (-40+85 °C) to avoid being close to the melting point where a “crack healing” mechanism can change the failure mechanism of the accelerated temperature cycling. To gain confidence in using the SnBi solder, different PCB configurations with different components were assembled and subjected to reliability tests (Table 3) from different assembly lines, different reflow equipments and different times to see if the process variation had any effect on solder joint quality and reliability. More than 300 PCBA samples were used (with about 18 PCB configurations) for each test (Table 3). Components ranged from 0402 resistors to 3212 capacitors, 10x10mm QFP (quad flat package), 8x8mm LGA (land grid array), and SMT 0603 LED (surface mount technology, light emitting diodes). Functional tests were performed before and after the tests, and many cross sections were performed after temperature cycling and drop shock (from 10 to 30 cross sections for each PCB configurations). The lead-free solder design variable was studied in more detail compared to the other design variables chosen in this study as there has been a significant push in adopting SAC as a lead-free solder candidate to replace eutectic Sn-Pb across applications. Our intent is to demonstrate that the use of solder is application specific.

PCB Material: FR1 and FR4 Two different PCB materials were compared in this study to see how they withstand the high melting point of SAC. On a bare and balanced PCB, the effect of temperature on PCB warpage is negligible. However, with surface mount components on the PCB and copper traces, the board warpage, caused by a thermal expansion mismatch between the surface mount components and the PCB, is not negligible. Board warpage can degrade the reliability of the PCB assembly, by weakening the solder joints, cracking via, cracking components, or by causing misalignment of the optical axis in an optical application.

There are 5 primary causes for board warpage for a given maximum temperature and rate of change:

1. CTE mismatch between surface-mount component and PCB (design issue)
2. Unbalanced PCB: asymmetric PCB about the neutral axis like uneven number of copper layers about the neutral axis (design issue)
3. Geometric features like large cutouts in the PCB reducing the stiffness of the PCBs, thin PCBs etc. (design issue)
4. Low flexural modulus PCBs (design issue)
5. Uneven temperatures on the top and bottom of the PCB (process issue)

A combination of the above reasons could cause excessive board warpage thus compromising the reliability of the PCB assembly.

For this study, a combination of (1), (3) and (4) are evaluated via the choice of the test vehicle and evaluation of the FR1 vs. FR4 materials. With a well controlled process, the temperatures are maintained uniform inside the oven to within +/- 30C and hence this parameter was not a critical issue in this study.

This study looked at 2 different board materials: FR1, and FR4. FR-1 is a paper phenolic based material while the FR4 is an epoxy woven glass based material. FR-1 with a lower flexural modulus and higher coefficient of thermal expansion will have a relatively higher warpage compared to FR4 (See Table 2). Nearly 200 samples were made for each PCB type and the reliability tests were conducted as per Table 3.

**Table 2 - Properties of PCB Materials**

Properties	FR1	FR4
Flexural modulus (Mpa)	8275	18620
Coefficient of thermal expansion (ppm/°C)	26	13
Glass transition temperature (°C)	130°C	140°C

**Table 3 - Test Conditions, Samples Size and Results**

58Bi42Sn & SnPb/ Comparison	Temperature Cycling	Temperature Humidity Bias	Drop s hock	Push/Pull	Cross Section
Tests	-40 to 85°C, 200 cycles, more than 300 samples to evaluate SnBi reliability - 40°C to 85°C for 500 cycles, more than 200 samples to evaluate PCB, plating finish and SAC/SnBi reliability	65°C 90% RH, 300 hours, more than 300 samples to evaluate SnBi reliability 85°C, 85%RH for 500 hours, more than 200 samples to evaluate PCB, plating finish and SAC/SnBi reliability	Several drop iterations at 42 inc, more than 300 samples	Compare lead with lead free solder joints for BGA, Gall-wing lead, resistors, capacitors	Cross section after TC and shock, compare lead and lead free, and effect of plating finish
Results	PASS no cracks initiation in the solder. Surface crack with SAC were seen at time zero but they do not seem to propagate. No cracks were seen with 58Bi42Sn	PASS. No dendrites growth or electrical overstress	PASS no cracks in the bulk of the solder. Surface crack with SAC were seen at time zero but they do not seem to propagate. No cracks were seen with 58Bi42Sn	PASS Similar to Lead solder, variation of +/- 15%	Bigger voids observed with SAC, they can be reduced with process setting No cold solder joints

**PCB Finish: NiAu and OSP**

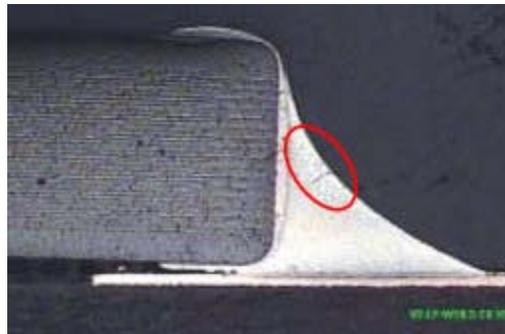
The nature and quality of the surface finish on the pad determines how well the solder bonds to the pad via the intermetallic layer. The surface finish must foster the optimum wetting and intermetallic formation under multiple thermal excursions and higher soldering temperatures for lead-free solders. Electrolytic nickel/immersion gold is a metal finish on PWB that is widely adopted in the industry due to high reliability. Alternatively, low cost organic solderability preservatives (OSPs) 6 have also been used in the PCB industry as a replacement. OSPs are preferable as they are environmentally friendly, provide a coplanar surface, require low equipment maintenance 4 and they are low cost. Conventional OSPs used in the Sn-Pb solder applications have a decomposition temperature around 240-250°C, which is the typical peak temperature of SAC solders. High temperature OSPs are currently being developed for use in lead-free applications and are regaining a leadership role as a plating finish. One such material was used in this study. The exact composition of the material was not disclosed by the manufacturer and hence an experimental study was conducted in this paper. However, whether a high temperature OSP surface finish can withstand multiple thermal cycles and high temperature reflows and wave solder with the use of lead-free solders, and whether solder wettability and shelf life are acceptable, are concerns that need to be addressed. The ability to quantify this variance in solder joint strength or reliability in an actual product before it is deployed in the field has potentially significant cost benefits.

In this study, the impact of OSP on lead-free solderability was assessed via single -sided and double-sided reflows. Nearly 200 samples were made for each configuration and the reliability tests were conducted as per Table 3.

### Results and Discussion

Examples of the test vehicles used in this study are shown in Figures 5 and 6. This test board was 1.6mm thick and was populated with numerous SMT components ranging from 0603 capacitors to an LGA package (8x8mm) and through-hole components including resistors and crystals.

Reliability Tests on 58Bi42Sn and SnAgCu Environmental and mechanical stress tests were conducted to evaluate the reliability of SnBi and SAC solder joints. The reliability tests used to evaluate these configurations were accelerated tests that correlate with an office-home user application. Temperature cycling was used to detect a crack initiation in the typical failure site of each component-solder joint, and to verify if cracks on the surface of the solder joint (Figure 1) seen in SAC after wave solder propagate inside the solder bulk. Temperature humidity bias was used to verify that dendrites, which can cause electrical shorts, will not grow between solder joints. Multiple drop shock tests were used to see if the solder joints were brittle. The push-pull test was used to compare the strength of the lead free and the lead solder joints, and cross sections were used to verify the solder joint quality, voids, intermetallic, crack initiation and propagation, and component overstress. Reliability results were all positive and were equivalent to results found with SnPb.



**Figure 1 - Capacitor Soldered through Wave Soldering with SAC**  
(Crack on the solder surface at time zero. No solder underneath the pad due to excessive glue)

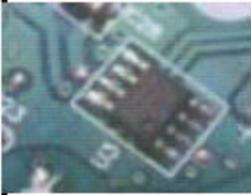
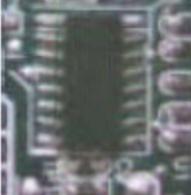
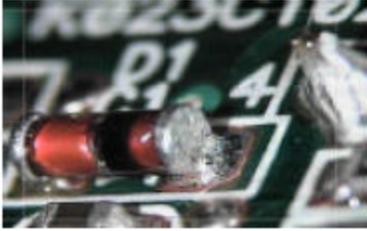
### Reliability Tests on 58Bi42Sn with Pb Coating

We analyzed the impact of lead coating on 58Bi42Sn solder joint reliability by comparing the Push/Pull test of leadless components and leaded components with pure Sn coating and SnPb coating (see Table 4). The test results between pure Sn and SnPb with SAC, 58Bi42Sn and SnPb solder were very similar. Some push tests were performed after temperature cycling at the conditions used in Table 3 and compared with no temperature cycling with SnPb solder, also these results look similar or better with 58Bi42Sn solder and Pb coating. The presence of Pb on coating terminations seems to not affect the solder joint strength if the temperature is below 96°C, which is the melting point of the possible ternary phase 16Sn32Pb52Bi that can be formed with SnBi and Pb.

**Table 4 - Push/Pull Test Comparison between 58Bi42Sn and SnPb Solder and Different Coatings**

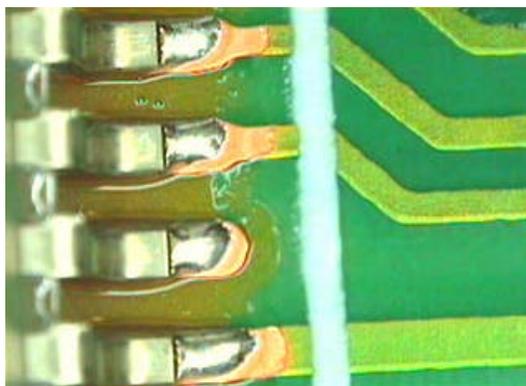
Solder	Coating	Process	Component	Pull-test (N)	Push test(N)	After Temp Cycling
SAC	Sn	W/S*	U1	24.38		No
SAC	Sn	W/S*	U1	25.13		No
SAC	Sn	W/S*	U1	26.03		No
Bi58	SnPb	Reflow	U3	23.8		No
Bi58	SnPb	Reflow	U3	22.48		No
Bi58	SnPb	Reflow	U3	20.54		No
Bi58	SnPb	Reflow	U3	22.87		No
Bi58	SnPb	Reflow	U3	21.4		No
Bi58	SnPb	Reflow	U3	21.92		No
Bi58	SnPb	Reflow	D1		39.06	Yes
Bi58	SnPb	Reflow	D1		36.07	Yes
Bi58	SnPb	Reflow	D1		46.61	Yes
SnPb	SnPb	Reflow	D1		46.69	Yes
SnPb	SnPb	Reflow	D1		42.05	No
SnPb	SnPb	Reflow	D1		33.43	No
SnPb	SnPb	Reflow	D1		34.61	No

W/S\*: solder joints in W/S were bigger than in reflow

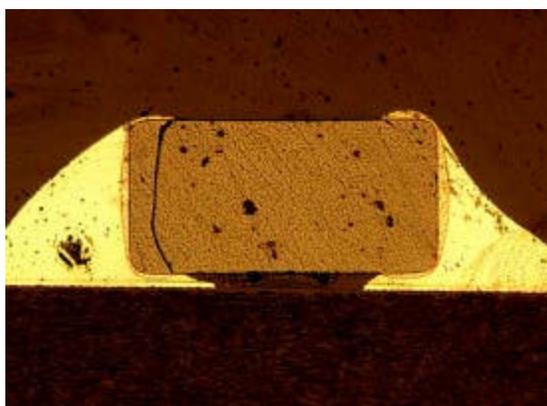
 U3	 U1	 D1
--	--	---

Process: 58Bi42Sn and SnAgCu (SAC) From a process point of view there were no major concerns with 58Bi42Sn. The printing process and the reflow dppm were not very different from those found with the SnPb solder. A few tweaks in the stencil aperture had to be performed to optimize the solder amount on the pads (Figure 2). No more tombstones or bridges were seen than with the lead solder. The visual inspection shows the solder surfaces were not as bright as the lead solder but were not as dull as the SAC (Sn3.0Ag0.5Cu) alloy used. Because of the low melting point the reflow profile is very mild on the PCBA (Figure 8) allowing to use FR1 as before, and component like SMT LED and optical packages with low Tg could be used with no reliability issues. The dppm was very good and no major concerns were seen. Instead more issues were seen with SAC in the wave solder process. Bridges between components was one major issue. The design for manufacturing is more critical than ever before in order to have a good dppm. Another issue was the size of the voids. This issue requires a lot of tuning in the process, as the voids can be more and/or bigger than with eutectic SnPb, but they can be optimized. The more critical issue was the cracking of multilayer ceramic capacitor soldered through wave solder with SAC (see Figures 3 and 4).

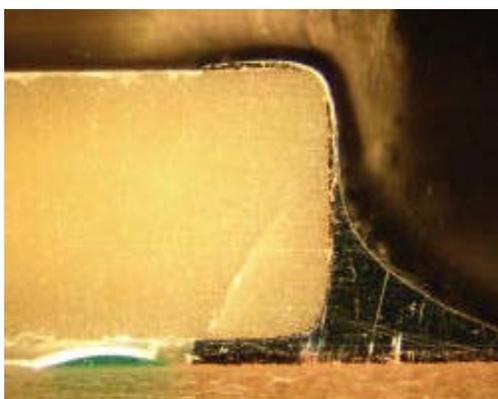
The cooling rate was identified as a critical parameter to solve this problem.



**Figure 2 - Gull Wing Leads with 58Bi42Sn Solder not Covering Completely the Pad, Stencil Redesign can Solve the Problem**



**Figure 3 - Cracked Capacitor after Wave Solder with SAC (Sn3.5Ag0.5Cu)**



**Figure 4 – Cracked Capacitor after Wave Solder with SAC (Sn3.5Ag0.5Cu)**

#### ***Effect of PCB Design and Material***

The 2 test vehicles (shown in Figures 5 and 6) were analyzed to assess the effect of geometry on warpage with all other parameters remaining constant. TV-1 had a big cutout in the front of the PCB resulting in thin finger-like structures while TV-2 was a plain PCB with no thin features. The PCBs were subjected to a lead-free process temperature with reflow profiles for 58BiSn42 (max temperature of 180 °C) and SAC (max temperature of 250°C) as shown in Figures 7 and 8. For the same PCB geometry, the effect of the reflow temperature was smaller compared to the effect of the flexural modulus and CTE mismatch for the warpage differences between FR-1 and FR-4.

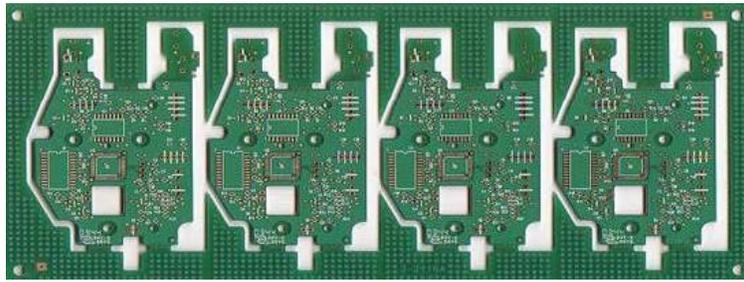


Figure 5: Test Vehicle 1 (TV-1)



Figure 6: Test Vehicle 2 (TV-2)

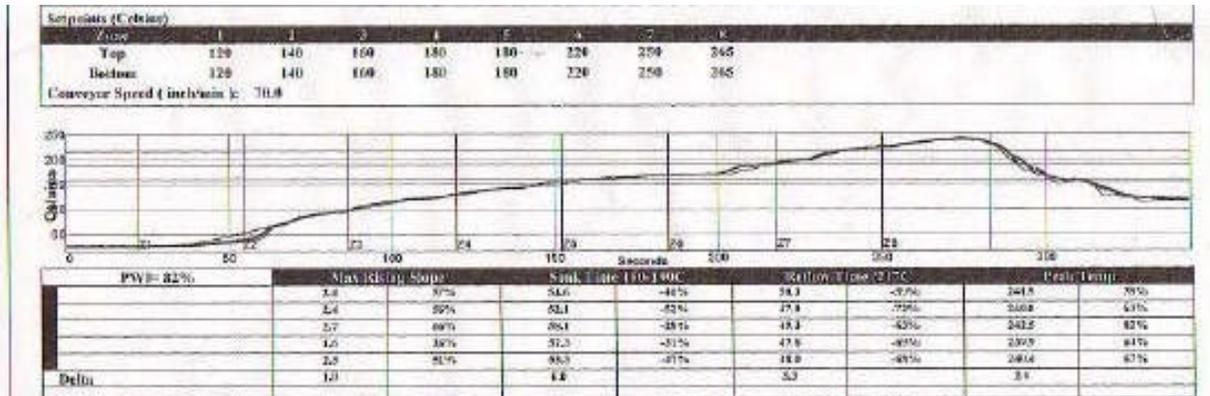


Figure 7 - SAC Reflow Profile

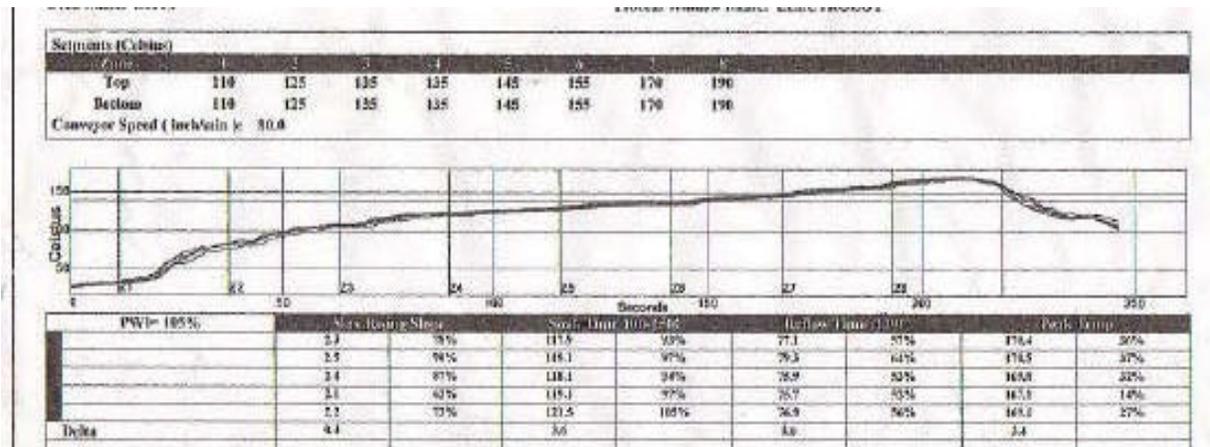
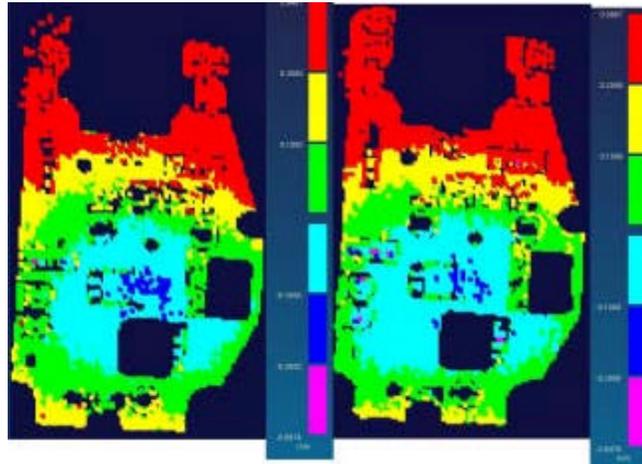


Figure 8 - SnBi Reflow Profile

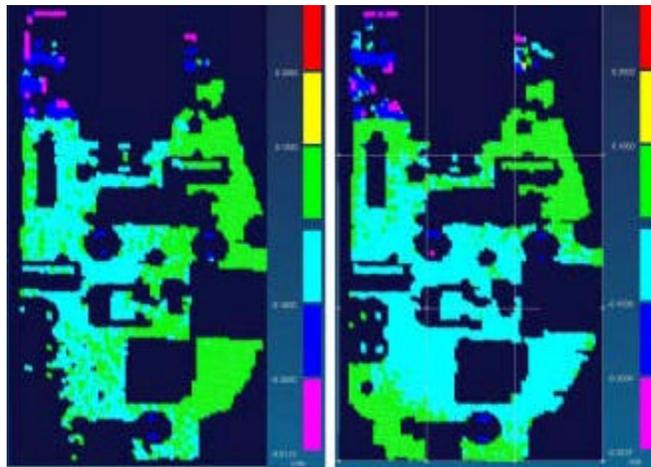
The warpage of the PCBA was studied to compare FR1 with FR4 after SAC reflow. The numbers in Table 5 are the ratio of the maximum out-of-plane displacement to the span of the PCB. For TV-1, due to the nature of PCB geometry with thin fingers protruding out due to the large cut-out in the PCB, the PCB warpage was nearly 2 times higher for FR-1 than FR-4. For TV-2, the PCB had no thin and un-supported structures and had a considerably lower warpage. Figures 9 and 10 shows TV-1 with SAC reflow. The highest warpage as expected is found in the bending of the thin and unsupported structures. The FR-1 PCB exhibited nearly 2 times the warpage of that of FR -4. However, this board warpage data was still within the specifications for the specific application.

**Table 5 - Maximum Coplanarity**

	FR-1	FR-4
TV-1	2%	1%
TV-2	1%	

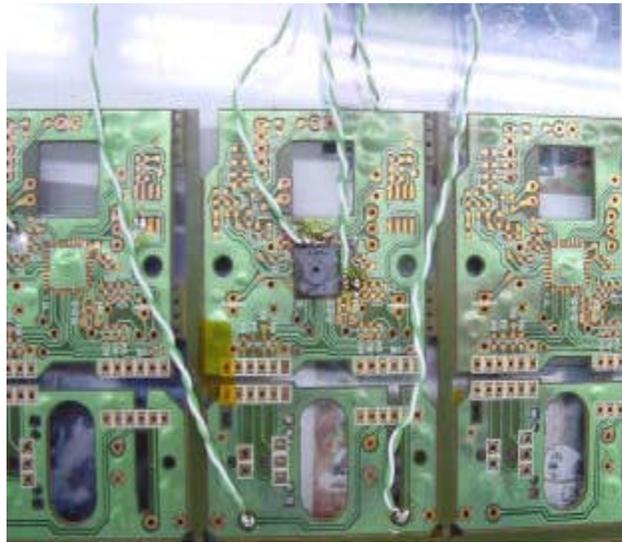


**Figure 9 - FR1 PCB Warpage**



**Figure 10 – FR4 PCB Warpage**

No blistering of FR1 was observed up to a maximum reflow temperature of 248°C. FR1 was deemed possible for use with SAC solder, but there is a risk that in full production, and with PCB material variation from different suppliers, this could become an issue. Beyond 250°C, FR1 exhibited blistering and delamination of the PCB as shown in Figure 11.



**Figure 11 – Blistering and Delamination of FR1 beyond 250° C**

Since every board configuration is different, there is no standard reflow profile that will fit all assemblies. An assessment of the severity of a SAC reflow profile to the PCB assembly has to be conducted to determine whether the respective assembly, PCB material and reflow profile would work for that specific configuration.

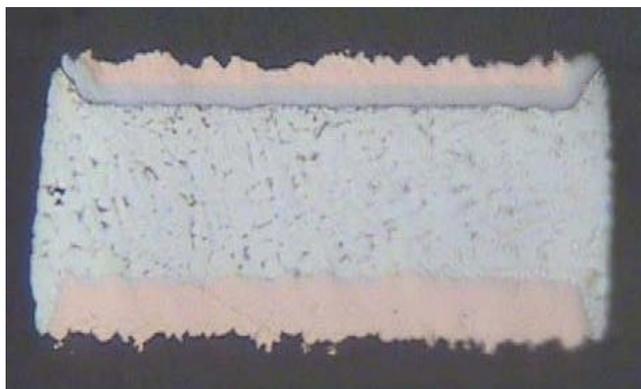
For the application of interest in this study, the FR1 board material is the optimal choice due to low cost and the warpage being well within the specifications.

***Effect of Lead-Free Process on Plating finish***

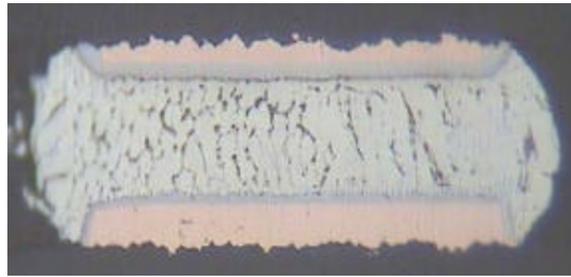
Detailed cross-sectional studies (Figure 12-14) were conducted to study the interfaces between the solder joint and the pad on the PCB with OSP and Ni-Au plating finishes. Select solder joint cross-sections are shown below. A solder push-pull test, as well as high temperature and humidity (TH) and thermal cycling (TC) tests were conducted to evaluate the integrity of the solder joint with the plating finish (as per configurations in Table 1).

For the choice of OSP in this study, the push-pull test of SAC and 58Bi42Sn solder joints were comparable to Sn-Pb for single-sided and double-sided reflow conditions. The failure mode in the push-pull test was the removal of the component solder joint from the pads for all the solder candidates and board materials. No failures were observed in the solder joints for either plating finishes with TH and TC tests, and the cross section confirmed the integrity of the solder joints.

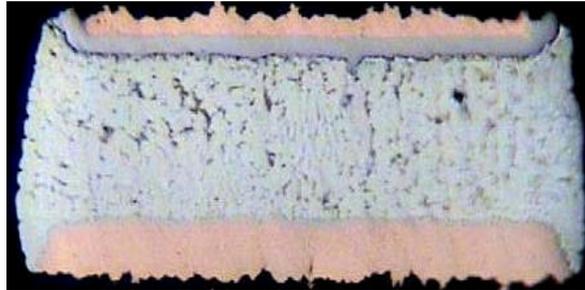
The OSP plating finish was proved durable in a double-sided reflow condition for both solder alloys.



**Figure 12 – SAC-OSP – FRI – Double-Sided Reflow**



**Figure 13 – SAC – NiAu – FR4 – Double-Sided Reflow**



**Figure 14 – 58Bi42Sn – OSP – FRI Single-Sided Reflow**

## Conclusions

A study was conducted to assess the optimal choice of materials for a reliable and cost effective lead-free assembly. Variables studied include choice of solder material (SnBi vs SnAgCu), choice of board material (FR1 vs FR4), choice of plating finish (OSP vs NiAu) and number of reflows. Based on the variables studied, for a consumer application, the optimal choice recommended is FR1, OSP, and 58Bi42Sn for reflow. The low melting point lead-free solder, 58Bi42Sn, revealed excellent solder durability comparable to the traditional Sn-Pb and SAC for a consumer application whose maximum temperature is limited to a maximum of 75°C. In addition the lower reflow temperature makes this an attractive candidate compared to the popular SnAgCu solder allowing one to use FR1 instead of FR4. The optimal configuration was reliable after double-sided surface mount reflow followed by wave-solder with SAC. This configuration has the advantage of being a low cost option and has a reflow temperature lower than 63Sn37Pb solder. SnAgCu also had a similar performance compared to SnBi, however the PCB started exhibiting blistering and delamination above 250°C reflow temperature. Moreover, the board geometry starts becoming sensitive to warpage with higher reflow temperatures. More study has to be conducted to prove that this is not an issue for the intended application.

## Acknowledgements

The authors would like to thank Kumar Upadhyayula and Pavan Davuluri for the innumerable discussions on lead-free study. In addition, the authors would like to acknowledge the support of Kurt Wrisley and Cesar de Leon in providing build support for the test configurations.

## References

1. Raeder C.H., Felton, Knorr L.E, Schmeelk G.B, and Lee D., “Microstructural Evolution and Mechanical Properties of Sn-Bi Based Solders”, pp119-127,IEEE/CHMT Int’l Electronics Manufacturing Technology Symposium. 1993
2. Mei Z., Hua F., Glazer J. “Low Temperature Soldering”. IEEE/CPMT Int’l Electronics Manufacturing Technology Symposium. 1997
3. Woodrow T., “The Effect of Trace Amount of Lead on the Reliability of Six Lead-free Solders”, Proceedings of the 3rd International Conference on Lead-Free Components and Assemblies, San Jose, CA, April 23-24, 2003 (on CD).
4. Saeki, K., and Carano, M., “Next generation Organic Solderability Preservatives (OSP) for lead-free soldering and mixed metal finish PWBs and BGA substrates”, pp. 406-411, IPC/JEDEC Fourth International Conference on Lead-free Electronic Assemblies and Components, Oct 21-22, 2003, Frankfurt, Germany.
5. Yamada, S., “A Mechanism for Board Warpage by Thermal Expansion of Surface Mounted Connector”, IEEE Transactions On Components, Hybrids, And Manufacturing Technology, pp. 508-512, Vol. CHMT-9, NO. 4, DECEMBER 1986
6. Davitt, E., Stam, F., and Baret, J., “The Effect of Power Cycling on the Reliability of Lead-Free Surface Mount Assemblies”, IEEE Transactions On Components, Hybrids, And Manufacturing Technology, pp. 241-249, VOL. 24, NO. 2, JUNE 2001