

Novel Substrate for Use as Embedded Capacitance: An Easy to Process Higher Dk Material

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Abstract

We have previously published our work on developing thin substrates for use as embedded capacitor layers. Both unfilled and filled materials were characterized in regards to performance, reliability and manufacturability. It was demonstrated that higher capacitance density came at the expense of ease of processing.¹ A new substrate was developed to address this issue.

As previously shown, high speed digital circuits benefit primarily from the capacitive layers being as thin as possible. For mobile electronics, however, they want the highest capacitance density so they can remove the most discrete capacitors. With both these markets in mind, a thin substrate with higher Dk than unfilled systems was developed. A major design objective was to be able to etch both sides of the substrate at the same time (like traditional power/ground layers).

We will discuss the experiences of PWB shops in processing the material and review the results of the various reliability studies. Also, test vehicles have been processed for testing at high frequencies to compare against the other capacitive materials. It will be demonstrated that this new substrate has excellent electrical properties (such as a DK of 10 and the ability to pass 500 volt High-Pot) while being able to be readily manufactured using typical inner-layer processing.

In addition we have developed a method, which utilizes our highest Dk material, which is compatible with HDI processing. This process can be used to embed capacitance within an organic chip package.

Introduction

The development of Embedded Capacitor technology has been driven by the need to save board area and/or reduce board size, increase functionality, lower costs and improve electrical performance. Current standard capacitive material used in the high end computing industry is mainly the 50 μ m (2mil) dielectric thickness material, mostly utilized for telecom and networking applications². For this particular high end PWB application, embedded capacitor technology has been utilized to realize the electrical performance they need to distribute capacitance, enhance signal integrity, reduce impedance at high frequency and dampen noise.

A number of papers have been published regarding development of materials for embedded capacitors and the advantages of incorporating embedded capacitors in PWBs. From the electrical performance standpoint, more and more demand of thinner capacitor material, as low as 8 micron, is arising as the signal frequency increases for these high end computing systems.³

Another field that has been aggressively looking to incorporate embedded capacitor technology is the modules used in cell phones and laptop PCs. This is mainly driven by the shrinking of the size of the boards, by converting from LTCC, and reducing the cost at the same time. For these module applications, since the size of module is limited, embedded capacitor material that has relative high capacitance value is required.

In this paper, newly developed embedded capacitance materials are being introduced and the incorporation of the material into PWBs is discussed.

Embedded Capacitance Material Properties

The Embedded capacitance materials are constructed from two copper foils with a dielectric polymer film layer in between (Laminate type) or one copper foil layer and dielectric polymer layer coated on one side (Resin Coated Foil –“RCF” type). Figure 1 describes the schematic construction of both material types.

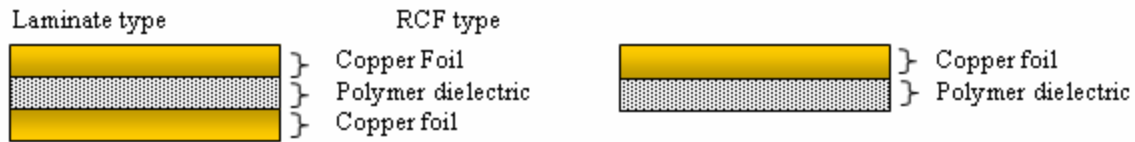


Figure 1 - Schematic Construction of Embedded Capacitance Material

Table 1 lists the properties of the various materials. The first four products are unfilled laminate type materials, the next two are filled laminate type materials and the last is the filled RCF type product.

Laminate type of capacitive material is more suitable for use as power distribution layers in high layer count boards. It can be “designed in” as power and ground planes. One of the benefits of the laminate type is that it can be pre-tested to hi-pot (high potential testing) prior to shipment and processing.

For laminate type, dielectric thicknesses of 8, 12, 16 and 24 μm are available. Standard material has Dk of 4.4 at 1MHz. For higher capacitance material, Dk of 30 is available for 16-micron material as BC16T. The new intermediate product with Dk of 10 is available as 12-micron material as BC12TM. Standard copper thickness is 35 μm (1oz) since most of the applications for these materials are power distribution layers where it carries a lot of current. Thicker and thinner copper can be used based on current carrying requirements.

RCF type is more suitable for use as singular (discrete) capacitors in module application. The advantage of RCF type is that it can be processed through the standard HDI build-up process and be able to form small individual capacitors.

Table 1 - Characteristic of Embedded Capacitance Material

Properties	Method							
		BC24	BC16	BC12	BC8	BC12T M	BC16T	BC16T (RCF)
Dielectric thickness, μm	Nominal	24	16	12	8	12	16	16
Dielectric type	-	Polyme r film	Polyme r film	Polyme r film	Polyme r film	Filler/ film	Filler/ Polyme r	Filler/ Polyme r
Cp @1MHz (pF/cm ²)	IPC TM- 650 2.5.5.3	155	250	300	480	700	1700	1700
Dk @1MHz	IPC TM- 650 2.5.5.3	4.4	4.4	4.4	4.4	10	30	30
Df @1MHz	IPC TM- 650 2.5.5.3	0.015	0.015	0.015	0.015	0.019	0.019	0.019
Peel Strength (kN/cm)	IPC TM- 650 2.4.9	>1.0	>1.0	>1.0	>1.0	>0.7	>0.7	>0.7
Migration, (hrs), 85C/85%RH/DC35V	Mitsui method	>1000	>1000	>1000	TBD	TBD	>1000	>1000
Flammability/Temp. Rating	UL- 94/UL74 6	V0 130C	V0 130C	V0 130C	Pendin g	Pendin g	Pendin g	Pendin g
PWB processing	-	Both side etch	Both side etch	Both side etch	Both side etch	Both side etch	Sequen tial	Build up

Processing of Embedded Capacitance Material

Laminate Type Capacitor Material

Laminate type capacitor material is suitable for forming distributed capacitance for power and ground planes. PWB fabrication step of laminate type capacitor material is basically same as that of processing a conventional inner layer of power and ground planes. Since the material is thin, in some steps special consideration is required. Processing examples are described for each step as follows.

Pattern Formation

The material is processed through the following processes.

1. Chemical Cleaning (may include micro-etching)
2. Dry Film lamination
3. Image transfer (Expose)
4. Pattern etching –Develop, Etch and Strip Resist (Dual sides, except for BC16T)
5. Inspections and Hi-Pot Testing
6. Black or alternative oxide

Unfilled laminate type material can be processed in a single pass due to the tough and flexural dielectric property. For THE 16 MICRON, since the dielectric of this material is loaded with High Dk ceramic fillers, sequential lamination process is required. This requires going through the above process for one side only, then laminating prepreg and copper to that side. This sub-assembly is then processed through the above operations again.

In order to avoid this sequential operation, yet still have better capacitance density than the unfilled materials, a new product was developed which is designated BC12™. It is tough and flexible like the unfilled systems but has a capacitance density 50% higher than the best unfilled material. It has been processed through several PWB facilities with similar results to the unfilled systems.

Although, processing thin capacitance material can be challenging and may need modifications/adjustment to the process, the material is capable of processing through the conventional PWB manufacturing steps.

One of the important factors of processing these thin laminates is the capability of horizontal processing equipment. Figure 2 shows the comparison between standard transport system and ultra-thin compatible system provided from Schmid system Inc. The distance between squeegee rollers and transport disk rollers are minimized. Guiding rollers and clips are added to prevent thin laminate from jamming.

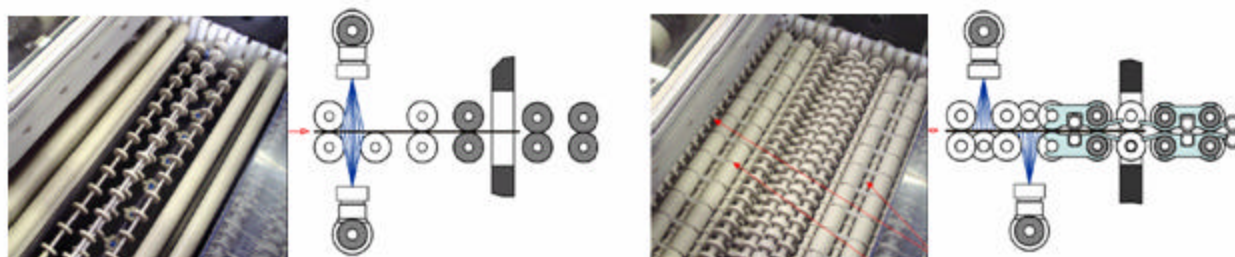


Figure 2 - Standard (Left) and Ultra-Thin Compatible Transport System (Right)⁴

Another important point of processing thin laminate is material handling. Thin laminate material should be held in two opposite corners while being manually handled to prevent damage.

After being processed through inner layer fabrication, embedded capacitance laminate is tested 100% for Hi-Pot (High potential) testing at 250V or 500V. The IPC specification draft is proposing 250V for material thickness below 50µm (2mils), but actual testing voltage is often specified by the OEMs. During Hi-pot testing, it is very important to take into account the ramp rate and cut off amperage. Current that is drawn during voltage ramping is defined as the following formula:

$$I = C \times dV/dt + i_a$$

“C x dV/dt” is the current that is required to charge the capacitor. Where “C” is a capacitance (Capacitance density x effective capacitive area) and “dV/dt” is voltage ramp rate. The “i_a” is leakage amperage at certain voltage.

As you can see from the formula, with a same voltage ramping rate, higher capacitance material (higher “C”) will be drawing more current. Hence, cut off current needs to be adjusted higher, taking into account the increase in current when conducting a Hi-pot testing for higher capacitance material.

Lamination

Scaling is a very important parameter for multi-layer lamination. Figure 3 shows the measured result of the movements of the distance between the holes during the process. As it can be seen, thin capacitance material’s (12μm) movement was equivalent to that of 50μm (2 mil) core material. Hence, scaling factor for the thin capacitance material can be processed to lamination process just like 50μm core material.¹

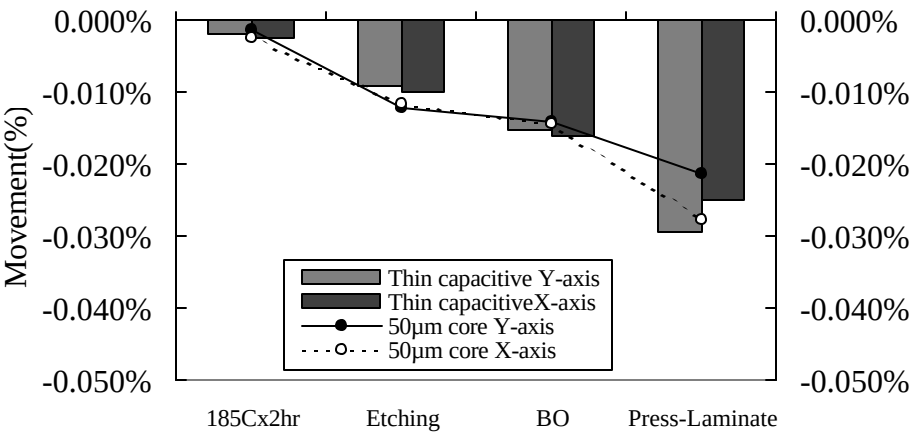


Figure 3 - Dimensional Stability during Each Process

Hole Formation and Plating

Figure 4 shows the cross section of the board using thin capacitive material, 24 microns. Thin dielectric layers and plated copper showed good connection. Also, they showed good compatibility with the surrounding FR-4 laminates. Table 2 shows the reliability tests performed at board level, which showed excellent reliability.

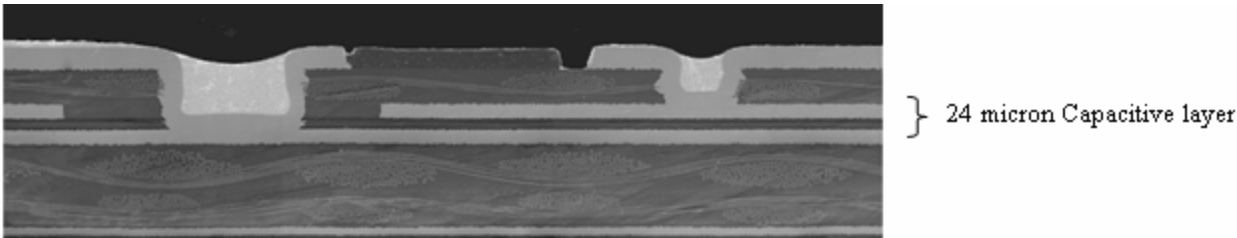


Figure 4 - Cross Section of Embedded Capacitor Layer with Microvia Connection⁵

Table 2 - Reliability Testing on Board Level

Testing	Result
6x Solder shock 288C	Pass
T-260 (>4min)	Pass
IST testing	Pass
Core level Hi-pot testing	Pass
Finished board Hi-pot testing	Pass

RCF Type Capacitor Material

In order to form individual capacitors, as opposed to distributed capacitance, the build-up process using RCF type capacitor material is practical. The processing steps are proposed in Figure 5.

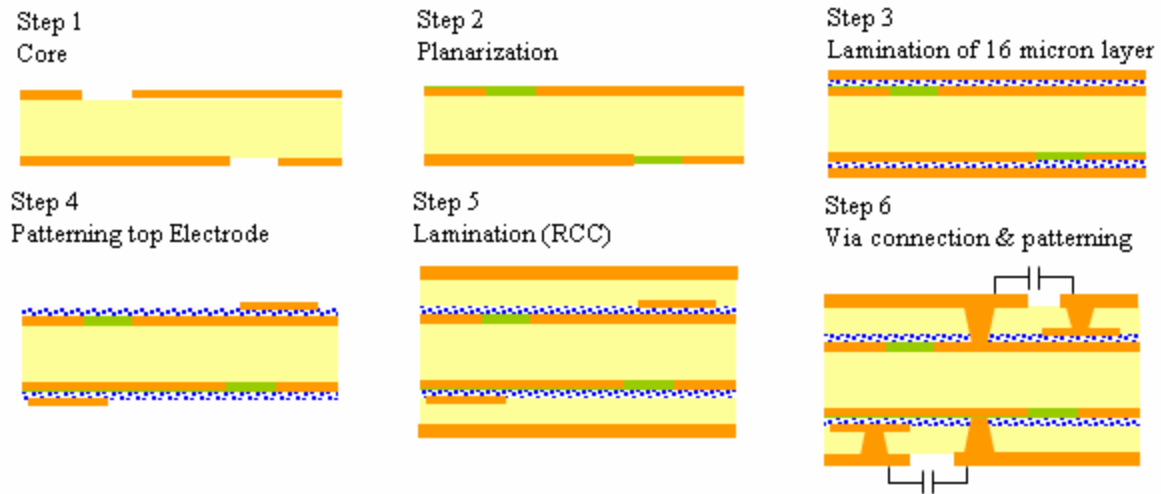


Figure 5 - Capacitor Formation by Build-Up Process

Planarization process is required since dielectric material used for capacitor is designed not to flow, in order to control the capacitance value. In the process of planarization, flat coating material such as UC3000 from San-ei Kagaku Co., LTD can be used. The planarization process has become popular and is a standardized method for build-up technology. It is available from Noda Screen Co., LTD and advanced PCB facilities in Asia and Japan. In Figure 6, a cross sectional picture is shown after being processed for planarization and laminated with 16 micron (RCF). Adhesion between 16 micron (RCF) and inner layer copper showed sufficient bond to withstand solder shock, 288C x 6 times.

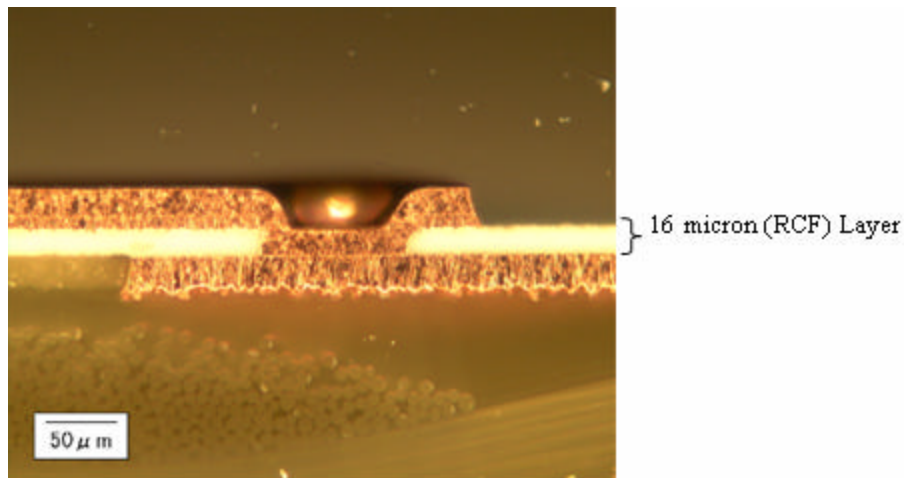


Figure 6 - Capacitor Formation by Build-Up Process

The example of capacitance uniformity is shown in Figure 7. The capacitance was measured on panel size of 470mm x 648mm and 96 individual capacitor with electrode size of 50.8mm x 50.8mm were formed. The data on Figure 7 is combined result of two different panels, 192 capacitors. Uniformity of capacitive layer is within 10% tolerance inside a panel.

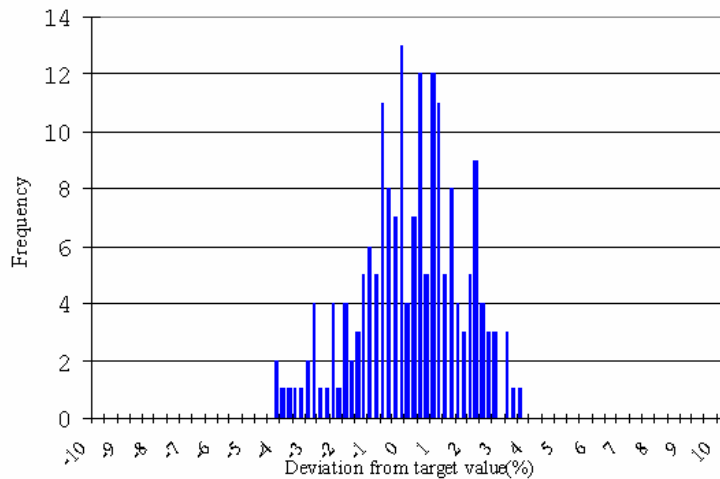


Figure 7 - Transfer Impedance Measurement with Different Capacitor Laminates

Electrical Performance of PWB using Thin Capacitor Material

Many advantages on electrical performance, such as improvements in power distribution network and reduction of Electro Magnetic Interference (EMI), can be expected by using thin capacitive materials in PWBs. For high-end computing and networking systems, power distribution is becoming an issue as data transmission speeds are increasing.

One of the acknowledged solutions to cope with this issue from PWB technology is known as BC (Buried Capacitance) technology⁶. The idea of this technology is based upon the use of a thin laminate as power distribution layers, which function as a decoupling capacitor at high frequency.

Figure 8 is the transfer impedance measurement result for ZBC-2000 and 24, 16 and 12 micron layers (all unfilled materials). As it can be seen, with thinner capacitance material, lower impedance is achieved from a few megahertz and above. This frequency range is the region where it is difficult to decouple with discrete capacitor components. The reduction in impedance has direct impact to decrease in power distribution voltage noise and EMI. Compared with 50 μ m material (typically called ZBC2000), which is the industry standard for BC technology, the 24 micron material has one third and the 12 micron has one tenth of the impedance. This reduction in impedance will allow stable and clean power distribution at the frequencies where the high-end computing and networking system are now starting to operate.

The EMI reduction has been previously reported 1) and can be seen in Figure 9. As the thickness is reduced between the power and ground planes the level of noise decreases as well as the frequencies at which the noise is present.

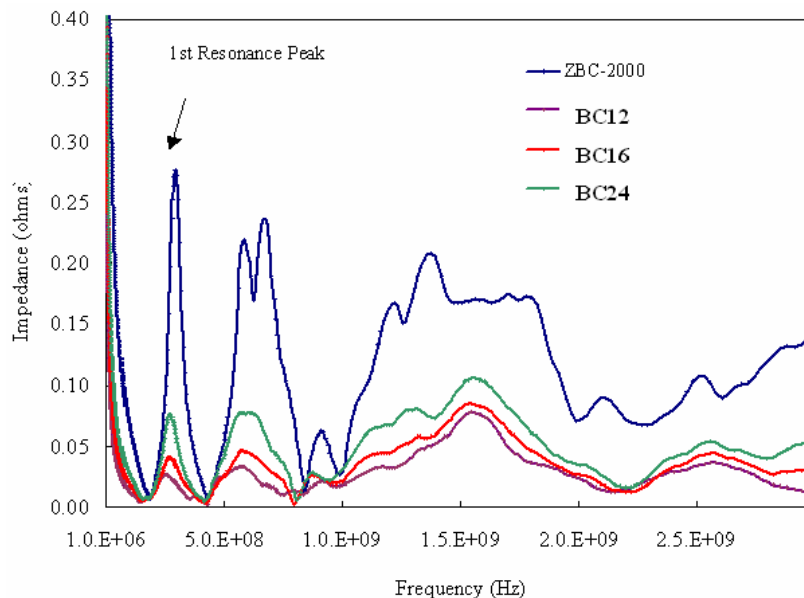


Figure 8 - Transfer Impedance Measurement with Different Capacitor Laminates

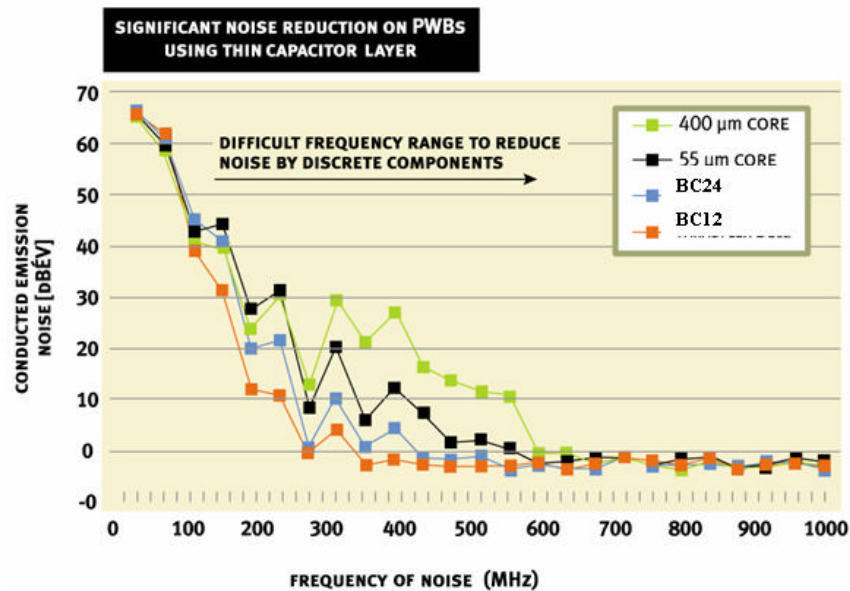


Figure 9 - Radiated Noise vs. Frequency for Various Thicknesses of Materials

The addition of High Dk fillers to the polymer system used for making the capacitor material also affects the impedance versus frequency response. As can be seen in Figure 10, the filled systems show lower impedance on the capacitive side of the graph (the left side before the inflection point). However when the impedance is dictated by inductance (the right side of the graph) the thinnest material has the best performance (although the filled systems still have excellent performance). The addition of fillers also lowers the frequency at which impedance changes from capacitance to inductance driven.

As mentioned earlier, the 12 micron material has electrical properties between the unfilled and highly filled system. At lower frequencies it has a capacitance density and impedance better than the 8 micron material, but not as well as 16 micron material. At the higher frequencies it has better impedance with less noise than the BC16T, but only slightly worse than the 8 micron material. This can be seen more clearly in Figure 11 when the graph is rescaled and only the high frequency response is shown.

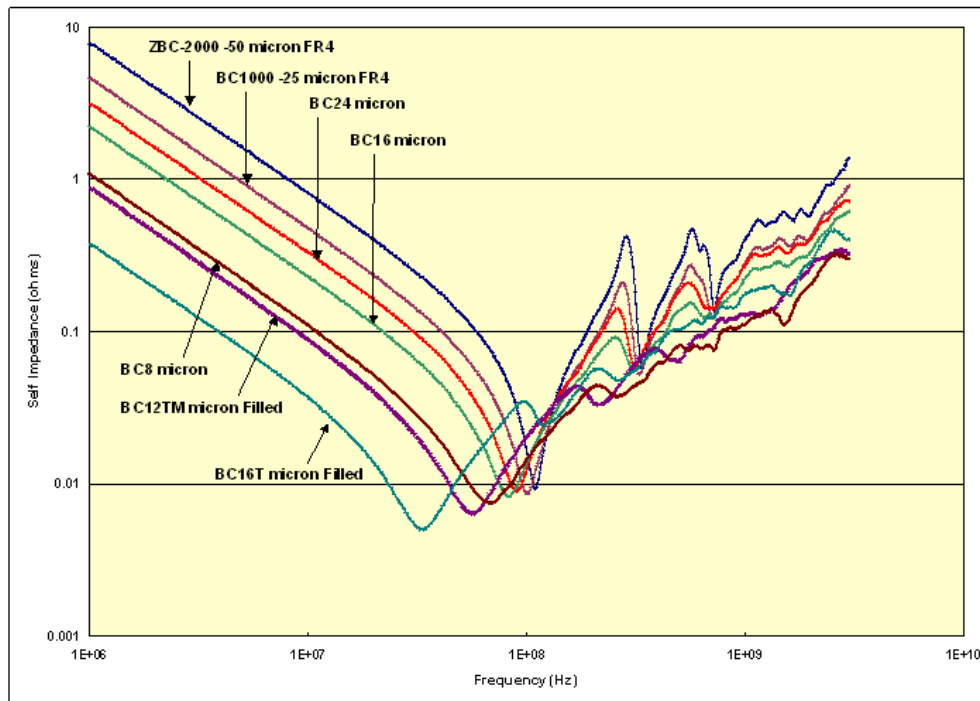


Figure 10 - Impedance vs. Frequency of Various Capacitor Materials- Filled vs. Unfilled

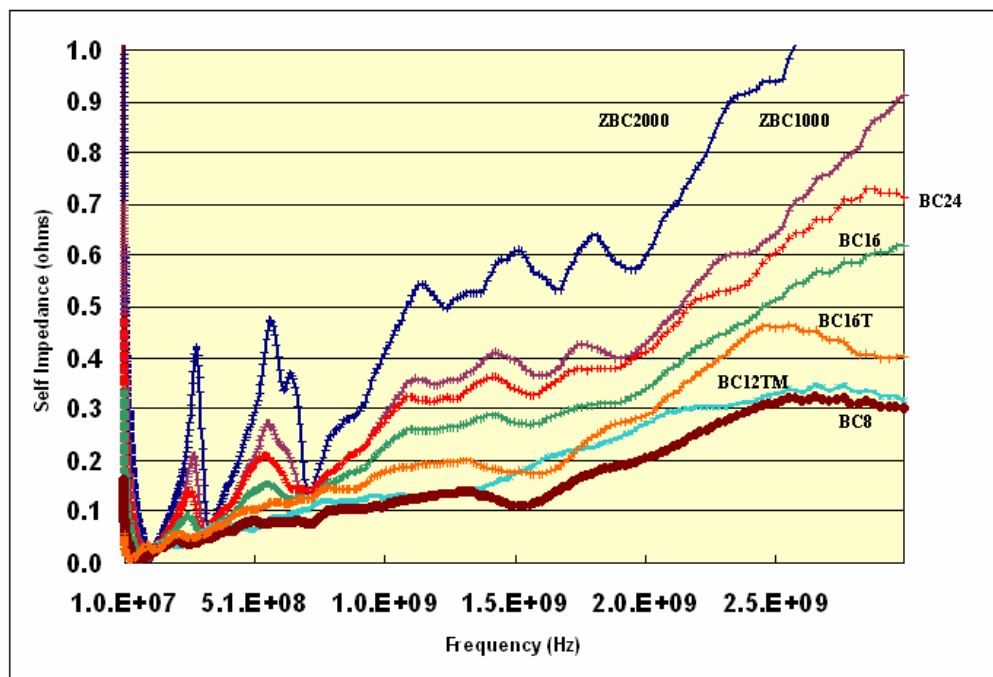


Figure 11 – Impedance vs. Frequency of Various Capacitor Materials – Filled vs. Unfilled

Conclusion

For high-end computing and networking applications, laminate type capacitor material is suitable since the main driver is to lower the system impedance by lowering the inductance. For module type application, RCF type capacitor material is suitable for forming singular (individual) capacitor since it can be fabricated using standard build-up techniques. The partially filled material bridges the two types and can applications in both areas.

For processing thin laminates, consideration of transportation and handling need to be taken into account. For RCF type capacitor materials, planarization step is proposed to form uniform capacitance.

As the demand for a power distribution system with low impedance and control of EMI increases for high-end computing boards with high signal frequency, the use of thin film capacitive material in PWBs are expected to grow.

As the electrical designers get more familiar with designing modules with organic substrates, and with the need to remove discrete components from the surface, the activity of using high Dk RCF material is expected to increase.

Acknowledgement

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Reference

1. IPC 2nd International Conference on Embedded Passives, Andresakis et al., San Jose, CA., June 16-17,2004
2. An improved laminate for embedded capacitance application, Jeffrey Gotro and Jeffery Kamla, 1999 IPC proceedings
3. Embedded Passive Electrical Characterization Results, Istvan Novak, 2000 IPC proceedings
4. Courtesy of Schmid system Inc.
5. Courtesy of Sanmina-SCI
6. IPC Proceeding 2004, Nicholas Biunno et al., Sanmina-SCI.