Presented in the ECWC 10 Conference at IPC Printed
Circuits Expo®, SMEMA Council APEX® and
Designers Summit 05

PCB Design for Flipchip Components

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The emerging technology known as 'flipchips' is poised to take over the world of the portable device. In an age when more and more power and functionality is being offered in ever smaller packages, the flipchip will become mainstream in delivering the promise of "Information at Your Fingertips, Anytime, Anywhere".

Flipchip technology places a specially prepared silicon chip onto a substrate for connection to other chips and to the outside world. Also known as Direct Chip Attach, it uses no traditional packaging, no bond wires, has no lead frame, and has a number of significant advantages and disadvantages compared to current mainstream technology.

A conventional package has these features:
- Adds size and weight to the original silicon die
- Adds environmental protection
- Provides for easier handling
- Provides easier post-package and pre-assembly testing
- Provides all the advantages of standard footprints
- Provides geometric re-distribution for external connections
- Creates mechanical stress relief for thermal excursions

Flipchip technology has a number of singular advantages:
- Size and weight reduced
- Higher performance
- Eliminating lead frame reduces parasitic capacitance
- Eliminating bond wires reduces parasitic inductance and resistance
- High i/o capability
- Extreme packaging density
- Efficient heat removal
- Cheaper in high volumes
- Low profile for portable products

Flipchip technology also has significant disadvantages:
- Known Good Die (KGD) - difficult to guarantee working die
- Very difficult to rework
- Usually requires high tech expensive boards
- Die shrinks change die size, footprint
- Some die are light sensitive and need an opaque coating
- Underfill not a simple issue
- ICs are not always available in die form
- Might need third party rebumping

From a reliability point of view, flipchips have the potential to be ultra-reliable components if thermal mismatches are carefully addressed. There are a number of old mainframe computers still working that have flipchip processors on ceramic substrates. In this case, thermal excursions between die and substrate are evenly matched. This is more difficult to do with conventional organic substrates, but is not impossible with careful design. The critical process is the selection and application of underfill, discussed later in this article.

Conventional organic substrates have severely mismatched Coefficients of Thermal Expansion (CTE), the common and therefore cheaper organic substrates have a propensity for moisture absorption, and some have Glass Transition Temperatures (Tg) low enough to be a problem with high heat dissipation integrated circuits. In all cases, a careful selection of substrate needs to weigh up all of these issues, as well as raw material cost, availability and processing cost.

Underfill is the process of adding a substance into the space between die and substrate in such a way as to inhibit the shear stresses that occur when the substrate and die are expanding and contracting at different rates during thermal excursions. Silicon, the basic material for the die, has a TCE of 3 parts per million per degree Celsius, while the common FR4 substrate has a TCE in the order of 15 to 18 parts per million per degree Celsius. While seeming to be insignificant, this difference becomes critical when there are significant thermal excursions during operation, and become much more so as the die becomes bigger and the amount of expansion and contraction becomes greater. This is especially a problem along the diagonals of the die, where the connections at the corners are most vulnerable.

Underfill material is usually applied with a nozzle as a liquid after the die is mounted and soldered, and is then cured through heat or UV application to form a rigid interface between the die and the substrate. This tends to translate pure shearing forces into a combination of shearing and flexing forces, and so spreads the stresses more evenly around the solder ball. The rheology of the underfill is critical for speed of application and reliability of injection. The complete avoidance of voids is essential - air trapped in the space between die and substrate is fatal to long term reliability, and can lead to vertical die cracks which render the die unusable.

New technologies in the lab hold promise of improving underfill application. Underfill at wafer level that is processed along with the die will eventually replace current technology, which is slow, expensive, and very easy to get wrong.

Current integrated circuit production usually relies on a die mounted on a lead frame and wire bonded to the metal arms that will eventually form the component leads. Current practice is to have one or more rows of bond pads on the die on each of the four sides to achieve this. Flipchip technology currently makes use of the same die but the bond pads are usually in the order of forty microns square on seventy micron centres, making them too small and too close together for reasonable substrate technology. A process of rebumping the die interposes a layer of insulating passivation over the die, opens holes in this layer for a metallization process that re-distributes the bond pad connections to larger balls on larger ball to ball centres, all with maintaining the die's performance. (Figure 1)

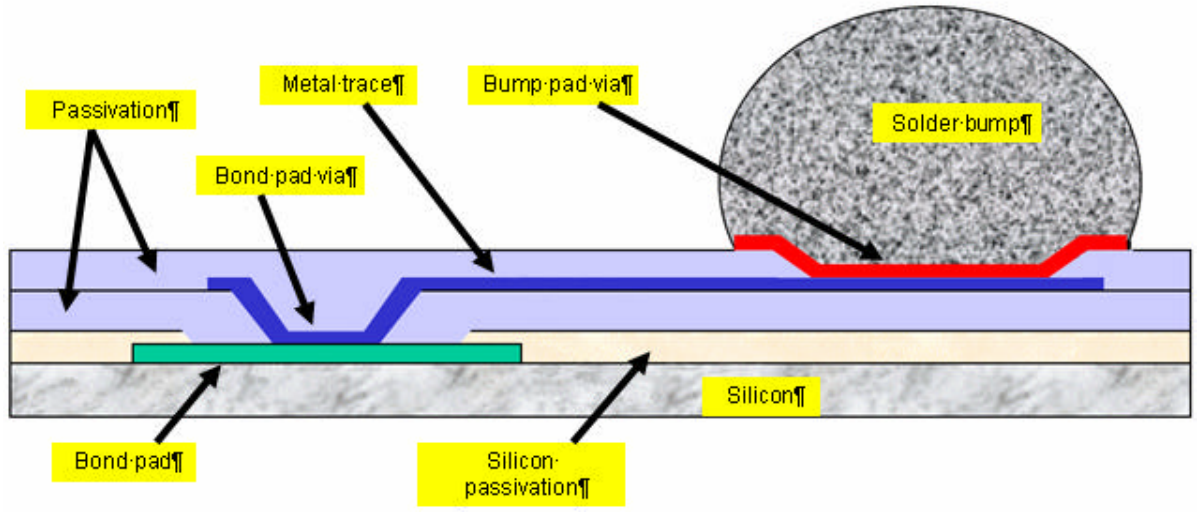

Figure 1 - Rebumping Cross-section

Balls may be collapsible or non-collapsible, can be eutectic tin lead or lead free, with some variations existing in the form of columns instead of balls.

Ball Grid Arrays (BGAs) perform a similar function in that they use an interposer that redistributes the die connections to something more manageable in the real world for a reasonable price. However the very short connections resulting from a rebumped die mounted directly to a substrate (flipchips) have the highest performance.

Die may be attached using conductive adhesives, and much work is being done in this area. However the most common method is still a process of reflow soldering, lead free solders and their higher operating temperatures becoming de rigueur. Stencils for solder application are usually very thin as the amount of solder required is usually very small. In some cases the pin size and pitch in a re-bumped die preclude the use of a conventional stencil and the die might be dipped into flux before placement, relying on the minute amount of solder in the ball to reflow correctly and form a good solder joint.

Current PCB fabrication technology tends to split into two broad categories, mostly known as "PCB" and "IC substrate". The IC substrate processing is essentially the same as conventional PCB fabrication, except for thinner dielectrics, finer lines and spaces and more critical solder mask application. Boards also tend to be smaller and so arrays are more common. The 'IC substrate' fab lines tend to use smaller panels to achieve the tighter accuracy required, and as a result 'IC substrate' circuit boards tend to be considerably more expensive per square centimeter than 'PCB' circuit boards. 'IC substrate' lines currently are mostly providing the huge board volumes required for BGA components.

To achieve the extraordinarily high Input/Output count that flipchips are capable of providing in a very small space, leading edge High Density Interconnect (HDI) technology is mandatory on all but the most trivial of flipchip applications, itself leading to increased substrate costs. Quite often, microvias at the leading edge of the technology are

essential to escape the dense cluster of I/O connections on a die, with the added advantage of minimizing interconnect parasitics like inductance, capacitance and resistance.

Careful choice of substrate is essential. Thermal characteristics may over-ride price considerations, both from internal heat dissipation and with high ambient temperatures. There is increasing use of BT resin laminates because of their lower CTE and higher Tg. BT laminates, despite more difficult processing, also tend to be somewhat stiffer than 'normal' FR4, a significant advantage in thin substrates.

As always, communications between designer, board fabricator and assembler are essential, even more so while flipchip technology is still closer to the leading edge than to mainstream. For board fabrication, design rules in terms of trace width and space, layer stackup and via technology need to be clarified very early in the design process, and need to be confirmed with the board shop if the design rules are anywhere outside the mainstream. Designing boards with high risk design rules that might lead to low yields and therefore high prices is not a great career move, and likely to lead to a sudden career change involving janitorial duties for the designer.

Similarly, it is very important to involve the board assembler early in the design process. Component to component spacing, die to die and die to component spacing, and assembly array sizes are all critical to product success in a competitive marketplace. The type of underfill and the dispensing mechanism is also critical to tight designs, which flipchips invariably are. Again it is essential to design in a way that assembly provides high yields and therefore minimum costs, especially where expensive flipchips are involved. Rework for flipchips that have underfill is close to impossible and needing to throw away expensive assemblies that reduce yields and hence push up costs could again lead to a sudden and undesired career change.

The following texts make an excellent start to the budding flipchip designer. They are all good reference works for PCB designers in general, and very good value:

- CLYDE F. COOMBS Jr., *Printed Circuits Handbook, 5th Ed*, McGraw-Hill, New York, 2001
- CHARLES A. HARPER, *High Performance Printed Circuit Boards*, McGraw-Hill, New York, 2000
- MARTIN JAWITZ et al, *Printed circuit Board Materials Handbook*, McGraw-Hill, New York, 1997
- JOHN LAU et al, *Electronics Manufacturing with Halogen-free & Conductive-adhesive Materials*, McGraw-Hill, New York, 2003
- Charles Harper, *Electronics Packaging and Interconnection Handbook*, 3rd Edition McGraw-Hill, New York, 2000

PCB Design for Flipchip Components

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February 23rd, 2005

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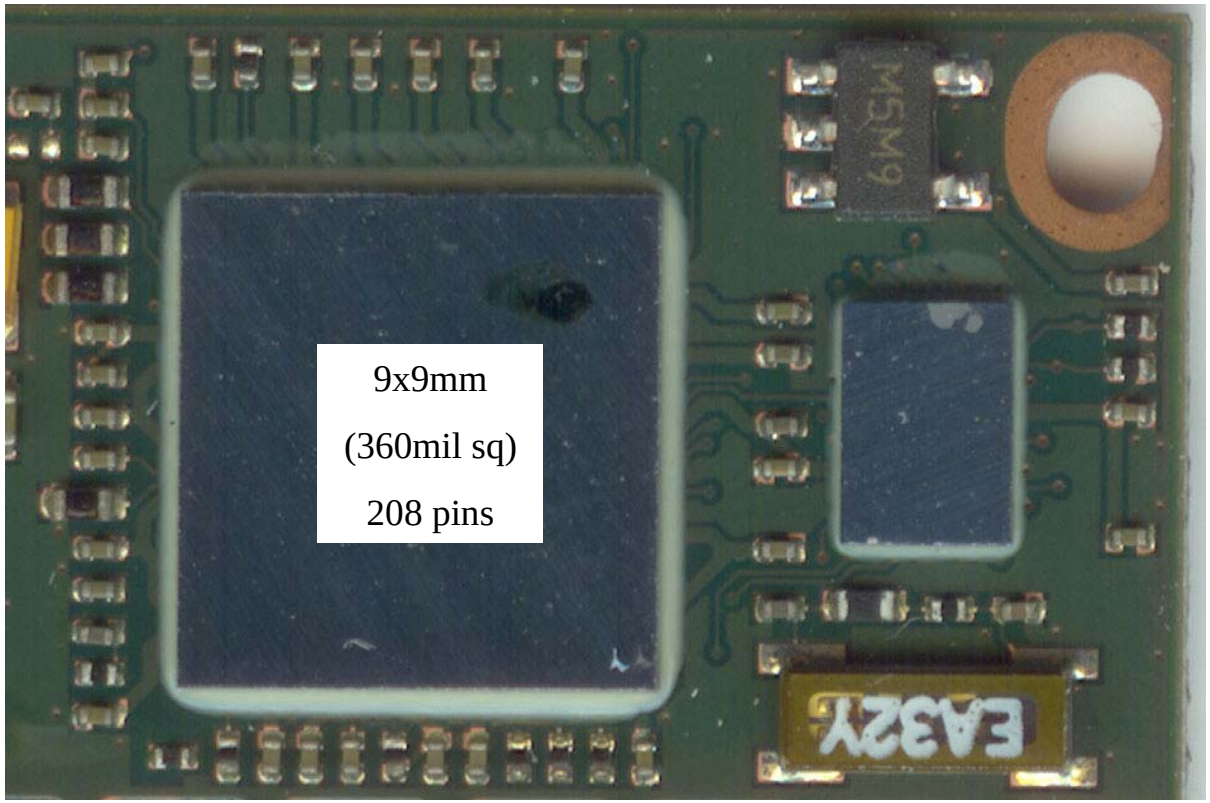
Flipchip defined

Mounts Integrated Circuit silicon die directly to substrate

No wires ----

Direct Chip Attach



Packaged IC

Adds size and weight to original silicon die

Adds environmental protection

Easier handling

Easier post-package and pre-assembly testing

Generates standard footprints

Generates geometric re-distribution

- Increases spacing between external connections

Creates mechanical compliance for thermal excursions

Flipchip advantages

Size and weight reduced

Extreme packaging density – up to 10,000 I/O in lab

Efficient heat removal

Cheaper in high volumes

Lower profile for portable products

Higher performance

- Eliminating lead frame reduces parasitic capacitance
- Eliminating bond wires reduces parasitic inductance and resistance

- Package inductance is reduced 98%
- Package capacitance is reduced 68 to 70%
- Package resistance is reduced 95 - 96%

Flipchip disadvantages

- Assembling Known Good Die (KGD)
  - Wafer level testing fast but not totally reliable – sometimes just DC test
  - Singulation can also produce some defects
- Very difficult to rework
- Usually requires high-tech expensive boards
- Die shrinks will change die size, footprint
- Some die are light sensitive and need an opaque coating
- Underfill is not a simple issue
  - Adds to assembly time and assembly difficulty
  - Critical for assembly reliability but not easy to get right
  - Takes up valuable room for underfill dispensing nozzle
- Desired die is not always available
- Desired die might need third-party rebumping

Reliability

- Flipchip on ceramic totally reliable
  - Very old mainframes still running
- Flipchip on FR4 less reliable
  - Significant thermal mismatch
  - FR4 more prone to warping, with vertical stresses on die
    - Die can crack easily
  - Underfill essential to counteract thermal stresses

Laminate - CTE

TABLE 1.5 CTE Values of PWB Laminates

Laminate	CTE (ppm/°C)	
	x–y	*z*
E-glass/epoxy	16–18	50–70
E-glass/polyimide	13–15	45–70
Woven aramid/epoxy	6–8	100–150
Epoxy-PPO/E-glass	12–18	150–170
S-glass/cyanate ester	8–10	40–60
Nonwoven aramid/epoxy	7–9	90–110
Nonwoven aramid/polyimide	7–9	75–95

Source: Harper p1.10

Glass CTE: 3ppm/°C

Laminate - High Tg

TABLE 1.1 High T_g Laminate Systems

Resin	Reinforcement	T_g (°C)
Bismaleimide triazine—Epoxy	Woven E-glass	170–220
Polyimide	Woven E-glass	200 minimum
Polyimide	Nonwoven aramid	220 minimum
Polyimide	Woven quartz	250 minimum
Cyanate ester	Cross-plied aramid	230 minimum
Cyanate ester	Woven S-2 glass	230 minimum
Cyanate ester	Woven E-glass	230 minimum

Source: Harper p1.5

Laminate moisture absorption, Tg

TABLE 23.1 Typical Values of MLB Material Properties

Material	D_k, 1 GHz	tan δ, 1 GHz	T_g, °C	T_x, °C	Moisture,* %
Difunctional	4.40	0.020	123	277	1.4
Multifunctional	4.43	0.018	134–178	280–295	1–1.5
Polyimide	4.06	0.006	>250	>300	1.0
Cyanate ester	3.65	0.005	>200	>300	—
BT	2.94	0.011	181	295	0.6
PPO-epoxy	3.85	0.012	179	311	0.6
PTFE-glass	2.60	0.001	†	>300	—
PTFE mat-CE	2.79	0.003	†	>300	—
PTFE-ceramic	4.06	0.002	†	>300	0.4

* Percent weight gain for 0.062-in-thick sample after 24 h at 100°C; 100% RH (live steam).
† PTFE is a thermal plastic that melts without a well-defined T_g.

Source: Coombs 4th Edition
p23.8

Underfill

- Matches silicon thermal excursion with substrate excursion
- Rheology very important
- Standard application is capillary flow with nozzle
  - Applied in “L” shape around two sides, one side for smaller die
- Slow for large die
- Voids can be fatal
- Need to leave clearance for underfill nozzle
- Need to leave clearance for underfill fillet
- Solder paste, solder mask must be compatible
- Lab development of “pre-applied” wafer level flux/underfill technology

Rebumping Also called “UBM” – Under Bump Metallisation

Re-distributes bond pads to interconnect balls as array

Re-distribution can suit PCB interconnects ☺

Will increase signal length and reduce performance

Die will eventually have array built into standard silicon

Needs even distribution of balls for underfill “pull-through”

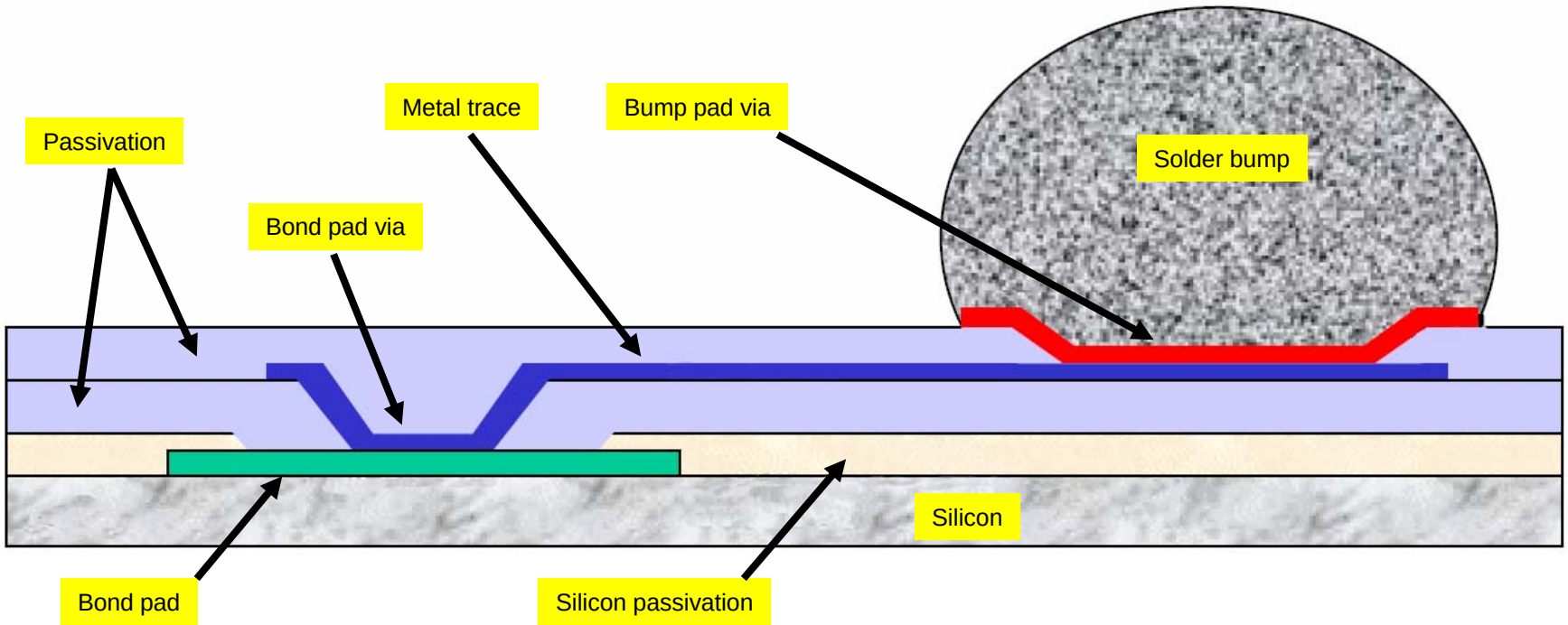
Bigger ball size improves compliance, increases height

Diagonal extremities most vulnerable to thermal cycling

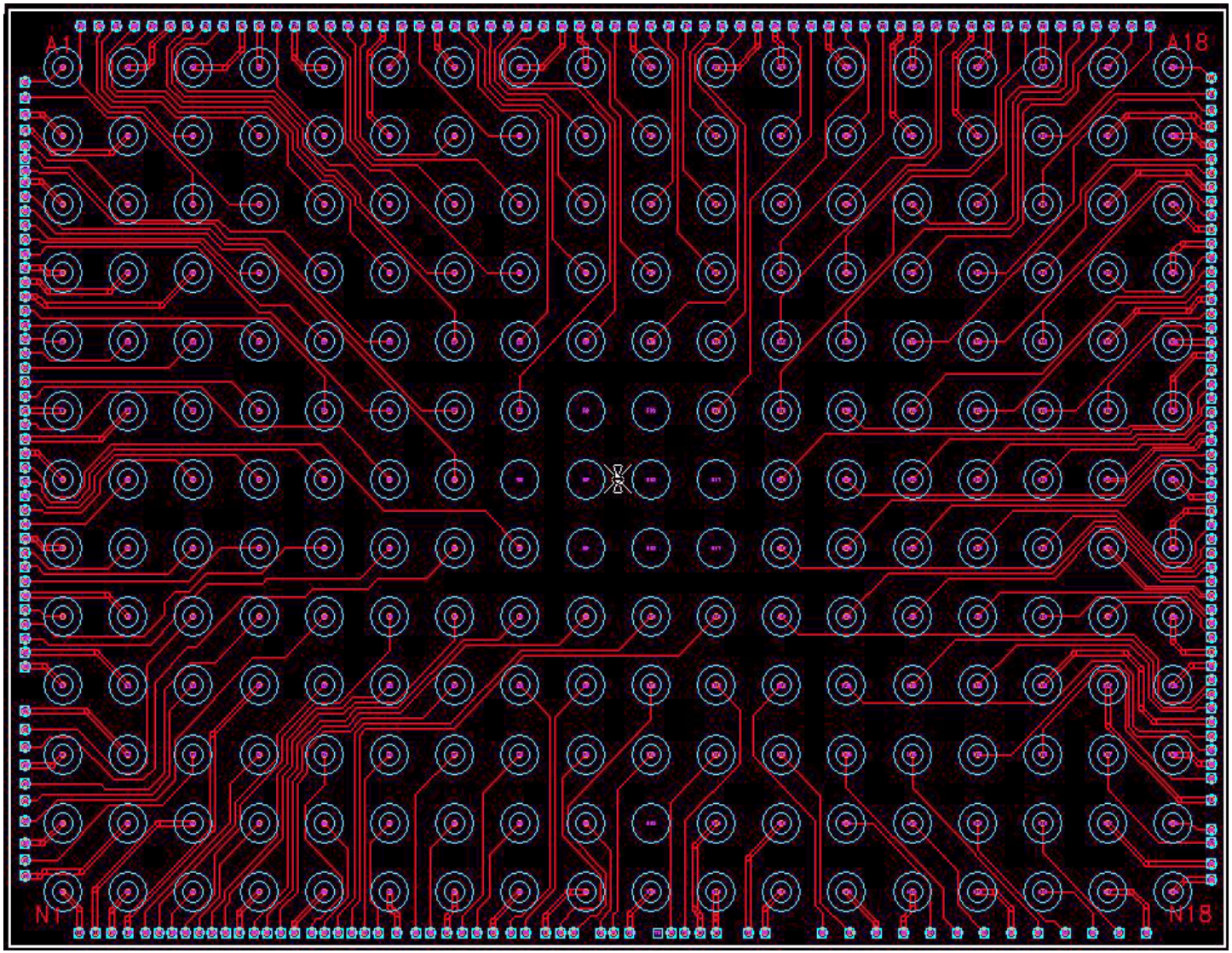
Ball types

- Collapsing & Non-collapsing
- Leaded & lead free

Rebumping Cross-section

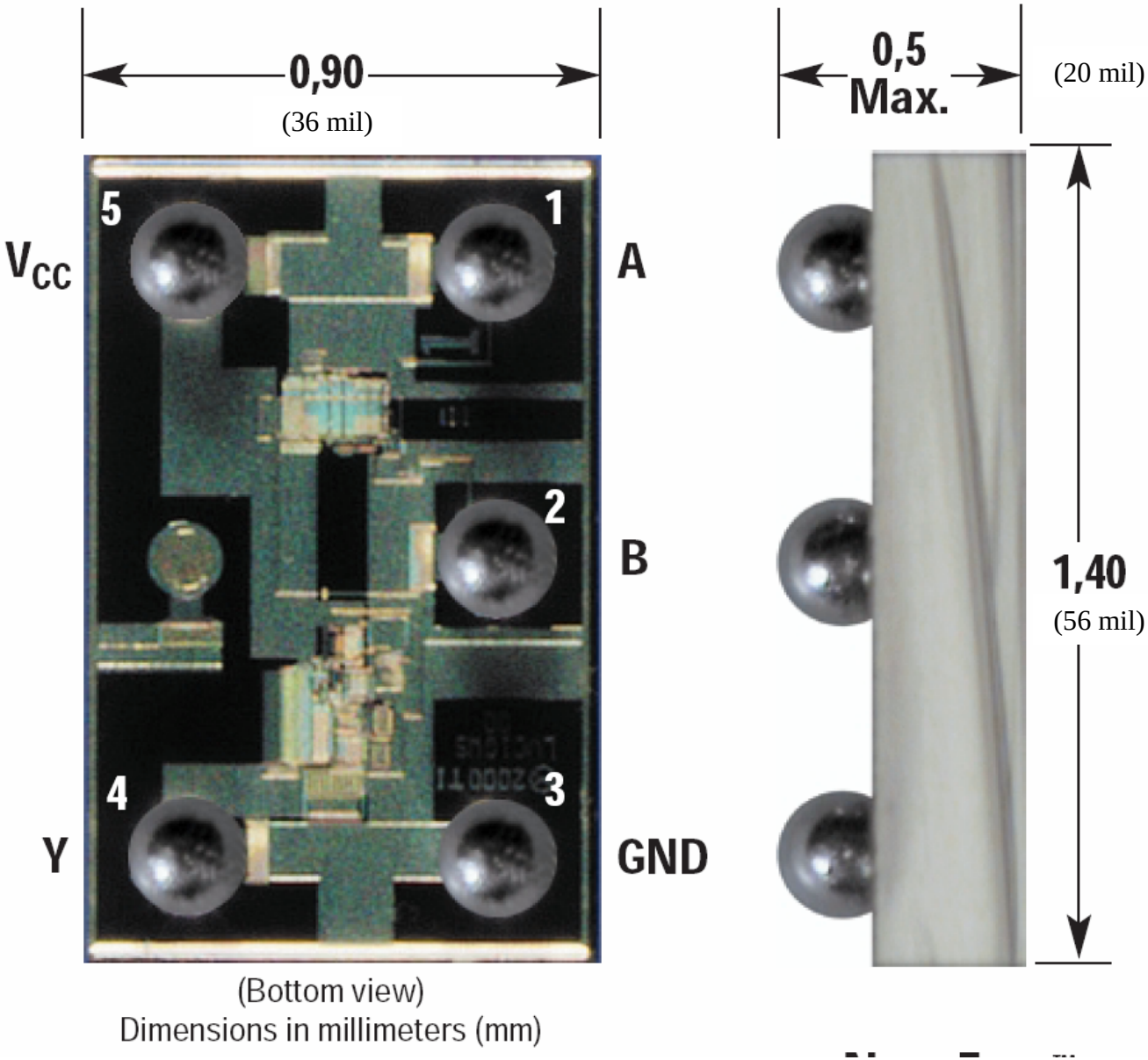


Rebumping



234
Balls

Pitch
360u
(14mil)



Courtesy:

Texas Instruments

Die attachment

- Electronic conductive adhesives can be used
- Pick up, flux dip and place without added paste
  - Tacky flux holds die in place
- Add solder paste – usually only on wide pin spacing
  - Stencil might be very difficult – might need to be very thin
  - Solder paste needs to be compatible with underfill
  - Solder paste generally very fine particles
- Self-alignment during reflow very good

PCB Technology

- Fab splits into PCB and IC Substrate
- Small die sizes with high I/O require high tech boards
  - Special laminates
  - Usually need microvias for HDI
- Ceramic substrates good for TCE match, heat dissipation
  - Expensive
- Organic substrates also feasible
  - BT resin widely used for BGA – Lower CTE, Higher Tg
  - Flex - Polyimide –High Tg, flexible for compliance

Super essential

Talk to proposed board fabricator
Talk to proposed board assembler

PCB Design rules

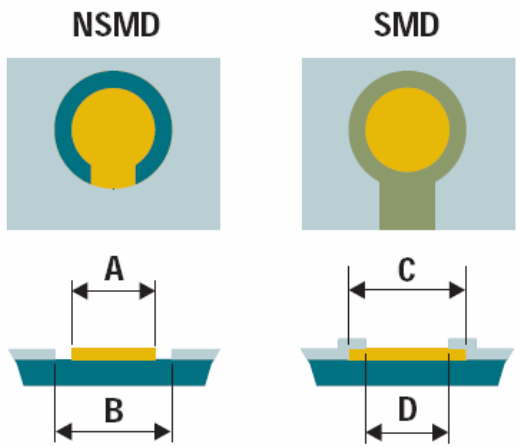
- Trace width/space, internal and external (etch tolerances)
- Via technology, microvia, microvia in pad
- Stackup
- Solder mask technology (registration tolerance)
  - Registration tolerance
  - Ganged mask opening
- Pad technology – (Mask defined, Non-mask defined)
  - Should be same as bump pad or less than 10% bigger
- Traces
  - Dummy traces for even underfill “pullthrough”
  - Beware of microvias in very small pads
  - Thin trace entry to pads, teardrops on vias

PCB Design

Assembly Design rules

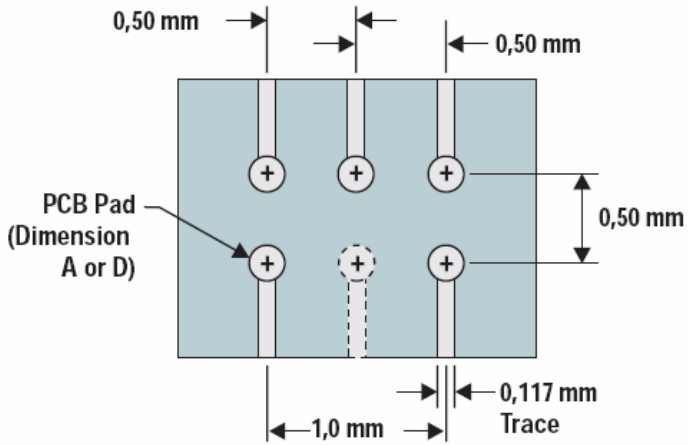
- Component placement clearances – die to die, die to comp
- Underfill nozzle (bigger is better)
- Underfill fillet clearance all around die

PCB Design

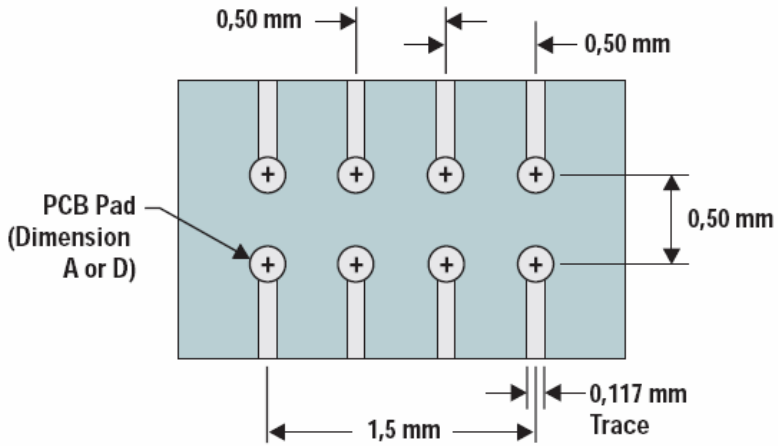


Non-Solder Mask Defined (NSMD) Preferred Method		Solder Mask Defined (SMD)	
Copper Pad	Solder Mask Opening	Copper Pad	Solder Mask Opening
"A"	"B"	"C"	"D"
Small Ball (YEA, YZA)			
0,175 mm + 0,0/–0,025 mm	0,350 mm ± 0,025 mm	0,350 mm ± 0,025 mm	0,175 mm + 0,0/–0,025 mm
Large Ball (YEP, YZP)			
0,225 mm ± 0,025 mm	0,350 mm ± 0,025 mm	0,350 mm ± 0,025 mm	0,225 mm ± 0,025 mm

5-/6-Ball PCB Pattern



8-Ball PCB Pattern

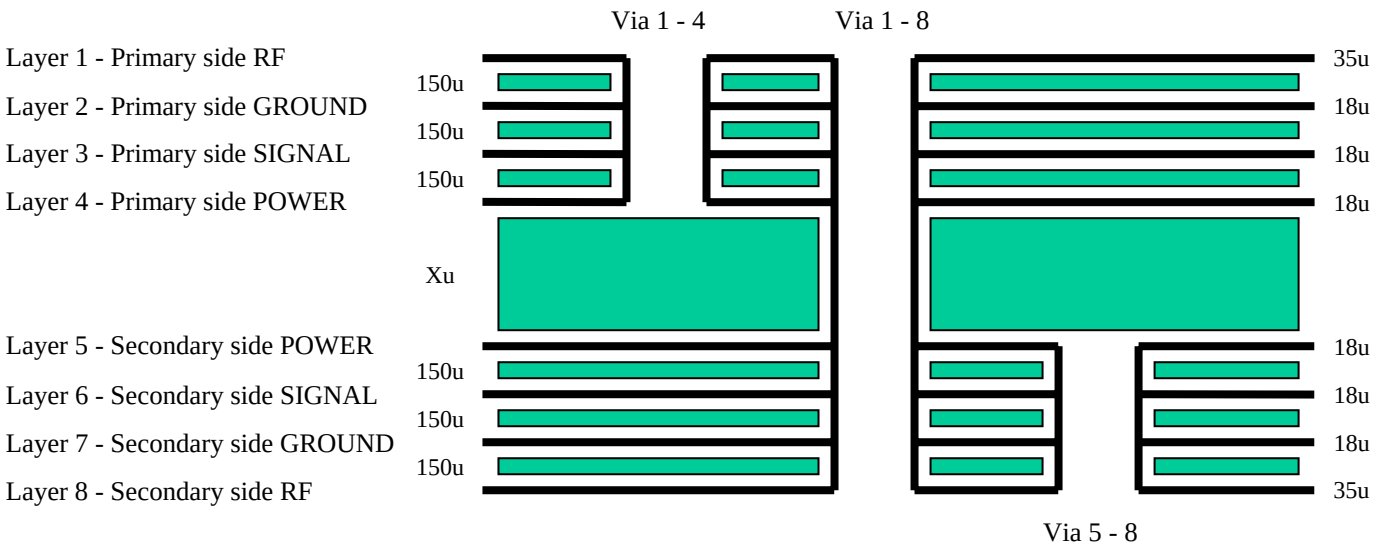


Note: Trace width shall be ≤ ⅔ pad diameter.

Courtesy: Texas Instruments

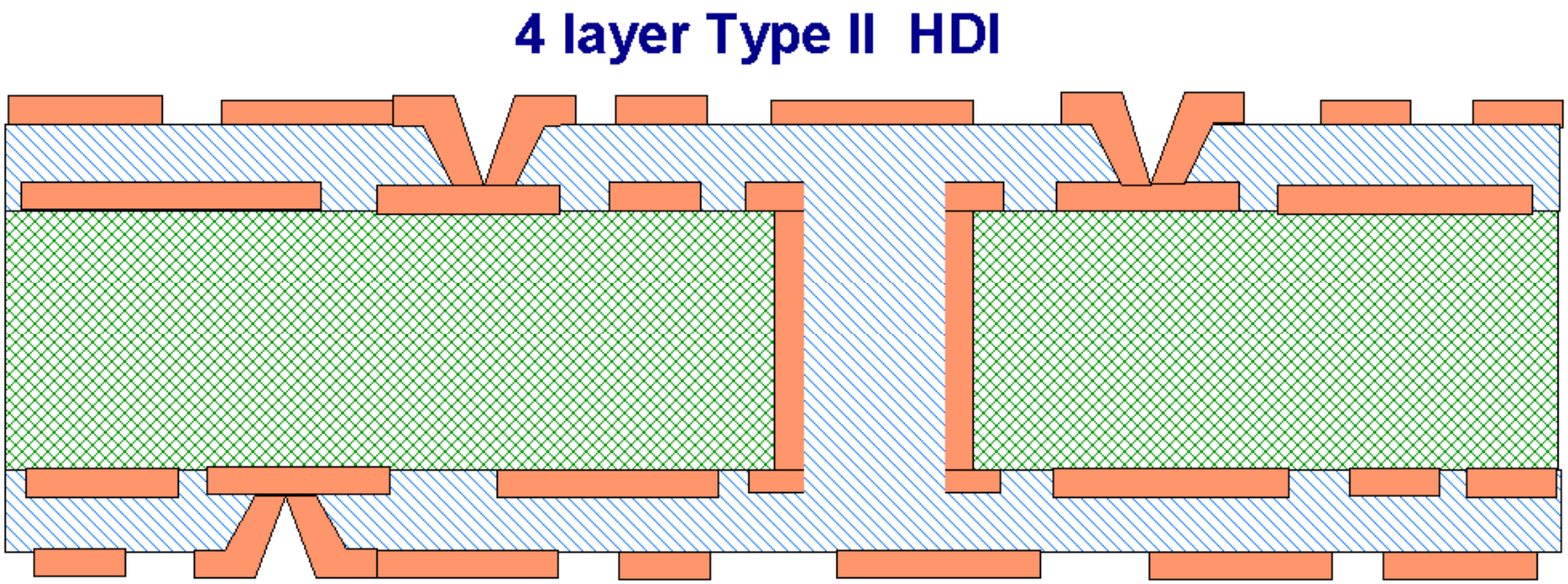
Laminate - Board stackup - Traditional

Typical mobile handset stackup 1998



0.3mm = 50 ohms on surface

Laminate - Board stackup – Microvia 1+2+1



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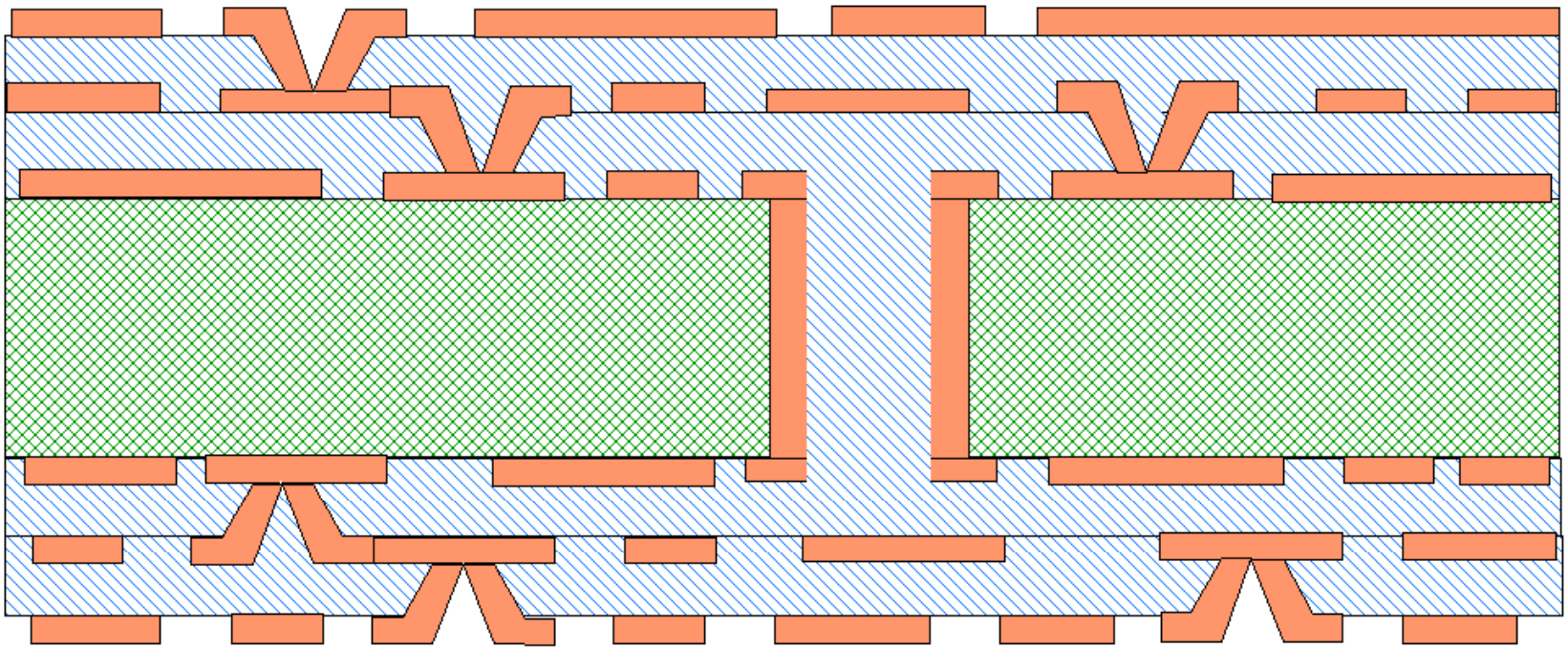
Laminate - Board stackup – Microvia 2+2+2



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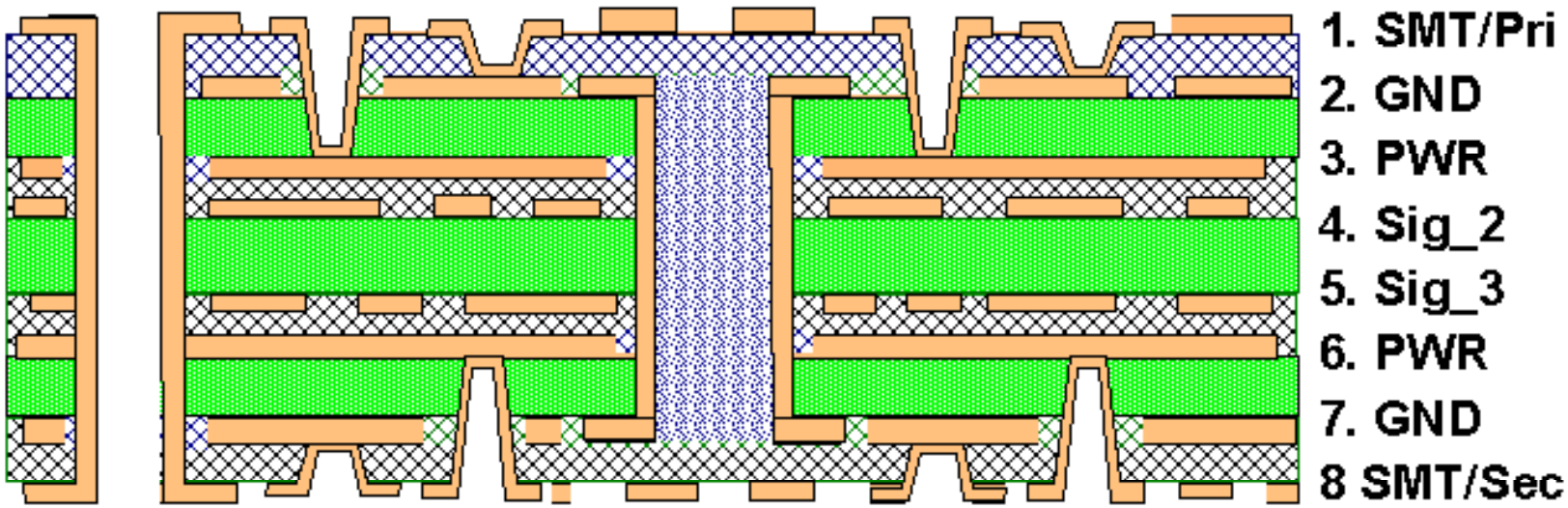
Laminate - Board stackup – Microvia 2+4+2



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Charles Harper, *Electronics Packaging and Interconnection Handbook*, 3rd Edition McGraw-Hill, New York, 2000

Conclusion

Flipchip is the technology of the future

Needs thorough understanding of task to achieve reliable design

Still needs infrastructure to become mainstream

Needs **VERY** close cooperation between

DESIGNER

FABRICATOR

ASSEMBLER