Presented in the ECWC 10 Conference at IPC Printed
Circuits Expo®, SMEMA Council APEX® and
Designers Summit 05

Reference Designs Leading PWB Fabricators to Future Technology

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Abstract
New Chip Packages for advanced electronics are striving for higher density of the printed wiring boards. However, in the supply chain, the PWB fabricator is often the last link that will learn what is needed in terms of packaging density, hole size, line width and space, surface finish and dielectric material requirements.

At the Wireless Terminal Business Unit of Texas Instruments in Denmark, new packaging technology combined with new chip functions are tested in reference designs. This takes place one to three years before the products enter the market in larger quantities. At the early product development only small number of PWBs have to be made to prove that the functionality of the hardware is working and to provide software engineers with "Reference Design" printed circuit boards that will enable software engineers to develop the software for new mobile phone applications.

PWB fabricators that are involved in the early product development have to manufacture PWBs using new fabrication technologies and often new materials as well. The involvement in this advanced technology allows the PWB fabricators to have a one to two years time span to get the technologies and materials integrated in production for large quantities. The reality often demonstrates that proto series are made at companies that do not manufacture volume series at a later stage. Making fast turn around in small series block relatively high capacity in a volume factory and is often avoided unless volume orders are attached.

Based on the past history, it will be explained how difficult it was to have the total supply chain lined up to meet the PWB fabrication technology to manufacturing PWBs for latest chip packages and to be able to source high quality PWBs at acceptable delivery time and cost.

Objective
The aim of this presentation is to describe some of the issues when trying to influence the road map of the leading PWB fabricators.

Introduction
The micro via is the natural evolution from its ancestors, (See Figure 1.) The standard via from the eighties was a solid drill of approx. 800 micrometers capable of drilling a stack height in the range of 4 to 5 millimeters.

In the nineties we saw the mini via take over the scene. The diameter fell to a rest at approx. 300 micrometers and this value is still in use today for through vias.

With the beginning of the new century the micro via found its way to applications where the need for small dimensions was primary. The definition of the micro via size was related to the lower limit of mechanical drilling which in general was 150-200 micrometers at this timeframe. Thus the micro via hole size was below 200 micrometers.

The land or via pad has been the compromise of registration tolerance plus whether the hole should be used for other purposes than just a layer shift e.g. test point or spare hole for jumpers. The designers dream has always been a landless hole or a land that would fit within the connecting track width. Up till present time this is still a dream, as registration tolerances do not seem to be able to keep up the pace, the hole diameter to land diameter ratio is increasing rather than decreasing.

Looking at the line/space history the bar graph for this item is the most stable development with an approx. 50% cut for every 10 years. The drill and land bar graphs on the other hand seem to flatten out a bit in the new century.

The base copper is not included in the bar graph but the base copper pretty much is on a parallel track to the line/space development. To make etching of thinner tracks possible a span of 35 to approx. 3-5 micrometers thickness is expected from 1980 to 2010.

The designer have to keep a close watch at the copper section of the finished line as electric current and resistance per length are changing dramatically for the minimum line widths in the years to come. The days when a minimum line width could easily carry up to 500 milli amperes is rarely seen in present applications.

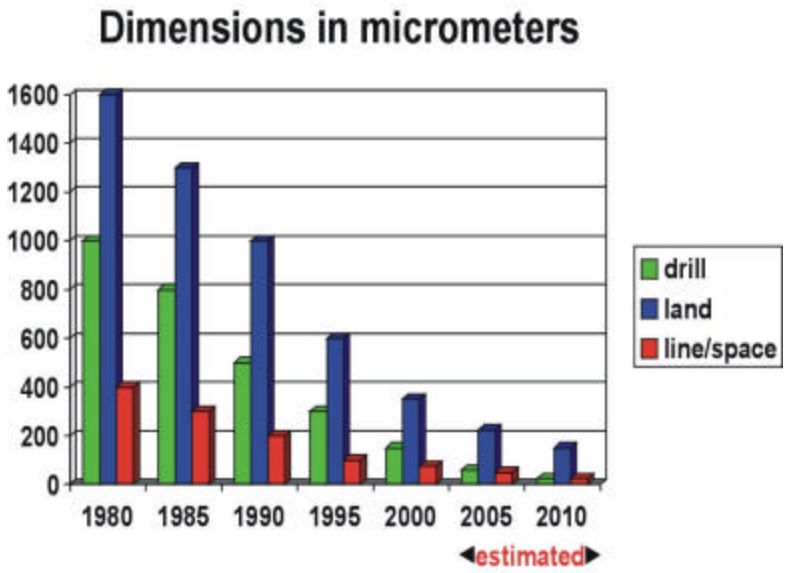

Figure 1 - Connection Element History

Micro via issues

In the case of dense BGA routing this is dictating the hole diameter, the land diameter, etc. When the 0.5mm pitch BGA entered the stage the parameter screw was turned to the limit. Not many volume fabricators were ready to deliver even proto type boards with the new specifications.

Hole diameter

The natural step forward (downward in size) from a 100 micro meter laser drilled hole would be 75 micro meters, see Figure 2, but time has shown that the expectations of 75 micro meters in 2005 did not come all the way through. It is of course possible to buy boards with 75 micrometer drilled holes in volume but there are several issues to consider. One would be the problem of second sourcing as the majority of the leading fabricators still offer 100 micrometers as the smallest drilled hole. The next issue could be the cost per board and this relates to the speed of drilling. Even though CO2+YAG combination lasers have provided both the speed and smaller hole advantage, the large inventory of CO2 lasers in the volume factories are the obstacle to breaking the barrier.

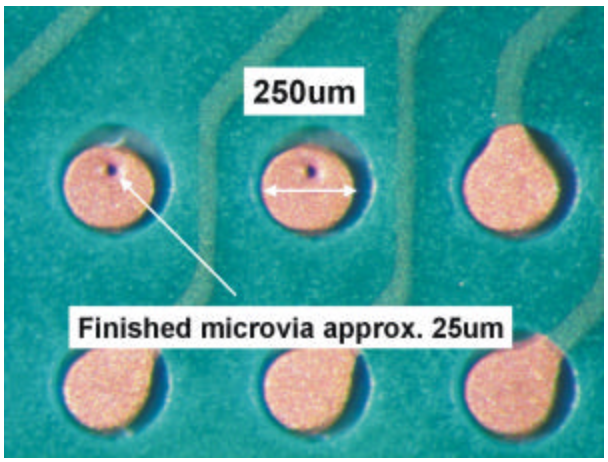

Figure 2 – Micro via Dimensions

Aspect Ratio

Drilling the hole smaller is one thing but keeping the aspect ratio of hole width to hole depth at an acceptable value is a trade off between dielectric isolation distance, 50 Ohm impedance and the 100 micro meter hole diameter. As the 100 micrometer

hole is kind of a fixed value and the aspect ratio must stay in the range of 1 up to 1.3 the dielectric can be calculated to the 50-75 micrometer nominal range.

Filling
The typical pad size for 0.5mm pitch BGA's is 250-300 micrometers and given the 100 micrometer hole, the finished hole is often has an air volume too big for the soldering operation to avoid excessive entrapped air in the solder ball. One option to avoid this issue is to specify surface micro via hole filling also known as copper capping.

Stacking or staggering
To deal with 2 or more layers of micro vias one has to consider if the vias should be on top of each other, stacked or side-by-side, staggered. Stacking is the most space economic way to do it but not the most cost economic way. So far staggering the micro vias has shown to be the current solution and the stacking is reserved for the demanding designs in the future. To place a micro via on top of another require the lower via to be filled and copper capped to provide a flat metal surface for the top via to connect to, see Figure 3.

Base copper
To keep aspect ratio and etching tolerance both at a reasonable level the base copper should be as low as cost and technology permits. Also via filling with galvanic copper has base copper as a parameter, the thinner the base copper is then it leaves more room for heavier galvanic copper and thus better filling.

Materials
Like everything that is mass-produced also state of the art multilayer boards with micro vias are subject to the search for the penny to spare. The standard FR4 has been ruled out several times but it has survived every attack so far. The special materials like BT and others have found their niches and wait for the wider success when FR4 fall short. One exception to the rule is the aramid fiber based laminate that has been used in large quantities in Japan. The advantages of aramid are mainly its dimensional stability and the fact that the fibers are easy to laser drill unlike glass.

One of the improvements to FR4 is LDP (Laser Drillable Prepreg) with its finer glass threads and flatter weaving. (See Figure 4.) The resin rich areas of FR4 LDP are much smaller and this aids the laser drilling to a better quality. To set up the laser to drill equal in almost pure resin or glass bundles, as is the case in standard FR4, is simply not possible with current laser technology.

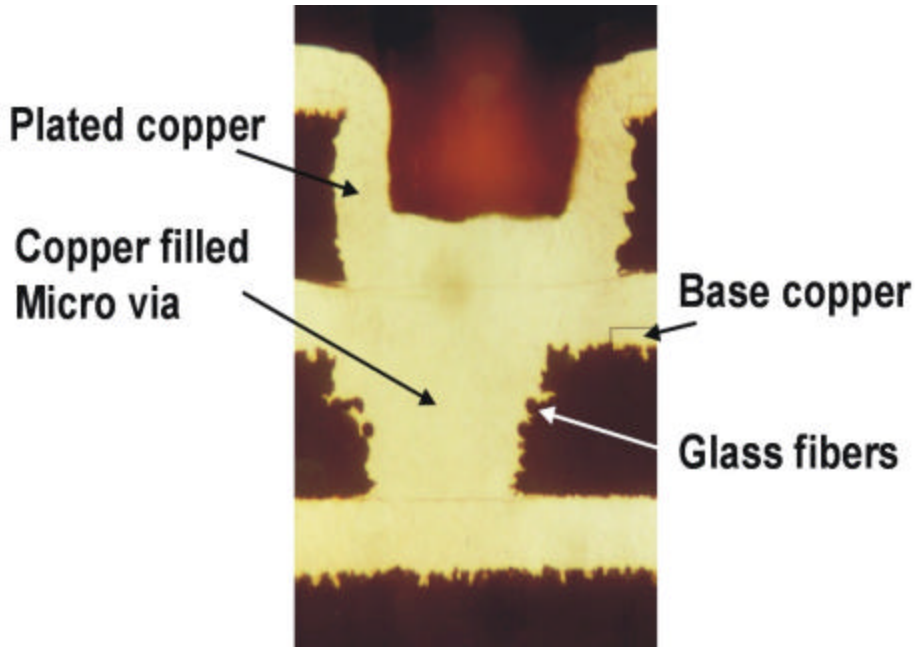

Figure 3 – Filled Micro Via

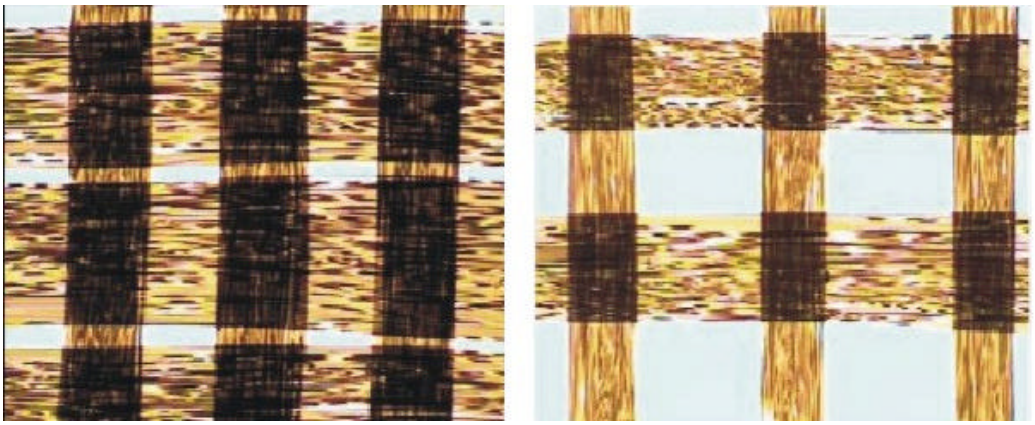

Figure 4 – FR4 LDP and FR4

Preparing For Lead and Halogen Free

In general the preparation for lead free soldering is not concentrated on the PWB but mainly on the supply of electronic components and the soldering process it self as these 2 items cause the majority of problems. The PWB designer should look for 3 items, surface finish, footprints and laminate material. Tin, Silver, immersion gold over nickel, lead free HAL and OSP are the most popular and very familiar surface finishes for lead free use. The designer may contact his mounting facility to get advice on how to upgrade the footprint library.

The halogen free PWB materials are still relative high in cost and often the supply line for this laminate is very thin due to lack of consumption. It happens that the fabricator must report back to the customer that the halogen free material will arrive too late for production and then the standard materials are chosen to fulfill the order. One of the free advantages of using halogen free laminate is the higher Tg value when compared to standard FR4 with its 120-140 degrees C range.

Being ready for lead free production also means testing for higher soldering temperatures. The old solder float test at 288 degrees C for 10 seconds is not as tough a test as it used to be. With soldering temperatures peaking at 250-260 degrees C, the often-used solder float test at 260 degrees C does not stress the finished board to a level where early signs of degradation surfaces. To further enhance the test a second solder float test now for 20 seconds or 2 times 10 seconds may be prepared, good boards will survive this test with no or minor degradation signs. (See Figure 5.)

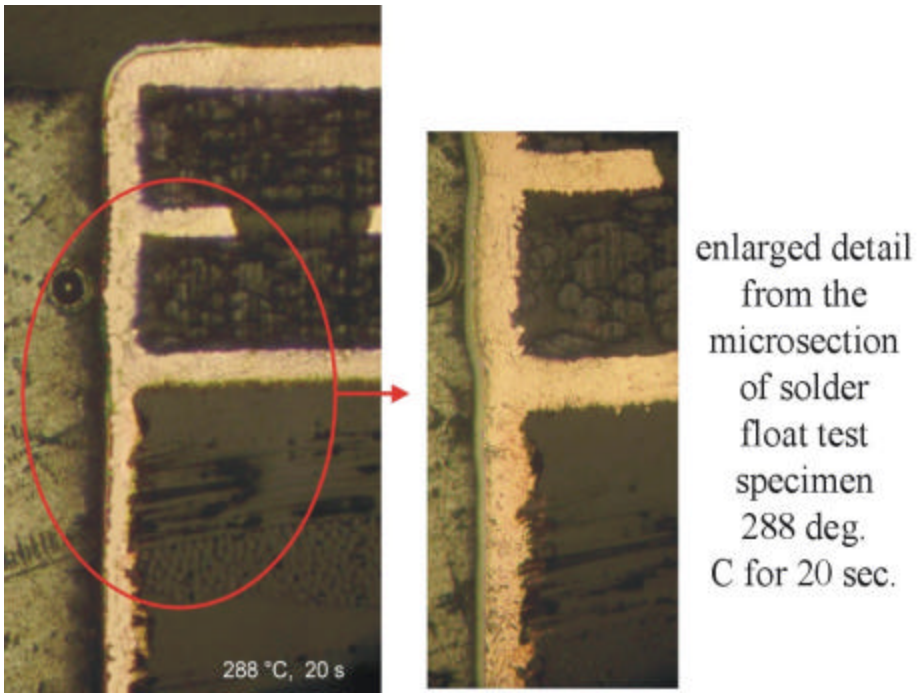

Figure 5 - The Solder Float Test is a Very Aggressive Test for the Dielectric Material, the Resin as Well as for the Copper Through Hole Plating

It has been demonstrated that organic reinforced laminates provide CAF resistance and do not exhibit resin recession even under stringent solder float test condition of 288°C for 20 seconds or several times at 288°C for 10 seconds.

Leading the Edge?
What does it take to change the course of the leading PWB companies just a little bit?

Know the basic processes inside out and stay updated with current + emerging technology. Why? Leading companies will not waste their time on teaching you what you should already know. They want to focus on and give you insight in areas where they are superior.

Share as much information with your fabricator(s) as you can without compromising anyone. The fabricators also want information to build their roadmap upon.

Spearheading fabricators need real life PWB designs with the latest technology to test their processes and technology, test designs made just for testing do not cover the corners like real world. To help the fabricator you must be willing to take some risk and to lower the risk of important projects it may be wise to have a second source to deliver in parallel.

Being up front in technology together with your PWB fabricator(s) mean cooperation and taking a common risk of failure or limited success.

The future is always around the corner and so is the next challenge to the PWB designer, 0.4mm pitch or even smaller pitch BGA's. To conquer this raised bar one has to rely on known but enhanced technology as well as emerging technology.

One of the well known is the any layer technology, it originates in Japan well guarded by patent but several companies around the world have invented their own way to build the PWB with micro vias placed anywhere in any combination even as stacked all the way through. Through holes are still needed though at least for not plated mechanical interface.

Another example is the next generation lasers like the green laser or combinations of UV, green and red (CO2) lasers. Smaller holes are needed for the smaller lands and to make filling the micro vias easier. The new laser generations with higher throughput, small hole capability and removal of both resin, fibers and copper will convince volume PWB fabricators to invest in new rather than current technology.

Advanced Material Options
Reference designs are manufactured 12 to 24 month before any volume production is used. A good knowledge about materials, processes and PWB fabrication technologies is needed to predict what technology will be used in the future. A good knowledge of individual roadmaps is needed as well as latest know how on materials and processes.

As indicated in the earlier part of the paper, finer lines and spaces as well as smaller holes, and micro-via-holes, will be needed to meet future routing density and cost-effective design requirements. Standard FR4 laminates may reach its limits in terms of conductive anodic filament (CAF) resistance and dielectric properties. (See Figure 6.) This is due to the inorganic glass materials and its capabilities to adhere to the resin. Resin recession may result in CAF that create shorts between narrow insulation distances in micro-via-holes or in "layer to layer" areas.

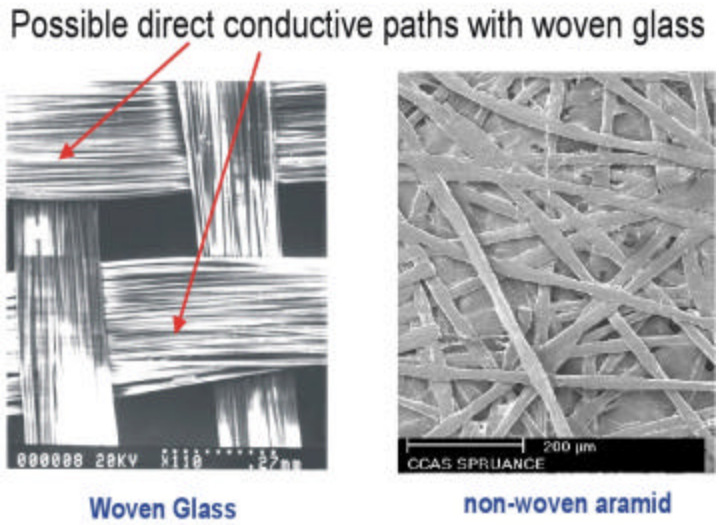

Figure 6 - Comparison of Reinforcements used in PWBs
Woven Inorganic Glass Cloth In Comparison with Non-Woven Aramid

Summary

To lead or influence the roadmap of the heading fabricators is not an easy task as outside factors play a major role.

- Downturns in the world economy tend to delay the scheduled investments.
- Heavy investments in current technology are delaying emerging technologies.
- Have personal contact with the PWB fabricators.
- Monitor the quality of state of the art boards delivered.
- Monitor the limits and possibilities of the board fabricators.
- Read technical articles covering process techniques and laminate development.

Acknowledgements

Analytik - Labor- Possendorf
Weinhold Consulting
Feinfocus
Flextronics
Du Pont
Isola
Polyclad
Masushita
Hytek Aalborg
EIPC (IPC Europe)

ECWC10 feb. 2005

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Leading PWB fabricators
to future technology

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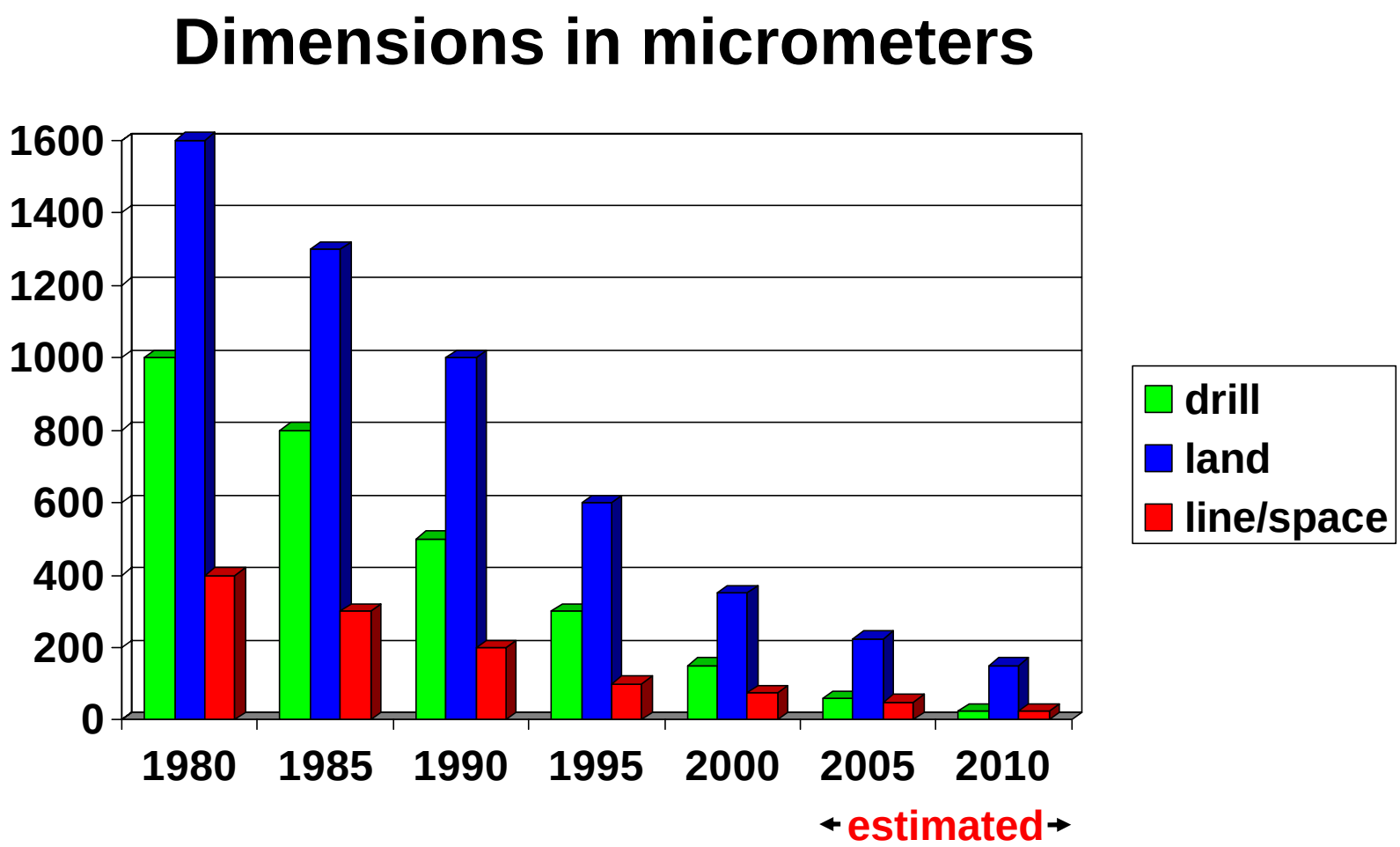
Presentation overview

- Objective
- Microvia issues
- Materials
- Lead- and halogen free
- Leading the edge ?
- Summary
- Questions

Objective

The aim of this presentation is to describe some of the issues when trying to influence the road map of the leading PWB fabricators

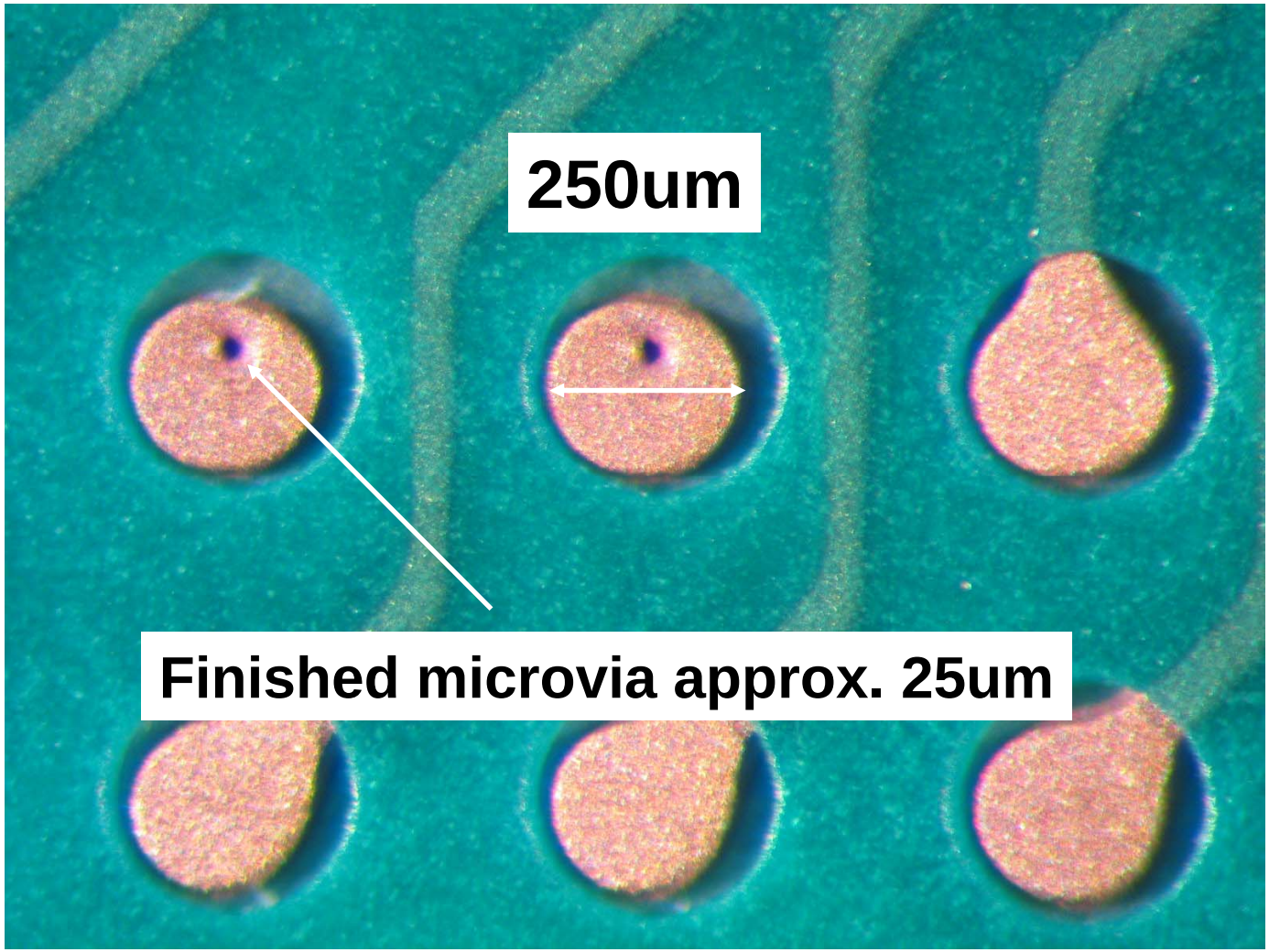
Connection element history



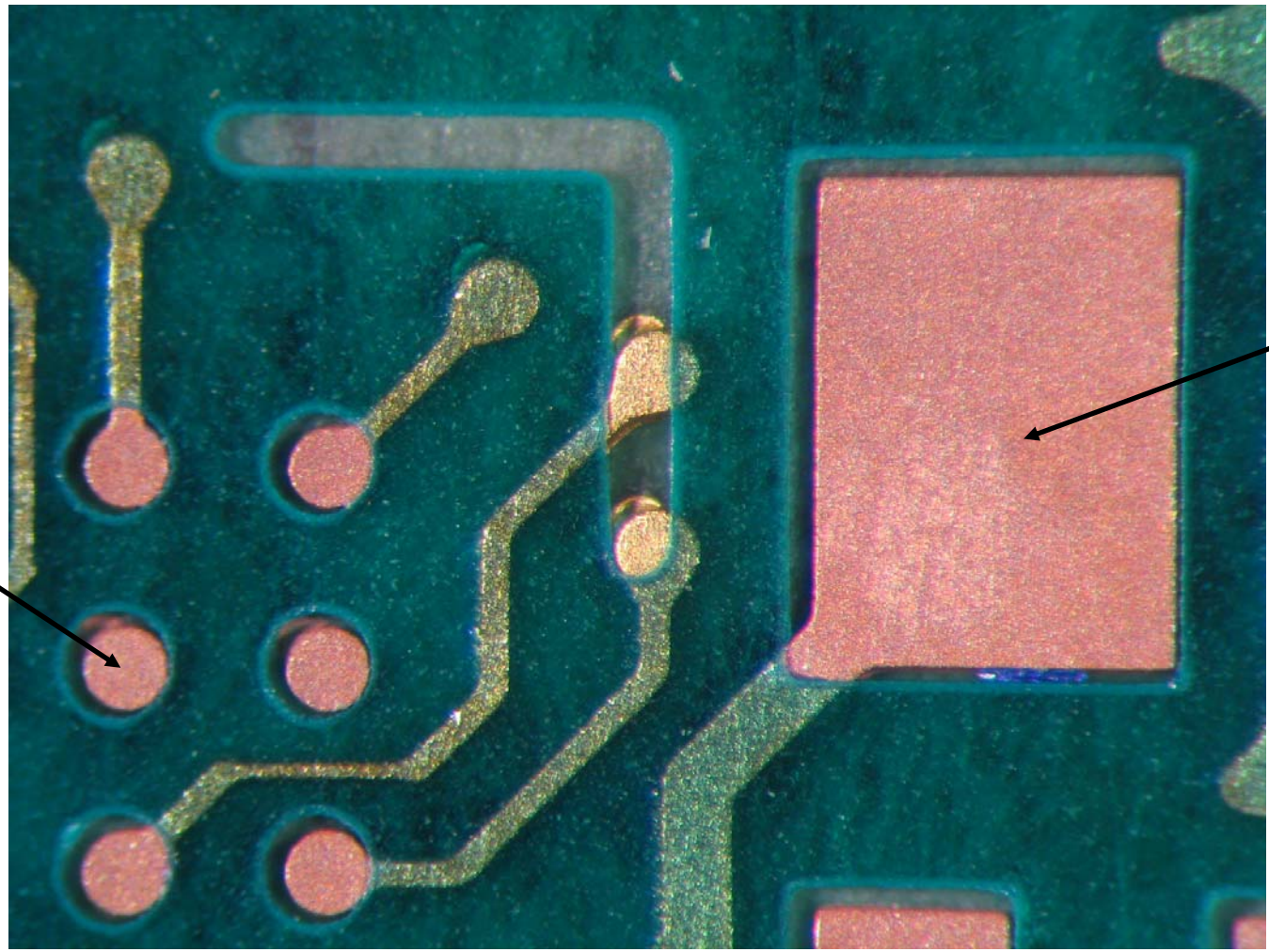
Micro via issues

- Hole diameter
- Aspect ratio
- Filling
- Stacking or staggering
- Base copper

Micro via dimensions



Copper capping



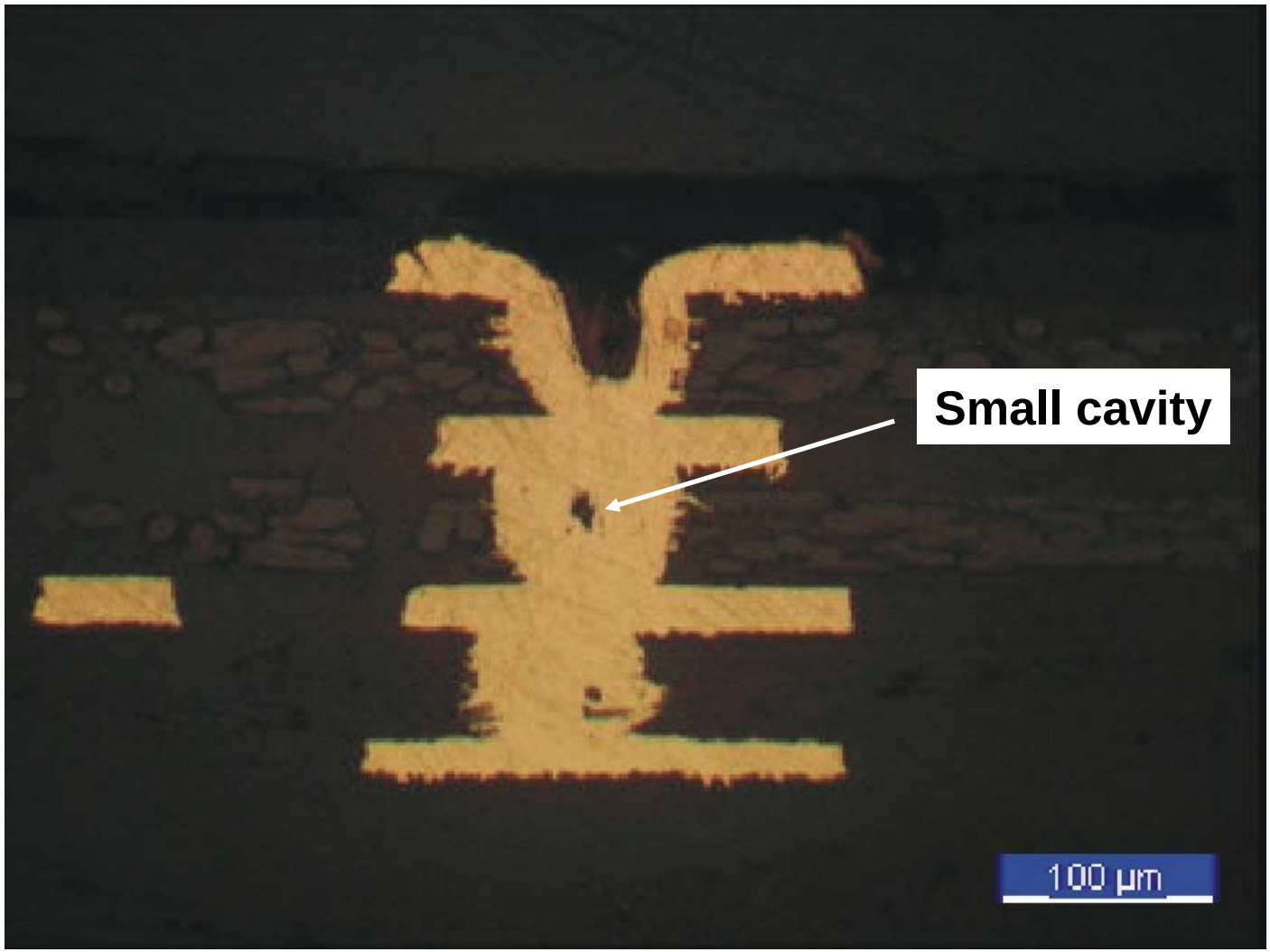
Microvia in pad copper filled

OSP Organic Solderability Preservative

Pattern dimensions

	Today	Near future
Line width (µm)	100->75	75->50
Line spaces (µm)	100->75	75->50
Via hole land size (µm)	250	200->>250
Via hole size (µm)	100->75	75->50
Via hole depth (µm)	70->60	50->40

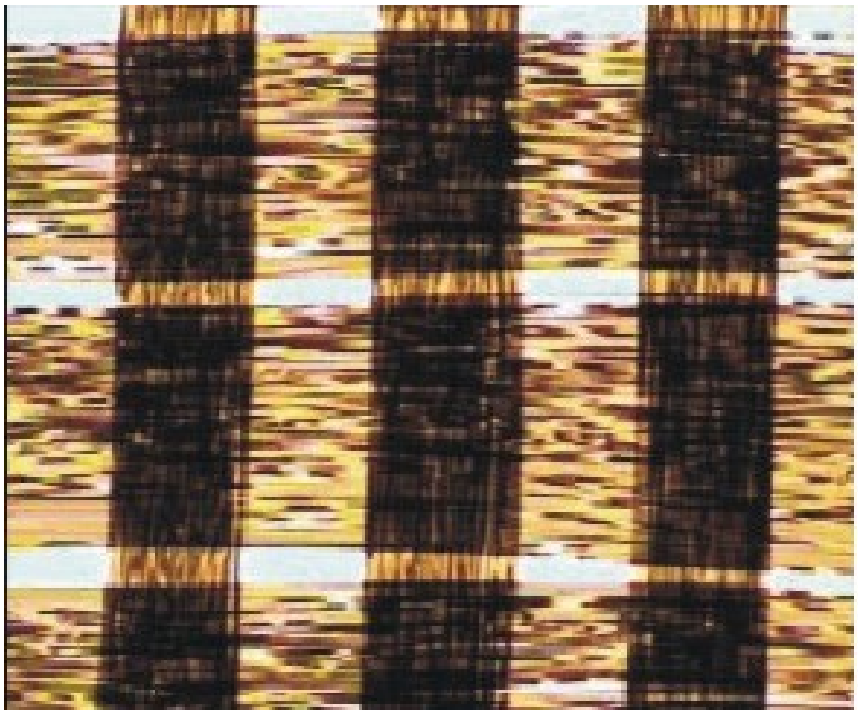
3 layer stacked microvia

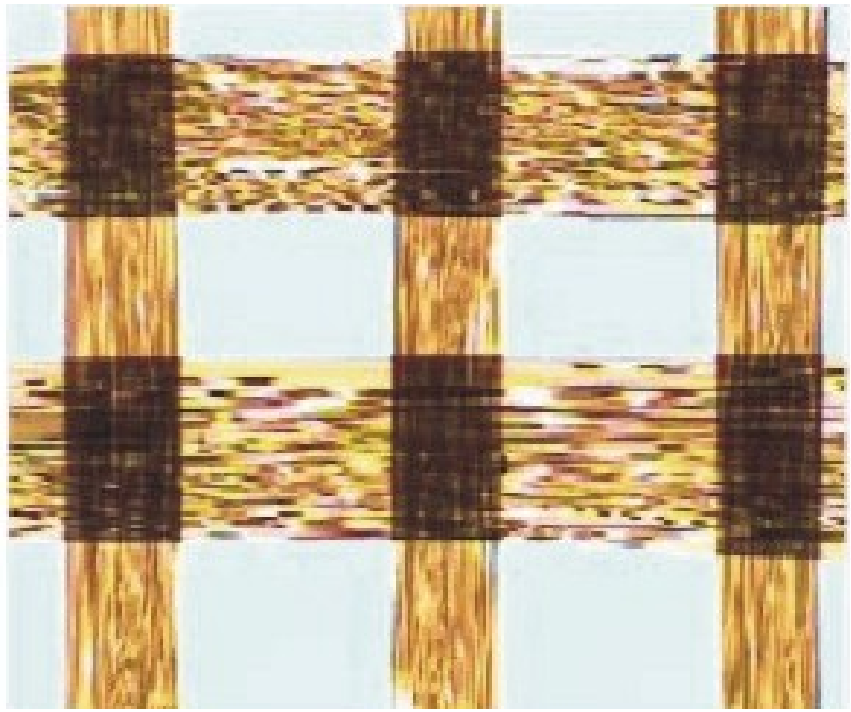


Materials

- RCC
- FR4
- FR4 LDP
- Advanced materials

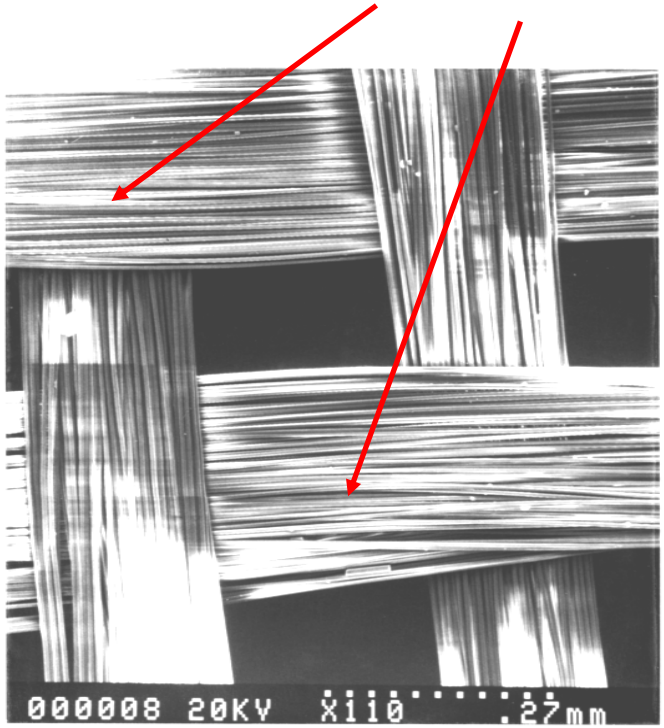
FR4 LDP and FR4



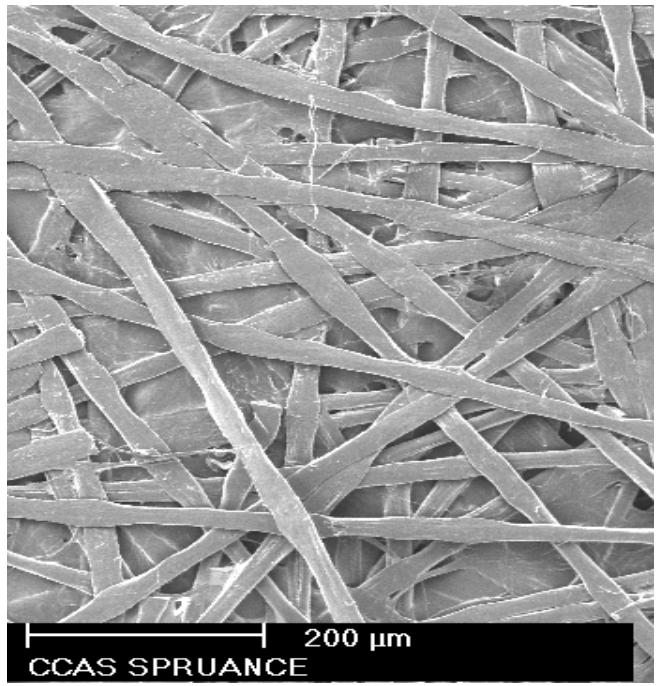


Comparing Glass and Aramid reinforcements

Possible direct conductive paths with woven glass



Woven Glass

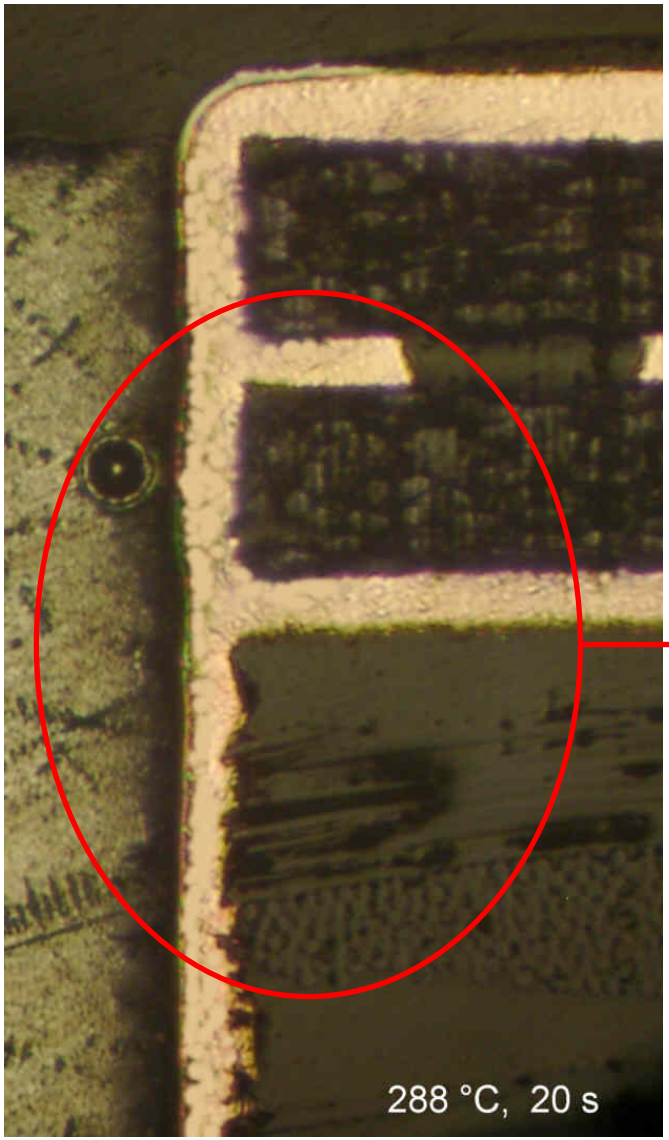


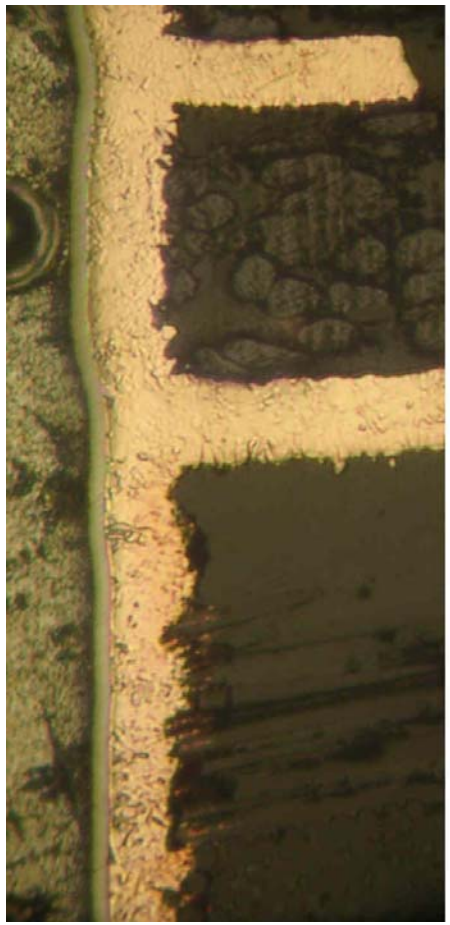
non-woven aramid

Lead- and halogen free

- Halogen free laminate is still expensive and is not off the shelf at any time
- Higher Tg is included
- The board is not the main problem
- Selection of surface finish
- Lead free and the solder float test 288 deg. C min. 10 seconds

Solder float test





enlarged detail
from the
microsection
of solder
float test
specimen
288 deg.
C for 20 sec.

Leading the edge ?

- To lead or influence the road map of the heading fabricators is not an easy task as outside factors play a major role
- Downturns in the world economy tend to delay the scheduled investments
- Heavy investments in current technology are delaying emerging technologies
- Cooperate advanced projects with your PWB fabricator
- Know the basics of PWB fabrication and stay updated

Summary 1

- Have personal contact with the PWB fabricators
- Monitor the quality of state of the art boards delivered
- Monitor the limits and possibilities of the board fabricators
- Read technical articles covering process techniques and laminate development

Acknowledgement

- Analytik - Labor- Possendorf
- Weinhold Consulting
- Hytek Aalborg
- Feinfocus
- Flextronics
- Du Pont
- Isola
- Polyclad
- EIPC (IPC Europe)

Questions ?