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The Integration of Third-Party Boundary-Scan Products into Customer Preferred Test Platforms has Become and Attractive Cost Effective Test Solution

Anthony Sparks and Pete Collins
JTAG Technologies, Inc.
San Diego, CA

Abstract
In today's complex manufacturing test environments, it is becoming increasingly difficult to detect and diagnose structural faults within highly complex multi-layer PCB designs that offer extremely limited physical test access.

The widespread use of array style packaging i.e. BGA, CSP and FCA have resulted in significant limitations in physical test access, reducing the effectiveness of conventional test methods such as in-circuit test in favor of other complimentary test strategies. This is further complicated by the EU directive (WEEE and RoSH) that legislates that companies must adopt a lead-free soldering process by 2006, which will have a significant impact on the effectiveness of physical contact probing methodologies i.e. in-circuit test and flying probe testers.

This paper explores the utilization of boundary-scan as an alternative complimentary low-cost, high-performance but more importantly a non-contact, fixture-less test methodology. It also examines the significant benefits offered by importing legacy boundary-scan tests directly, without the need for redeveloping tests for execution on to a contract manufacturers preferred test platform.

Introduction
Circuit cards with thousands of devices, in excess of 10,000 circuit nets and 18 or more PCB layers are not unusual in modern design practices. Unfortunately, as the level of PCB complexity increases, so too does the expected presence of manufacturing faults.

Conversely, the ability to provide the adequate number of test points to enable traditional test strategies such as In-Circuit Test (ICT) to sufficiently verify the manufacturing process diminishes. High-speed functional performance requirements often preclude the use of discrete test pads in order to maintain noise immunity and overall signal integrity. Furthermore, the widespread use of Ball Grid Array (BGA) packaging with concealed contacts complicates the access problem.

In other words, board testing is becoming extremely difficult due to reduced test coverage at ICT, thereby driving the adoption of alternative test methodologies such as Automated Optical Inspection (AOI), Automated X-ray Inspection (AXI), Flying Probe Testing (FPT) and Boundary-Scan to provide complementary test coverage[1].

The reality is that these complementary test strategies are used to answer four rudimentary, manufacturing assembly integrity problems:

- Are the correct parts placed on the board?
- Are the parts placed in the correct location and orientation?
- Is the soldering quality appropriate and error free?
- Does the board operate and function as intended?

The Impact of Increasing Density on Test
The traditional method of testing electronic assemblies for structural faults has been In-Circuit Test. ICT drives electrical stimuli onto the board-under-test (BUT) and captures the responses to the electrical stimuli using physical probes that make contact with the BUT via test-pads connected directly to circuit nodes. The physical nails are arranged within a test fixture, commonly referred to as a "bed-of-nails" which is uniquely customized for each BUT's test access requirements.

A potential problem with this test strategy is that changes in the board design which result in the re-routing of PCB tracks can also mean the re-positioning of devices and/or test pads. Changes in artwork normally mean that bed-of-nails test fixtures that had been developed for previous revisions of the design will now be obsolete. This is the reason why bed-of-nails test fixtures are not developed until a PCB design has reached the pre-production phase when the design will be stable and not subject to further iterations in PCB layout.

As board designs are steadily becoming more complex, the test equipment vendors are continually pushing ICT technology. Testers capable of accessing in excess of 5000 nodes are now available, but the corresponding bed-of-nails test fixtures are so

densely packed with test probes that they commonly require the use of pneumatics to adequately compress the cumulative force of thousands of test probes in such a dense arrangement. Both of these factors lead to extremely heavy and extremely expensive test fixtures that can potentially become obsolete upon board artwork changes. Furthermore, a test fixture with such a high number of test probes can be subject to inconsistent results due to poor pin contact, particularly with manufacturing strategies that adopt a "no clean" process.

With each increase in the level of board complexity, the likelihood of any given board containing a structural fault rises. A paper by Charles Robinson and Amit Verma of Teradyne Inc[2] presents a dramatic picture of the impact of fault density on manufacturing yield: *even "world-class" factories (with quality levels in the range of 100 parts per million structural defects) will experience single-digit yields when 20,000 solder joints are present.* In other words, nearly every board produced will contain one or more structural defects, all of which must be detected and repaired before shipping the product.

Despite the advances in ICT technology, board manufacturers have experienced a steady decrease in test coverage. This decline is the result of the worsening imbalance between actual circuit nodes on the board and the number of circuit nodes that can be accessed with the test fixture.

Four factors account for the decrease in the placement of test pads:

1. Direct access to package pins in many cases is not possible because of new SMT package designs such as BGA and Chip-Scale Packaging (CSP).
2. Complex circuit designs do not have the physical space for additional test pads to be placed during layout.
3. High performance systems prohibit the use of test pads to avoid introducing EMI noise.
4. Many traces are not visible on either side of the board.

Change in Manufacturing Practices

In today's competitive marketplace, reducing manufacturing costs is a high priority. To this end, a tremendous amount of manufacturing is exported to low labor cost areas, distant from the groups that design the product and associated test systems. As test coverage deteriorates, the number of faulty boards erroneously passed to the next process stage, usually functional test increases. Since diagnostics at the functional stage can often be ambiguous making troubleshooting failures difficult, time consuming and dependant upon an extensive level of knowledge of the product and test system, the end result may be a large "bone pile" of boards that contain process faults that are extremely difficult to diagnose, ultimately leading to greater cost.

Because of the high and increasing costs associated with the process verification test of complex boards, manufacturers (and test equipment vendors) have developed and adopted alternative solutions as shown in Figure.

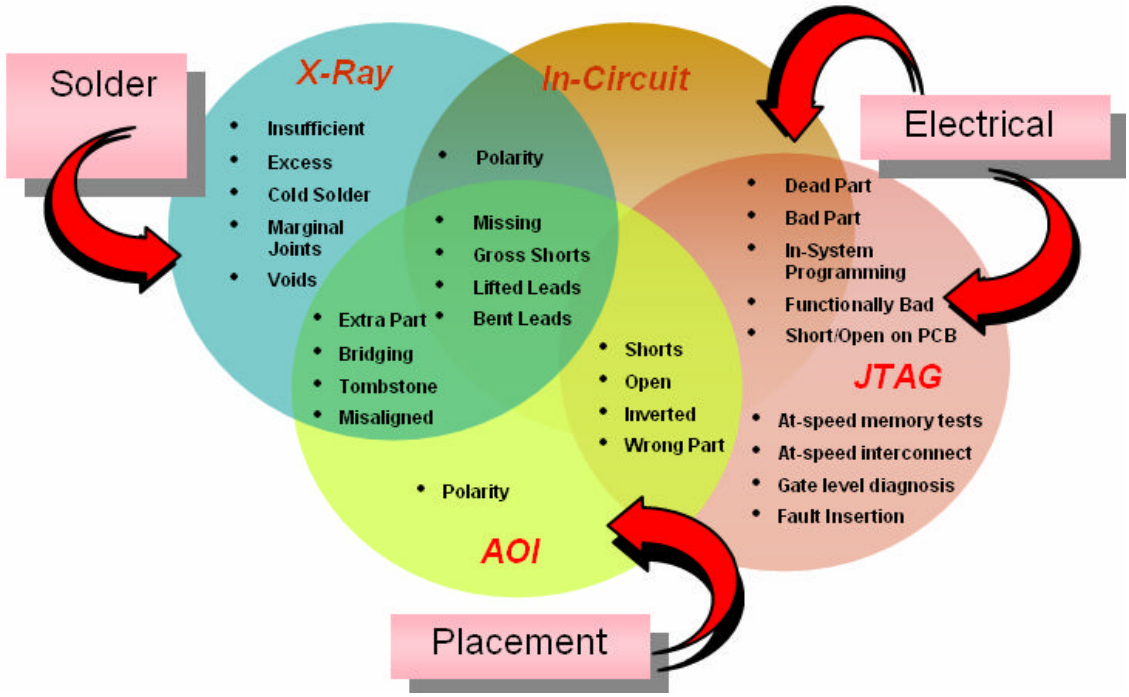

Figure 1 – Alternative Solution

Alternative Methods for Limited Access Testing

In recent years, several alternative test methods to ICT have been adopted by the manufacturing industry to provide complimentary test coverage and help to resolve the testing difficulties associated with complex SMT boards.

These alternative test techniques range from Automated X-ray Inspection (AXI), which has the capability to inspect solder related process problems to Automated Optical Inspection (AOI), which is capable of detecting the presence, or absence of devices and whether devices are misaligned. Provided the AOI system has some form of optical character recognition (OCR) it is also possible to detect that the correct devices are placed.

However, neither of these techniques have the ability to verify that the correct value of passive components has been placed, particularly with the miniaturized resistors and capacitors that are commonly used today, as these devices do not have any form of coding that can be easily detected by OCR. This is a situation that could easily occur if the incorrect component reels were loaded onto the pick-and-place machine and can only be detected by performing a parametric measurement on these components.

This parametric measurement can be achieved with Flying Probe Testers (FPT), which uses a so-called "fixture-less" solution that uses test pads or legs of devices on the BUT for the test probes to contact. However, the latter can cause damage to the legs particularly on fine pitch devices and therefore is not a preferred approach. Due to potentially lengthy test times, FPT can be a useful test technique for low volume products but can become a bottleneck in medium to high volume builds.

The ideal solution for verifying the correct placement of passive devices is of course ICT, however the afore mentioned physical access limitations make it difficult to provide sufficient test pads to measure all passive components as well as cover the digital sections of the BUT. It would be possible to utilize AOI to verify the correct IC's (large enough for part markings) have been placed and are not misaligned, ICT or FPT to verify the correct passive components have been placed and AXI to verify the solder connections but the drawback common to all these systems is the high capitol cost of the test equipment.

In the drive to achieve effective low-cost testing of complex PCB designs, many manufacturers are leveraging the effectiveness of boundary-scan to test digital portions of the BUT coupled with a complimentary test method such as ICT for testing of the remaining analog devices. This requires only a small percentage of circuit physically accessible by test probes, reducing the complexity and ultimately cost of ICT test fixtures or enhancing the coverage achievable with a FPT.

With a boundary-scan production package consisting of hardware and execution software at a fraction of the price of the previously mentioned ATE platforms, several low-cost high-performance test strategies are available.

Impact of Lead Free Soldering on PCB Test and Inspection

The manufacturing test problem is further complicated by the EU directive (WEEE and RoSH), which legislates the total abolition of lead in solder joints by 2006. This directive is forcing electronic manufacturing companies to introduce lead-free soldering within their manufacturing process.

The introduction of a lead-free soldering process will have a varying impact on the utilization of current physical probing test methodologies, such as in-circuit and flying probe, due to[6]:

1. Increase in flux residues, which may lead to probe tip contact resistance build-up requiring:
   - New probe styles
   - More aggressive test fixture cleaning schedules
   - Shorter probe replacement schedules
2. Lead-free brittle solder joints which may be damaged by:
   - Excessive board flexing on test fixtures
   - Sharp probe styles
   - Repetitive probing with flying probe testers

In addition there may be an increase in open and short fault conditions caused by the increased reflow temperatures, currently under investigation by the NEMI "Lead Free Hybrid Assembly and Rework Project". The outcome is that there may be a larger percentage of defective boards requiring rework, which also results in problems caused by potential damage to components and boards, further complicated by the inability of AOI and AXI to inspect manually reworked solder joints.

This will lead to an increase in the implementation of contact-free test methodologies like boundary-scan to determine that products have been manufactured correctly and are free of structural faults.

Fixture-Less Testing Using Boundary-Scan

This paper further examines the utilization of boundary-scan as an alternative complimentary test strategy that:

- Provides high test coverage on complex PCB's
- Short test development cycles requiring minimal test fixturing
- Low cost of ownership
- High diagnostic resolution
- A mechanism for conducting testability analysis prior to PCB layout
- An infrastructure for supporting in-system configuration

Boundary-scan was first proposed in 1985 and became the IEEE 1149.1 standard in 1990, but it was slow to catch on because it required the IC silicon vendors to produce silicon that was compliant with the IEEE 1149.1 standard. Each device must physically include the 4-wire (5-wire if the optional TRST signal is included) Test Access Port (TAP), internal boundary-scan cells for each pin and associated internal boundary-scan registers and additional multiplexing circuitry. In addition, the device vendor must provide Boundary Scan Device Language (BSDL) files that fully describe the boundary-scan architecture.

Initially this was a level of complexity that silicon vendors were unwilling to include and an additional chip cost that customers were unwilling to pay. This has gradually improved due to the problems associated with limited test access, such that silicon vendors have accepted the challenge of fabricating cost-effective boundary-scan compliant devices in order to eradicate the test coverage problems caused by limited test access.

Early adoption of boundary-scan solutions included some in-circuit test equipment suppliers providing this capability within their ICT platforms – a technique referred to as boundary in-circuit test (BICT), which didn't eliminate the need for test points. This solution had limited success, such that the leading ATE suppliers are now establishing relationships with the leading boundary-scan tools providers so that customers can now benefit from the expertise and knowledge already developed in applying boundary-scan tests for product designs, significantly eliminating the need for test points.

A number of factors have contributed to the recent explosion in the use of boundary-scan (IEEE 1149.1) for PCB assembly test and in-system configuration. Clearly, one factor is the ubiquitous availability and deployment of FPGA's, cPLD's, ASIC's, and other "off-the-shelf" boundary-scan compliant devices. As more 1149.1 compliant devices are placed on boards, the test departments are more likely to utilize this technology to improve the board level test coverage.

Further driving the adoption of boundary-scan test strategies within manufacturing groups is the board test environment, which is experiencing higher package densities, smaller traces, high-frequency interconnect requirements and the resulting loss of traditional nodal access. As discussed in the previous sections the digital device complexity of ASIC's and VLSI devices make test coverage from traditional digital in-circuit test much more difficult and costly.

Boundary-scan provides the ideal combination of ease of test generation, potentially high fault coverage, high diagnostic resolution and simple interfacing requirements. Such a combination makes its adoption almost essential for businesses that value high quality products, fast time to market, and lower product development and manufacturing test costs.

By enabling fixture-less test preparation and verification of tests off-line, boundary-scan adopters soon realize that with the availability of low-cost bench-top boundary-scan tools, product design, debug and prototype turn-on are much faster and easier. In this new environment, the use of stand-alone boundary-scan tools within PCB design and prototype verification has become extremely common with the desire to link early-phase prototype tests and programs to the manufacturing test process as shown in Figure 2.

This fixture-less test development strategy can be utilized at each stage throughout the PCB life cycle from early prototype designs to volume production testing.

Further benefits to both design and manufacturing are that boundary-scan can be extended to test designs that contain Multi-Chip Modules (MCM's) and daughter cards either as separate entities or combined within a module. Such system-level test schemes allow multiple boards to be tested within a backplane configuration. See reference[5] for further details.

The boundary-scan architecture provides far more than a test infrastructure; it often provides an access mechanism for in-system configuration of cPLD's and flash memory devices providing that the I/O pins of the flash memory device are accessible via the pins of 1149.1 compliant devices. It can also be utilized to program in-system configurable devices using device vendor specific protocols or the new industry standard IEEE 1532 protocol.

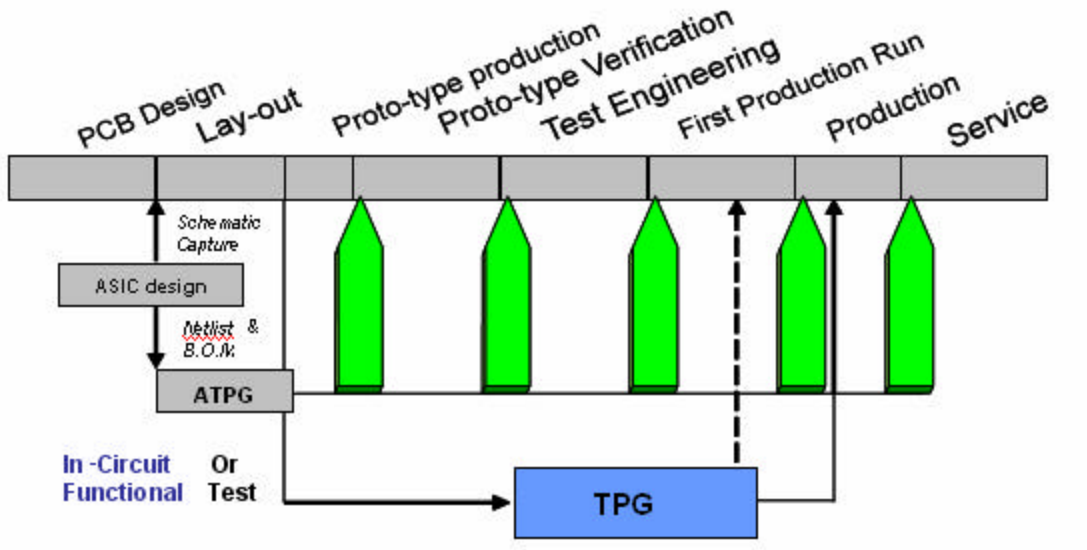

Figure 2 – Test Process

The ability to configure cPLD's and flash memory devices in-system allows boards to be assembled with blank devices, thus removing the logistical problems associated with stocking a large inventory of pre-programmed devices which invariably will end up placed on the wrong PCB. This ability to program devices on-board allows the late configuration of devices in the factory and also provides the capability of upgrading products in the field, eliminating the need to return products to the repair center.

Boundary Scan Principles

The boundary-scan cells on all components within a design are connected serially to form a shift register, which is commonly called a boundary-scan chain. Each end of this chain is connected to a designated Test Data Input (TDI) and a Test Data Output (TDO) pin. A signal called Test Mode Select (TMS) is used to control the sequencing of the finite state machine (FSM) synchronized with the Test Clock (TCK), which is also used to shift data and instructions in and out of the device. A fifth optional signal pin called TRST is used to provide an asynchronous reset of the FSM located within the TAP.

Boundary-scan registers within IEEE 1149.1 compliant devices provide access to more than just PCB traces. In the majority of cases, these traces connect to non-boundary-scan devices such as memory and standard logic. If adjacent boundary-scan devices provide sufficient access to the control and IO pins, these devices or groups of devices can be described as non-boundary-scan clusters and tested using the boundary-scan data register cells of connecting devices to provide the stimulus patterns and capture the resultant response data. In addition the 1149.1 standard allows internal registers other than the mandatory registers to be connected between TDI and TDO.

Because of this feature, boundary-scan has quickly become a data highway, providing access to internal test structures, such as FPGA user-definable registers, processor registers for emulation and address/data registers for in-system configuration as shown in Figure. 3.

The serially connected boundary-scan cells that form the boundary register act as "virtual nails" or "silicon nails" to provide the mechanism for driving test stimulus and capturing signal responses between interconnecting boundary-scan devices using the EXTEST instruction. As shown in Figure 4 the interconnect test performed by using the EXTEST instruction is very thorough.

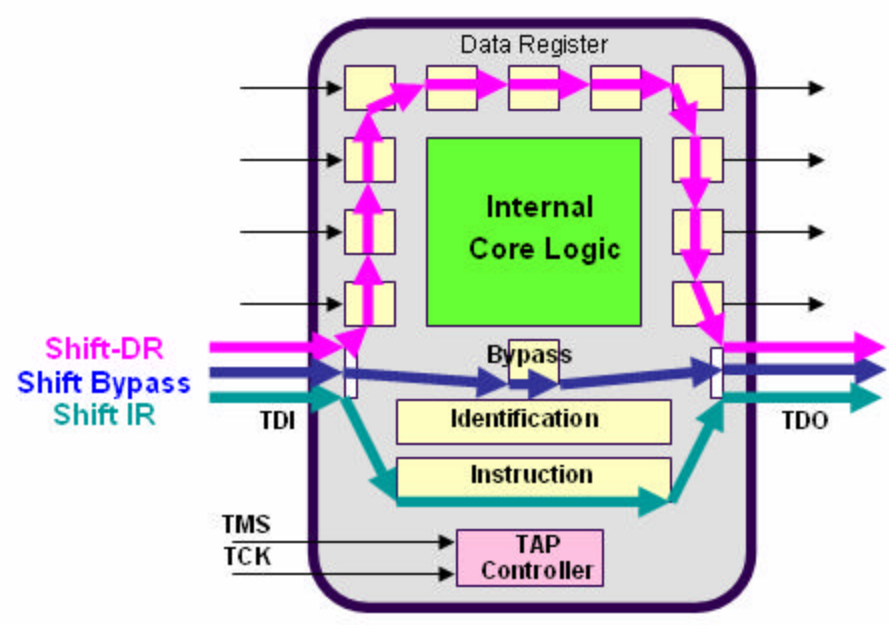

Figure 3 - Boundary-scan Architecture

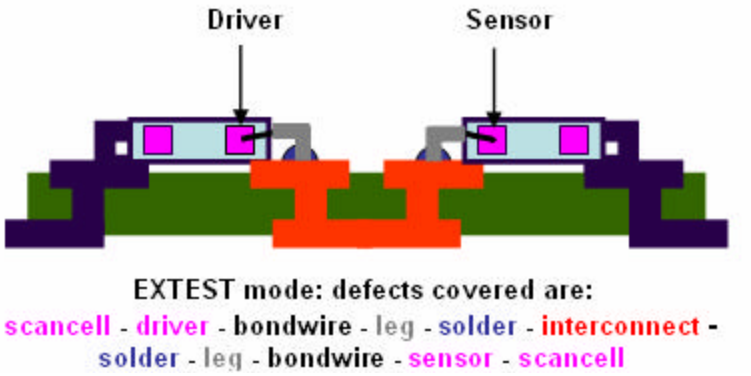

Figure 4 - Boundary-Scan Fault Coverage

Boundary-Scan Integration

A typical PCB manufacturing production line may consist of the process stages depicted in Figure 5, which is comprised of a mixture of inspection and test methodologies that complement each other to ensure that adequate defect coverage is achieved.

As previously discussed in the earlier section entitled: “Alternative Methods for Limited Access Testing”, there is now resurgence in interest particularly amongst the Contract Equipment Manufacturers (CEMs) to integrate third party boundary-scan equipment and software within the commercially available ICT platforms.

However, despite the obvious benefits that boundary-scan and ICT can bring to the test arena, this combination is not ideal for every application. For low volume production it may be more cost effective to use a dedicated boundary-scan tester in conjunction with a flying probe tester used to test passive analog components and other non-scan devices

Alternatively it may be more cost effective to integrate the boundary-scan test capability into a customized Functional Board Tester (FBT) where it could be used to compliment the structural testing provided by FPT, in addition to providing an infrastructure for the in-system configuration of programmable devices.

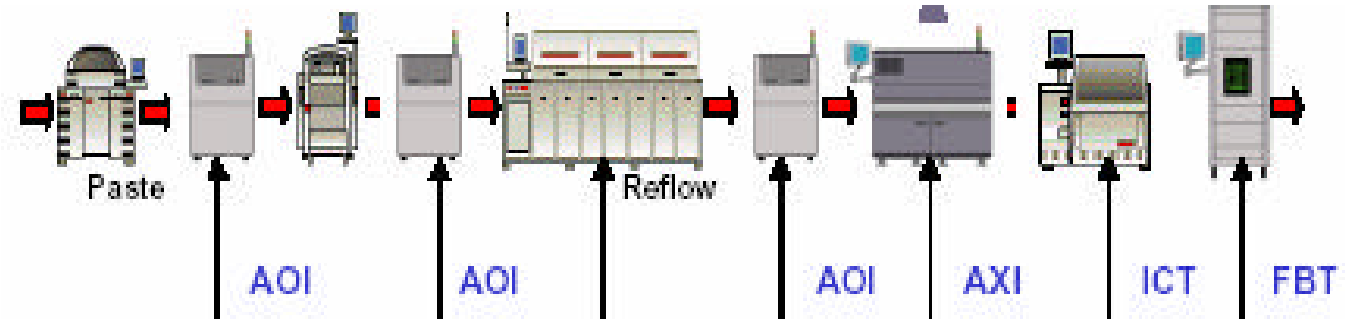

Figure 5 - Production Flow Line

Choosing between the many possible combinations of test and inspection methods depends on several factors including the characteristics of the product to be tested, production throughput requirements and the anticipated fault spectrum. Because boundary-scan and ICT are complimentary test methods, this combination provides an optimal test strategy with minimal cost and the maximum coverage for the anticipated fault types for the majority of complex electronic designs.

JTAG Technologies provides a number of production test migration paths, so that once the tests have been developed off-line using JTAG Technologies development software and validated against a know good version of the target production board, the test execution files can be ported to the chosen test platform as in Figure 6.

These migration paths include:

1. **Stand-Alone –** this test environment utilizes JTAG Technologies' boundary-scan controller hardware and test execution management software on a PC-based test system. The controller interfaces supported are ISA, PCI, USB 1.1 or 2.0, VXI, Ethernet and FireWire.
2. **Functional Test –** to provide a seamless integration into a customer's existing customized FBT test executive, JTAG Technologies provides test execution software for use with C/C++, VB, National Instruments LV, LW/CVI and TestStand, all of which exercise JTAG Technologies' full line of boundary-scan controllers.
3. **In-Circuit Test –** this solution integrates JTAG Technologies' boundary-scan controller and execution software (available in UNIX) within the chosen proprietary ICT test execution environment to provide a seamless integration of boundary-scan and in-circuit tests. Optionally, existing ICT hardware can be used for vector delivery and result collection.
4. **Flying Probe Test –** this solution integrates JTAG Technologies' boundary-scan controller and execution software within the chosen proprietary FPT test execution environment to provide a seamless integration of boundary-scan and flying probe tests. Optionally, existing FPT hardware can be used for vector delivery and result collection.

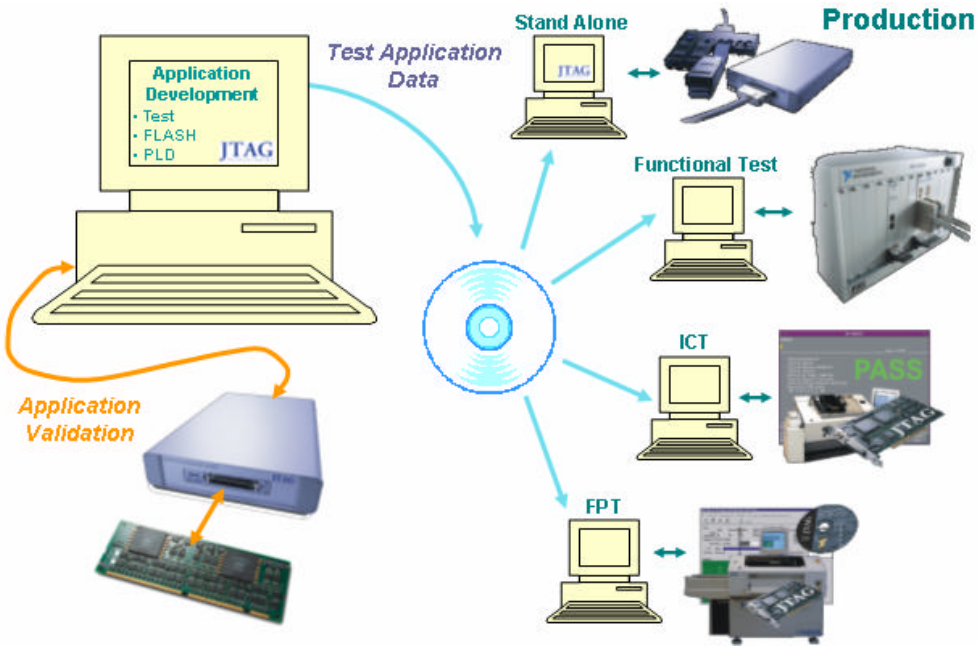

Figure 6 - Test Environment Integration

By combining boundary-scan and ICT or FPT the need to introduce an additional test stage to fully automated flow lines is eliminated. Consequently, additional operator training is not necessary as boundary-scan test and programming applications are launched from the familiar native test executive and results reported in a consistent format with other test activities.

In order to optimize configuration times for devices such as cPLD's and flash memories many would prefer to utilize dedicated boundary-scan controllers optimized for device configuration via boundary-scan to be installed in the ICT or FPT. On the other hand, if device configuration is not a requirement the compilation of boundary-scan applications targeting the ICT or FPT hardware for vector delivery may be desired to avoid the need for additional hardware.

The boundary-scan test development process remains the same independent of the vehicle chosen to deliver the vectors for full-scale production, dedicated hardware or host ATE hardware. This allows tests to be developed and debugged on a bench-top tester, used for prototype test and debug and at a later time integrated in the most efficient point in the test process.

Importing Legacy Boundary-Scan Tests

The ability to deploy test vectors from a single boundary-scan test development seat to any number of test platforms affords process and test engineers a great amount of flexibility when streamlining product test flow by allowing the execution of boundary-scan applications to be easily relocated. For instance, prototypes may be tested on a FPT, stand-alone boundary-scan tester and finally FBT. Once the design is verified and considered stable, the role of the FPT may be assumed by ICT as well as initiation of the boundary-scan applications resulting in the reduction of a test stage.

As described above it may be strategically advantageous or even necessary to relocate boundary-scan test execution from one platform to another or to another vendor's equipment. This can become a significant engineering effort in the event tools specific to that platform developed the boundary-scan applications. To aid in this migration JTAG Technologies has developed import utilities that compile third party test files such as SVF to formats supported by JTAG Technologies hardware and software eliminating the need to duplicate past development efforts.

This capability can be invaluable in the effort to standardize on tool vendors, eliminating a high mix of equipment in the test environment, which requires knowledge of several different systems.

Conclusion

Nobody is underestimating the problems within the manufacturing industry associated with testing the complex range of products, many containing BGA and CSP devices. There is no one solution and the majority of the manufacturing flow lines will use a number of complimentary test/inspection methods to resolve the structural test problem.

There is no doubt that boundary-scan has made a considerable contribution in resolving the test access problems introduced by the widespread use of BGA devices placed on both sides of PCB designs resulting in a significant reduction in PCB real estate to place test pads.

Since IEEE 1149.1 became a standard in 1990, boundary-scan has matured as a technology and is now widely accepted as a manufacturing structural test method. It is the only way to verify the electrical connectivity between BGA packages by conducting interconnect tests between boundary-scan devices and has substantially contributed to reducing the cost of test development and reducing lead-times for deploying test solutions.

Boundary-scan is extensively used within design departments for testing early prototype designs and in particular for the in-system configuration of cPLD, FPGA and flash memory devices with minimal fixturing required. This allows tests initially developed during the design verification phase to be ported to an existing ATE platform in the manufacturing environment, significantly reducing test engineering development efforts and utilizing engineering resources more efficiently.

Manufacturers of complex PCB's are now realizing the substantial benefits of integrating boundary-scan as a complimentary test method into existing test platforms to compensate for limited physical access and deliver a comprehensive low cost test solution.

The availability of many production test migration paths provides the necessary flexibility to meet the varying requirement of today's manufacturing environment. Furthermore, the ability to import legacy test vectors and the flexibility of a non-captive test solution allows existing automatic flow lines to be retrofitted or streamlined without redevelopment of boundary-scan applications or impact on performance.

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