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Reliability of CCGA and PBGA Assemblies

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Abstract
Area Array Packages (AAPs) with 1.27 mm pitch have been the packages of choice for commercial applications; they are now starting to be implemented for use in military and aerospace applications. Thermal cycling characteristics of plastic ball grid array (PBGA) and chip scale package (CSP) assemblies, because of their wide usage for commercial applications, have been extensively reported on in literature. Thermal cycling represents the on-off environmental condition for most electronic products and therefore is a key factor that defines reliability.

However, very limited data is available for thermal cycling behavior of ceramic packages commonly used for the aerospace applications. Thermal cycles and vibration test results for ceramic ball grid array (CBGA) with 361 and 625 I/Os were reported previously by this author and the trends for cycles-to-failures for four different temperature ranges were established. This paper presents thermal cycle test results for a ceramic column grid array (CCGA) and its PBGA version, both having 560 I/Os, exposed to two different thermal cycle regimes. One of the thermal cycles was that specified by IPC 9701, i.e. –55 to 125°C; the other was in the range of –50 to 75°C representing the qualification for the specific mission. Per IPC 9701, test vehicles were built using daisy chain package and were continuously monitored. The effects of many processing and assembly variables including corner staking, commonly used for improving resistance to mechanical loading such as drop and vibration loads, were also considered as part of the DOE test matrix. Optical photomicrographs were taken at various thermal cycle intervals to document damage progress and behavior. A representative samples of these along with cross-sectional photomicrographs at higher magnification taken by scanning electron microscopy (SEM) to determine crack propagation and failure analyses for packages with and without corner staking are also presented.

Key Words: ball grid array, BGA, PBGA, thermal cycle, stake, solder joint, column grid array, CCGA, CGA, inspection

Introduction

Advanced IC electronic packages are moving toward miniaturization from two key different approaches, front- and back-end processes, each with their own merits and challenges. Successful use of more of the front-end processes for the back-end packaging, e.g. microelectromechanical systems (MEMS) and Wafer Level Package (WLP), enable further reduction in size and cost. Direct flip-chip die attachment has become the most efficient approach for the 2nd level assembly. If and when the die can be easily screened to produce high yield known-good die, high density boards can be fabricated at low cost to accommodate high I/O with finer pitches, and defects associated with fine pitch 2nd level assembly are minimized. Wafer level packaging solves the known-good die issue by enabling ease of die testing in a package style, but they have other concerns including the I/O limitation, additional cost, and lack robust reliability. From the back-end approach, system-in-a-package (SIAP/SIP) development is a response to an increasing demand for package and die integration of different functions into one unit to reduce size, cost, and improve functionality.

BGAs and CSPs (chip scale package) are now widely used for many electronic applications including portable and telecommunication products. SIP development is the most recent response to further increasing demand for integration of different functions into one unit to reduce size and cost and improve functionality. The BGA version has now started to be widely implemented for high reliability applications with generally more severe thermal and mechanical cycling requirements. The plastic BGA version of the area array package, introduced in the late ‘80’s and implemented with great caution in the early ‘90’s was further evolved in the mid ‘90’s to the CSP (also called fine pitch BGA) with a much finer pitch to 0.4mm. Now, distinguishing between size and pitches has become difficult for the array packages.

These packages with balls/columns underneath and irrespective of the die/package ratios are now categorized as area array packages in order to be able to distinguish them from the flip chip bare die category. Bare dies have been around for a longer time, but their associated issues- including known good die and difficulty in direct attachment to printed wiring boards (PWB)- have limited their wide implementation. Wafer level packages were introduced several years ago to address the key issues of bare die and take the advantage of package ease of testing and handling. As PWB technology with finer features becomes widely available with lower cost, bare die becomes more attractive.

Extensive work has been carried out by the JPL consortia in understanding technology implementation of area array packages for high reliability applications. These included process optimization, assembly reliability characterization, and the use of inspection tools, including X-ray and optical microscopy, for quality control and damage detection due to environmental exposures. Lessons learned by the team have been continuously published.[1-5]

This paper will first provide a summary of most recent assembly reliability data presented in literature for the I/Os from 256 to 1849 and pitches to 1mm for plastic BGAs. Then, it will provide details on design and assembly of the experimental test vehicles including the design of printed wiring board (PWB) and solder paste print efficiency using automatic and manual printing. Manual printing using mini stencil was needed in order to have much higher localized solder paste print for CCGAs. Failure mechanism changes due to two different maximum thermal cycle temperatures for the CCGA and PBGA are compared. Finally, thermal cycle data and cross-sectional photomicrographs for these packages under two different thermal cycle regimes are presented.

Literature Review on 2nd Level PBGA Reliability

Area arrays come in many different package styles. Examples of typical area array packages are shown in Figure 1. These include plastic ball grid array with ball composition of eutectic 63Sn/37Pb alloy or its slight variation. The ceramic BGA package uses a higher melting ball (90Pb/10Sn) with eutectic attachment to the die and board. Column grid array (CGA or CCGA) is similar to BGA except it uses column interconnects instead of balls. Flip chip BGA (FCBGA) is similar to BGA, except it is internal to the package and flip chip die is used.

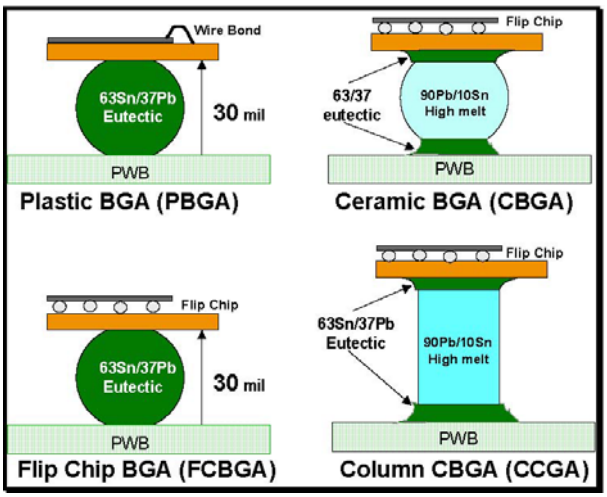

Figure 1 - Plastic and Ceramic Package Configurations

Three package configurations are popular. These are:

- Full array.
- Staggered array.
- Peripheral array.

Plastic packages come in all styles whereas ceramic package are limited to generally full array configuration. Fully populated BGA packages presents some significant routing challenges if conventional printed wiring board with plated through-hole (PTH) vias are considered for the design. The staggered grid BGA uses only half of the available sites and therefore, similar to peripheral arrays, eases routability. A staggered grid pattern of 1.27 mm pitch package provides an effective minimum pitch of 1.8 mm along the diagonal of the package.

A peripheral array format for plastic packages, with the die at the package center, was developed to increase thermal cycle reliability as well as to ease routability. Premature failures of solder joints under the die, due to a large CTE mismatch between the die and PWB, have been observed. Removal of the center solder balls; however, will slightly degrade thermal performance (θ_{ja}) of the package. To improve thermal dissipation, generally, a number of nonfunctional thermal balls are added to the middle of package.

Peripheral packages have been developed to reduce solder joint failures at the die edge as well as to improve routability characteristics. However, for ceramic package there is a lesser need for peripheral array because the CTE mismatch between die and package material is negligible. Most ceramic packages are supplied in full array configuration. The CCGA used in this investigation; however, was a peripheral array.

Die size in the plastic package is an important factor influencing solder joint performance. Experimental results indicate that solder joints close to the perimeters of the die fail first under temperature cycling. It has been shown that the number of cycles-to-failure is not only sensitive to the I/O counts, but also to the die size. The significant CTE differences between ceramic die (2.3 ppm/°C) and the PWB (about 15 ppm/°C) and encapsulating epoxy (> 70 ppm/°C) are the key contributing factors to the failures associated with the die.

Table 1 lists cycles-to-failure for a number of plastic packages with different configurations, selected from those reported in literature. Data were chosen to be able illustrate the effects of a few key parameters on reliability. The following parameters were considered when test data were tabulated even though in some cases specific information was not reported and is missing.

- Thermal cycle range, ramp rate, dwell times
  - For example, the CT1%F (cycles-to-one percent-failure) for PBGA 256 in the range of 0/100°C was 3200 cycles (Case #2); it reduced to about 2000 cycles when the temperature range increased to – 40/125°C (Case #11)
- Package size, thickness, configuration, and I/Os
  - For example, compare Case#2 to Case#3, a small reduction in cycles-to-first failure is shown when package I/O increased from the 256 I/Os, 1.27 mm, to 1849 I/Os (3200 vs 3095 cycles in the range of 0 to 100°C). A slightly higher reduction is shown when another test results for the 256 I/Os (Case #11) package with 1.27 mm pitch is compared to the 1156 I/Os (Case #13) with 1.0 mm pitch, 2000 vs 1601 cycles in the range of –40 to125°C.
- Die size and its relation to the package size and ball configuration
  - This is not apparent from the cases presented in the Table 1, but the die and package sizes are listed in the table for the purpose of identifying such a correlation. It is shown that as the die size increased, the cycles-to-failure decreased. Comparing Case #7 and 8, it shows an increase in cycles-to-failure when die size increased. The opposite effect shown here might be due to the confounding effects of heat sink addition for the Case #8.
- PWB thickness, definition of pad, surface finish
  - Preferred thickness was defined as 2.3 mm in IPC 9701[6] since it is known that generally packages assembled on thinner PWBs show higher cycles-to-failure. So, comparing Cases #4 and #5, one may conclude that one reason that PBGAs with 676 I/Os shows higher thermal resistance than ones having 256 I/Os, possibly is due to the use of thinner board for the 676 I/O package assembly.
- Single side or double side, relative offset of package on top and bottom
  - This is not shown here, but discussed by this author in another paper.[7]

Table 1 - Cycles-to-Failure Data Illustrating the Effect of a Number of Key Variables

Case Number	Package (I/O, Pitch)	Pkg Size (die size) mm	Thermal Cycle Condition (ramp, dwell, Cycle/hr)	First Failure	Mean Life(N6 3.2%)	Comments
1	PBGA-119-1.27	27x27 (17.8x17.8x0 .3)	0°C/100°C (10 min, 5 min,2)	6260 (1% failure)	12215	27 Pkg Ref[8]
2	PBGA-256-1.27	27x27 (10x10)	0°C/100°C (10 min, 5 min,2)	3200 (1% failure)	(6195)	Ref.[9]
3	FCBGA-1849-1. 27	??	0°C/100°C	3095 (1% failure	4710	Ref[12]
4	PBGA-256-1.0	17x17 (8.80x7.9)	0°C/100°C (10 min, 5 min,2)	3687 (1 % failure)	NA	Full Array PWB, 2.3 mm Thk Ref Altera[10]
5	PBGA-676-1.0	27x27 (17.8x17.8x0. 3)	0°C/100°C (10 min, 5 min,2)	5909	9267	15/32 Fail, PWB, 1.6 mm Thk[11]
6	SBGA-860-1.0	42.5x45.5 (22.45x21.44x 0.3)	0°C/100°C (10 min, 5 min,2)	> 8824	N/A	0/32, No failure to 8824 cycle, PWB 1.6 mmThk[11]
7	FCBGA1020-1.0	33x33 (22.6x19.9)	0°C/100°C (2 cycles/hr)	5670 (1% failure)	NA	PWB Thk 2.3mm 6 layer build up BT[10]
8	FCBGA1020-1.0	33x33 (17.9x16.7)	0°C/100°C (2 cycles/hr)	2770 (1% failure)	NA	PWB Thk 2.3mm 6 layer build up BT+ Cu heat sink[10]
9	PBGA-1156-1.0	35x35 (23.11x21.13x0.3)	0°C/100°C (10 min, 5 min,2)	7289	9350	8/32 Fail, 1.6 mm Thk Ref Xilinx[11]
10	PBGA-313- 1.27	35x35 (13x13)	-30°C to 100°C (25 min, 15 min, .75)	3310 (1% failure)	4000	13 Pkg[13]
11	PBGA-256-1.27	27x27 (10x10)	-40°C-125°C (15 min, 15min, 1)	~2000 (1% failure)	(3164)	Ref[9]
12	PBGA-676-1.0	27x27 (17.8x17.8x0. 3)	-40°C-125°C (15 min, 15min, 1)	1341	1830	27/32 Fail, PWB 1.6 mmThk[11]
13	PBGA-1156-1.0	35x35 (23.11x21.13x 0.3)	-40°C-125°C (15 min, 15min, 1)	1601	2386	30/32 Fail, PWB 1.6 mm Thk[11]

Objectives

The purpose of this investigation was to characterize the reliability of area array packages with 560 I/Os. This included ceramic column grid array and its plastic counterparts with the same peripheral package configuration. A designed experiment was utilized to cover many aspects that are considered to be unique for the potential use of these packages. Solder joint reliability is affected by many variables as briefly discussed in the previous section. The following parameters were either characterized or evaluated as part of the DOE implementation.

- Two pad design, one for PBGA and larger pads for CCGA attachment. PBGAs were assembled on both pad sizes to evaluate PBGA interchangeability with CCGA
- Two stencil designs, one for PBGA and a thicker mini stencil for the CCGA. Solder paste print volumes were measured and their variation shown in graphs.
- Assemblies without and with corner stake adhesive bonds. Corner adhesive bonds are used to improve resistance to mechanical vibration and shock.
- Added heat straps to the top of PBGAs to determine bonding attachment durability of the heat strap. The assemblies were subjected to two types of thermal cycles. The process and results for PBGA package assemblies are discussed in the following.

Test Vehicle
Polyimide printed wiring board (PWB) was designed to accommodate two pads configuration, one for PBGA and the other for column grid array. The pad size for PBGA was 24 mils whereas for CGA was 33 mils attached with traces to plated through hole, (PTH) vias with 24 mil diameter. The specific pairs of pads were connected through PTH such that these and those connections within a package pair complete a daisy chain to be used for monitoring. Four daisy chains for each package were used for continuous monitoring. Four additional pads were added at each side of the package for manual probing and failure identification to a narrower region after failure detection thorough continuous monitoring.

Similarly, two daisy chain sets, each with three rows, using PTH vias representative of the test design were added to monitor behavior of PTHs during thermal cycling. Continuity of these PTH daisy chain were performed by hand at each interval when assemblies were removed from the chamber for inspection. PWB's pads had HASL (Hot Air Solder Level) surface finish. HASL and OSP surface finishes are specified in IPC 9701 as the recommended surface finishes for solder attachment reliability evaluation. The key reason for such recommendation is to avoid potential immature intermetallic failures such as those occasionally observed for the Au/Ni surface finish. Because of space availability, additional parts such as leaded and leadless package and capacitors were added in order to assess their reliability; these are not discussed in the paper. Figure 2 shows the top and bottom of the board design showing daisy chain configurations for package, probing pads, and PTH vias.

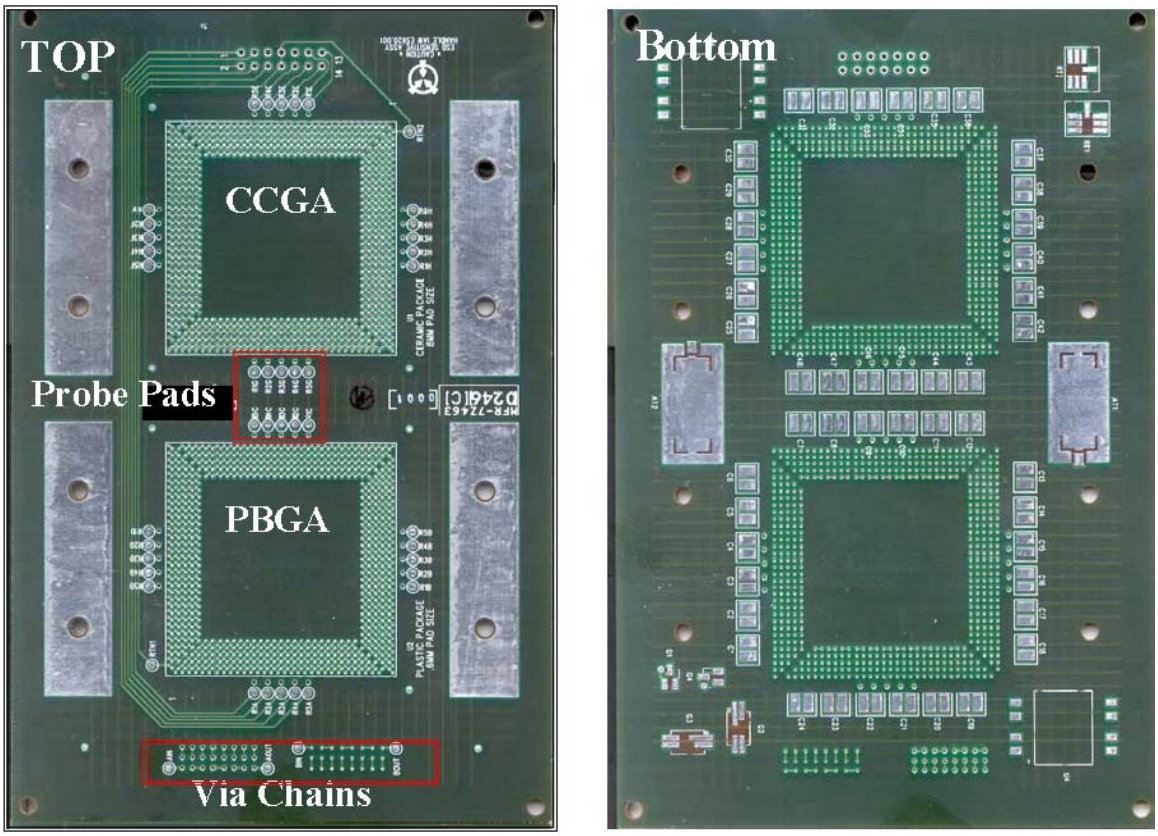

Figure 2 - Printed Wiring Board Design Showing Package Daisy Chain, Probing Pads, and Via Daisy Chains

Stencil Design, Paste Print, and Volume Measurement
Because of two solder volume requirements, two stencil types with two different thicknesses were used to meet optimized solder paste volume for each part assembly. Table 2 lists solder paste volumes that can be achieved with different stencil thicknesses and aperture openings. The 7 mil stencil thickness represents the general stencil that could be used for paste application on PBGA and other package pad patterns. The mini stencil with 10.5 mil thickness was used only for the manual paste print application in order to achieve the higher paste volume recommended by the CCGA package supplier. Previously, it was shown that higher solder paste volume could improve reliability of CBGAs (ceramic ball grid array) and CCGAs with 1.27 mm pitches.

Table 2 - Stencil Parameter and Solder Volume

Stencil Thickness	Solder volume (mil)3	Option
BGA-Aperture 23 mil-Stencil 7mil	2909	Stencil
BGA-Aperture 24 mil- Stencil 7 mil	3168	No
CGA-Aperture 32 mil dia-stencil 7 mil	5632	Stencil
CGA-Aperture 33 mil dia-stencil 7 mil	5990	No
CGA-Aperture 32 mil dia- stencil 10.5 mil	8448	Mini stencil

An RMA paste, type III (-325+500) mesh was used for paste printing using automatic and normal manufacturing parameter setup for the case of 7 mil stencil thickness. Manual paste printing was performed when the mini stencil was used. Each paste print on PWB was visually inspected after printing for gross defects such as bridging or insufficient paste. Paste print quality was improved when needed by adding solder paste when insufficient or removing bridges for bridging conditions. Solder paste heights were measured using a laser profilometer. Measurement was carried out at 16 locations as well as corner and center pads, to accumulate solder volume data and their distributions.

Figure 3 shows plots of solder volume distribution for two different stencil thickness (7 and 10.5) and pad opening for the 7 mil stencil thickness. Note the solder paste height measurement was done relative to the PWB surface rather than the Cu pad when made manually; therefore, the heights are a Cu thickness higher than their actual values. No adjustments were made when the solder volume was calculated based on the height and the pad diameter. Figure 2 shows distributions of solder volumes for the 16 locations. It is apparent that mini-stencil produced a wider distribution in the solder paste volume that can be achieved through automatic printing. Improvement in distribution was improved slightly after a 2nd manual printing, but distributions are still much wider than in the automatic version.

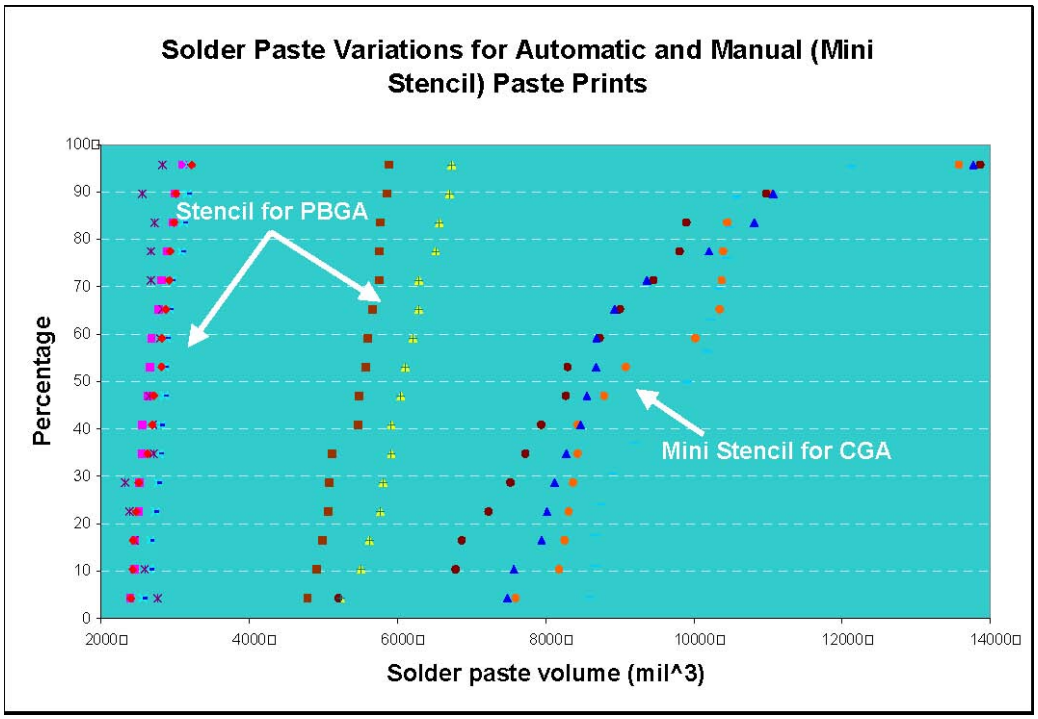

Figure 3 - Paste Volume Variations and the Effect of Automatic and Manual Using Mini Stencil for printing

Designed experiment for Assembly
The objectives and parameters considered in designed experiment were discussed previously. Figure 4 shows an assembled test vehicle having both PBGA and CCGAs.

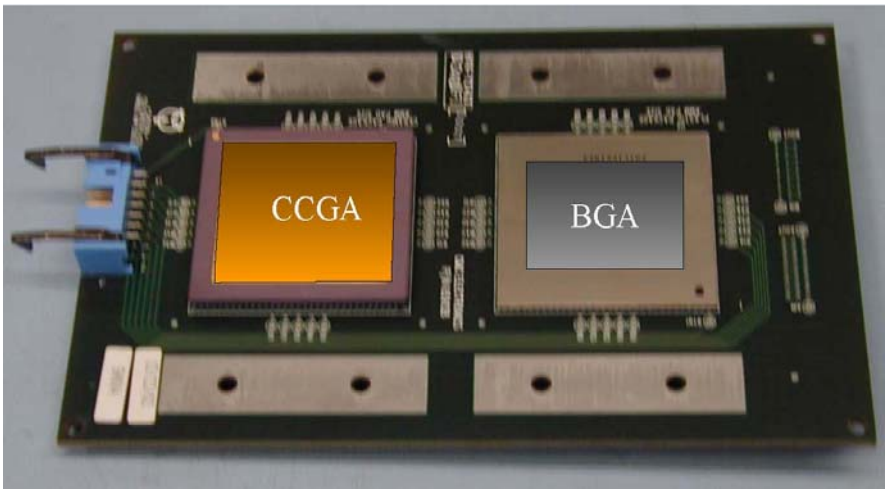

Figure 4 - A Representative of the Test Vehicle Assembly Showing Ceramic and Plastic Packages

Inspection before Environmental Tests
For high reliability electronic application, visual inspection is traditionally performed by Quality Assurance Personnel at various levels of package and assembly. Solder joints are inspected and accepted or rejected based on specific sets of requirements. Further assurance is gained by subsequent short-time environmental exposure, by thermal cycling, vibration, and mechanical shock, etc. These screening tests also allow detection of anomalies due to workmanship defects or design flaws at system level. For space application, generally 100% visual inspection is performed at prepackage prior to its closure (precap) and after assembly prior to shipment.

Visual inspection provides some usefulness for the area array packages, but no value for the hidden balls and columns under the package. X-ray inspection is needed for area array packages even though for CCGAs, the hidden solder joint could not be distinguished because of the heavy ceramic lid that inhibited X-ray penetration.[7] Visual inspection has a higher value for CBGA and CCGA assemblies since generally the solder fails at the exposed corners or periphery ball attachments. Peripheral balls and columns were inspected visually using an optical microscope at the start and during thermal cycling to document damage progress. Figure 5 shows photomicrographs of solder joints of PBGA and CCGA assemblies prior to thermal cycling.

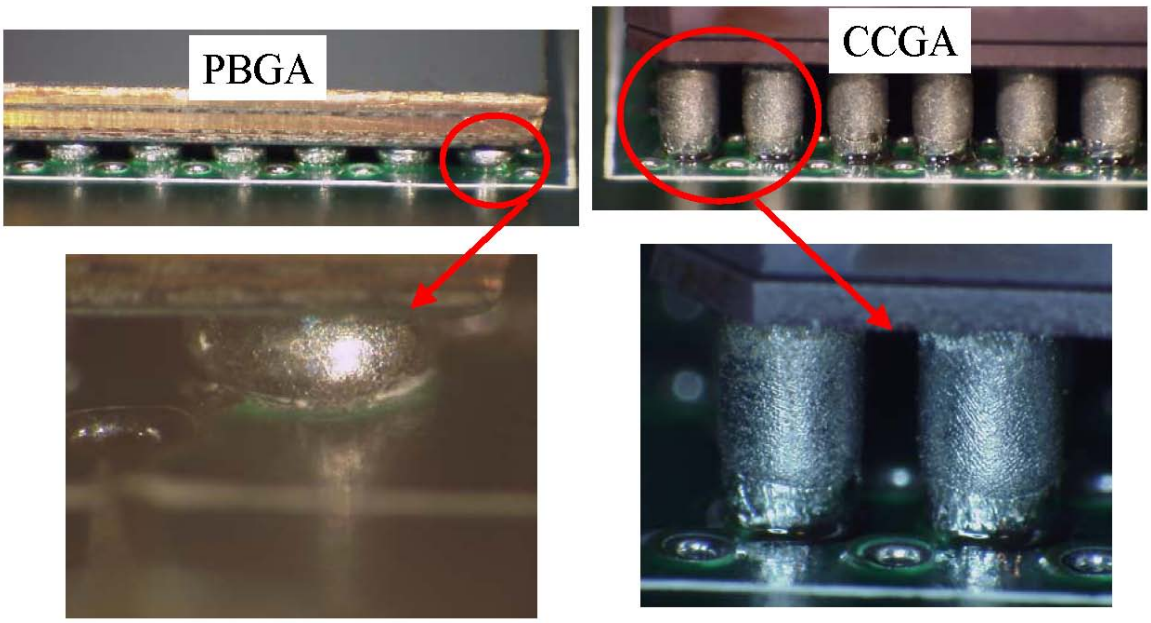

Figure 5 - Optical Photomicrographs of PBGA and CCGA after Assembly

Thermal Cycle Test

An industry-wide guideline document, IPC SM785, for accelerated reliability testing of solder attachment has been around for more than a decade. Only recently, industry agreed to release an industry-wide specification, IPC9701, in response to BGA and CSP technology implementation.[6] The IPC SM785 guideline, although very valuable and still valid, did not answer the key question of what the data means in terms of product application and data comparison. As is well established by industry and the JPL Consortia,[1-5] many variables could be manipulated to either favor or disfavor test results.

Also, in some cases, considerable resources and time could be wasted to generate failure data not related to solder attachment. An example is the use of a surface finish having the potential of inducing intermetallic rather than solder joint failure. This is especially likely for a novice user/supplier.

The IPC 9701 specification, addresses how thermal expansion mismatch between the package and the PWB affects solder joint reliability. In order to be able to compare solder joint reliability for different package technologies, PWB materials (e.g., FR-4), using a relatively larger nominal control thickness to minimize bending (0.093"), surface finish choice to eliminate intermetallic failure (OSP, HASL), pad configuration to eliminate failure due to stress riser (non solder mask defined), and pad size to have a realistic failure opportunity for package/PWB (80%-100 package pad), etc. were standardized in order to minimize their effect on the test results.

The thermal cycle (TC) test ranges, test profile, and the number of cycles (NTC) reported were also standardized. These include the reference cycle in the range of 0 to 100° C (TC1) and a severe military cycle condition of –55 to 125°C (TC4). Three out of five total TC conditions are identical to the test conditions recommended by JEDEC 22 Method A104, Revision
A. The NTC varied from a minimum value of 200 cycles to a reference value of 6,000 cycles.
Two different thermal cycle profiles were used. One is the same range specified by IPC9701 and the other one was specific to the mission specific thermal cycle range requirement. These were:

- Cycle A: The cycle A condition ranged from –55 to 125 °C with 2-5°C/min heating/cooling rate. Dwell at extreme temperatures were at least 10 minutes with duration of 159 minutes for each cycle.
- Cycle B: The cycle B condition ranged from –50 to 75°C with 2-5°C/min heating/cooling rate. Dwell at extreme temperatures were at least 10 minutes with duration of 105 minutes for each cycle.

The criteria for an open solder joint specified in IPC 9701 were used as guidelines to interpret electrical interruptions. Generally, once the first interruption was observed, there were many additional interruptions within 10% of the cycle life.

This was especially true for the ceramic packages. Open was verified manually after removal from the chamber at the earliest convenient time.

Test Results

Figure 6 shows optical photomicrographs of both PBGA and CCGA after 2973 (-50/75°C) and 478 (-55/125°C) thermal cycles. There is no apparent degradation of the solder joints for both PBGA and CCGA for the B condition where maximum temperature was only 75°C. Even though, most of CCGA assemblies had failed by this cycle; however, the board solder joint interconnects appear to be similar to the pristine condition shown previously in Figure 4. The failures were from package side within package and interposer where it is not visually apparent and cannot be inspected easily. The solder joints at the board interface showed insufficient solder with graininess for the case where the maximum temperature was 125°C. To the best of the author knowledge, this feature is not reported in the literature. This author has observed similar changes when solder joints of like nature were exposed to a thermal cycle with a 100°C maximum temperature. The PBGA balls exposed to a similar maximum temperature condition did not show this reduction in solder volume.

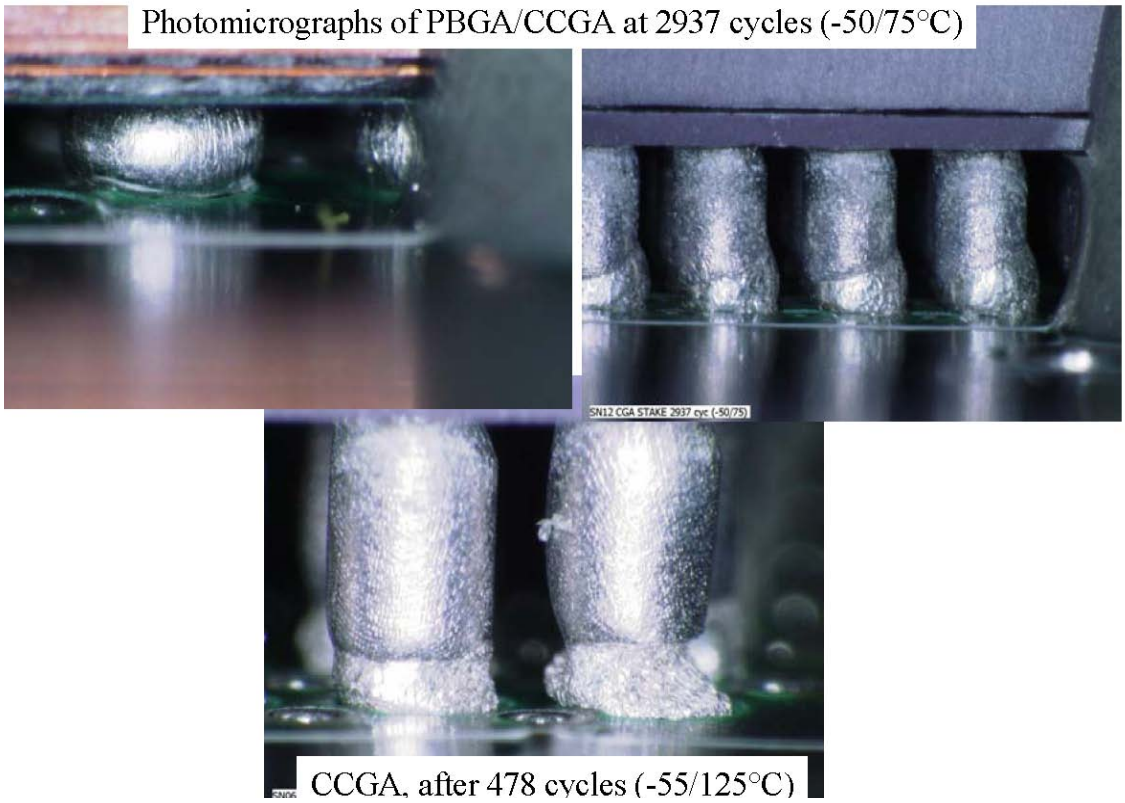

Figure 6 - Optical Photomicrographs of PBGA and CCGA under Two Different Thermal Cycle Conditions
Note graininess and solder volume reduction for CCGA exposed at 125°C

Figure 7 shows an SEM photomicrograph of a PBGA ball after exposure to 583 cycles in the range of –55/125°C. This figure also includes cross-sectional photomicrographs both at low and much higher magnifications. A small microcrack was initiated in the solder joint at the package interface. This photo also clearly shows the grain growth due to exposure to elevated temperature. This assembly was not staked at corners. A representative of PBGA package assembly cross-sectioned after 1819 cycles (-55/75°C) is shown in Figure 7. There is no significant damage or degradation due to such a large number of thermal cycles. Figure 8 shows photomicrographs of a daisy chain via after 1819 condition B cycles. Except for localized microcracks, most PTH vias appear to have no signs of damage.

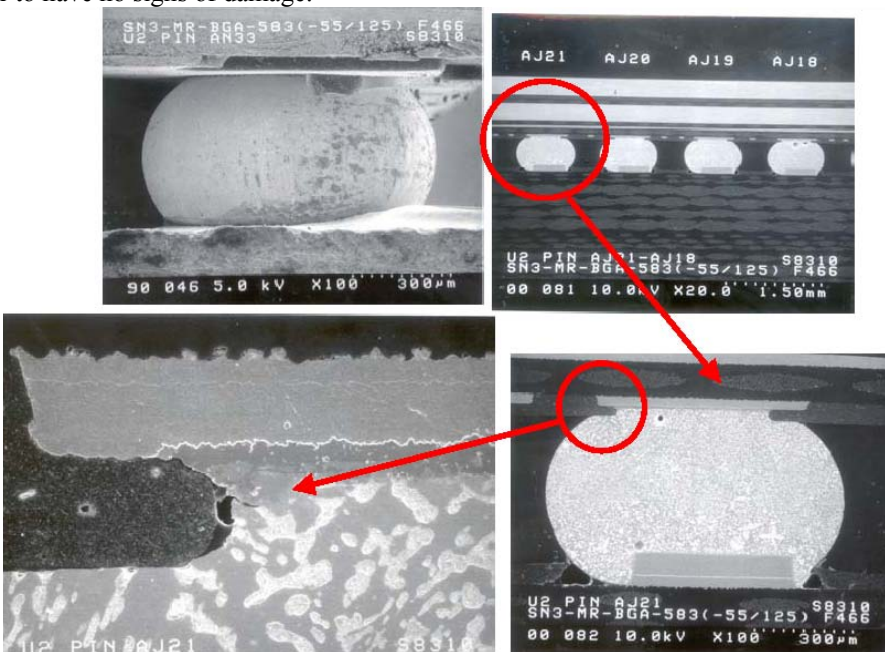

Figure 7 - SEM Photomicrographs before and after Cross-Section for PBGA Package after 583 cycles (-55/125°C)

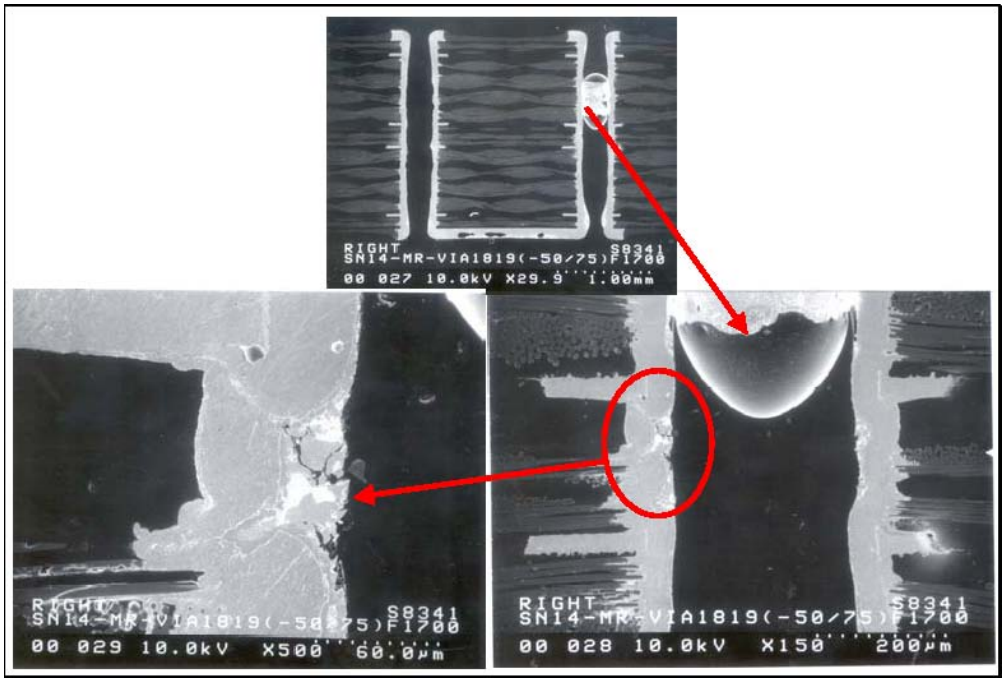

Figure 8 - Photomicrographs of PTH Vias

Conclusions

It is well established that generally solder joint reliability of plastic packages on polymeric boards is better than that of their ceramic counterparts. This was shown through this study and in addition the effects of the following parameters are also identified for the two PBGA and CCGA packages.

- Plastic package did not show failures to 2,000 cycles whereas CCGA version showed failure at slightly above 1,000 cycles when they were subjected to –50/75°C thermal cycle
- No additional degradation was identified due to adding corner adhesive stake to the PBGA package.
- CCGA solder joints at the board interface showed signs of graininess and reduction in solder volume when they were exposed to thermal cycling with a maximum temperature of 100 or 125°C. This was not the case for the PBGA solder joints or when CCGA assemblies are exposed to a maximum temperature of 75°C.
- One of the daisy chain vias showed a resistance increase at about 1500 cycles (-50/75°C), microsectioning at 1819 cycles showed signs of local microcracks without penetration to the PTH thickness in one of the vias.

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References

1. Ghaffarian, R., "*Shock and Thermal Cycling Synergism Effects on Reliability of CBGA Assemblies*", 2000 IEEE Aerospace Conference Proceedings, 2000, p327
2. Fjelstad, J., Ghaffarian, R., Kim, YG., *Chip Scale Packaging for Modern Electronics* (Electrochemical Publications, 2002)
3. Ghaffarian, R., "Chip Scale Package Assembly Reliability", Chapter 23rd in *Area Array Interconnect Handbook* (Kluwer Academic Publishers, edited by Karl Puttlitz, Paul Totta, 2002)
4. Ghaffarian, R., "BGA Assembly Reliability", Chapter 20, *Area Array Packaging Handbook* (McGraw-Hill Publisher, Ken Gilleo, Editor)

5. Ghaffarian, R., ”Comparison of X-ray Inspection Systems for BGA/CCGA Quality Assurance and Crack Detection,”, IPC APEX Proceedings, 2002
6. IPC 9701,”Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments”. Published by IPC, Association Connecting Electronics Industries
7. Ghaffarian R., Kim, N., “How underfill and Double-Sided Affect CSP Assembly Reliability,” http://www.reed-electronics.com/semiconductor/article/CA73744?pubdate=7%2F1%2F2000
8. Mawer, A. and Luquette, L. (1997),"Interconnect Reliability of Ball Grid Array and Direct Chip Attach", *IRPS 1997 Tutorial.*
9. http://www.amkor.com
10. http://www.altera.com
11. http://www.xilinx.com
12. Shiah, A.C., Zhou, X.,”A Low Cost Reliability Assessment for Double-Sided Mirror-Imaged Flip Chip BGA Assemblies”, The Proceedings of Pan Pacific Conference, Surface Mount Technology Association, 2002
13. Evans, J.W, Evans, J.Y., Ghaffarian, R., Mawer, A., Lee, K., Shin, C., “Monte Carlo Simulation of BGA Failure Distributions for Virtual Qualification”, ASME, Hawaii, 1991