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3-Dimensional Partitioning of Printed Circuit Design for High Speed Interconnections

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Abstract
When using standard approaches to PCB design and manufacture, there are a number of different elements that can impact signal integrity at high data rates including: inconsistencies in dielectric properties, inconsistencies in trace width, variation in circuit spacing, uneven copper thickness and/or adhesion treatments. All these attributes reduce the signal integrity engineer's ability to predict and design for maximum performance. When tied to the range of electrical concerns such as resistance, dielectric loss, conductor loss, stray capacitance elements, signal skew and inductance which can lead to cross talk and potential reflections due to electronic stubs from circuit features such as vias, one quickly sees a compounding of the problem. It becomes evident that new approaches to solving these problems are required. While improvements in materials and manufacturing processes have yielded some improvements, signal integrity experts still warn of the future impact of the limiting elements of current approaches to printed circuit design and manufacture. Thus it becomes clear that a new and better way of addressing these problems is to simply avoid the traditional design approach path in favor of new design methods that break the manufacturing challenge into more manageable pieces.

This paper will examine and describe such methods incorporating fundamental approaches, which three-dimensionally partitions printed circuit design and in the process segregates high speed signals from lower speed signals and power and ground connections. Novel methods and structures that accomplish this objective illustrate how high speed signals are interconnected by means of controlled impedance links that are fabricated separately from the PCB and later interconnected directly between IC packages where required. Thus instead of trying to precisely control a complex printed circuit design into a monolithic interconnect the signals are instead segregated and critical signals are shepherded to a more easily controlled interconnection paths that lead directly from chip-to-chip or chip to other suitable electronic device.

Introduction
The design and manufacture of circuit assemblies have gone through several definable eras since the invention of the printed circuit board. Early PCBs were relatively simple affairs designed primarily to replace discrete wire interconnections between simple devices. However, with the introduction of the integrated circuit, there came increasing complexity and the single sided board evolved to use the second side for circuits and power and ground distribution and shortly thereafter, the plated through hole era began. Further advances in IC technology and the desire for increased functionality gave rise to the concept of the multilayer board wherein power and ground were distributed on internal layers and interconnected by plated through holes. Multilayer technology remained fundamentally unchanged for nearly 20 years but was punctuated with incremental but important innovative changes, such as the buried via, which helped to further increase board density and functionality and ease assembly. In the early to mid 1990s, HDI (high density interconnection) technology debuted as the successor to the much more expensive multichip module. The new technology was marked primarily by the presence of micro vias, produced either by photolithographic or laser technologies, which paved the way to much greater circuit density capability. Since the introduction of HDI, which has faithfully served and still serves well the needs of high pin count packages such as BGAs, there have been described a host of new board construction technologies that provide the increased interconnection density to solve the problems of routing. Other technologies being tapped to help include the embedment of passives and use of distributed capacitance layers in the board.[1]

A more recent design response has been to create what has been labeled a “system in a package” (SiP). This technology is a rebirth of the MCM as it shares many of the characteristics of the earlier but ill-fated solution. Once again the technology is fundamentally targeted to increasing density in an effort to yield greater functionality per unit space and greater localized performance. From a density perspective, solutions to date have been most impressive. For example, leading edge SiP devices include up to eight or more chips integrated in their construction. While most SiP solutions have, in general, been related to increasing functionality and reducing volume while lowering cost (such as what has been witnessed in cellular phones), higher performance remains a never ending priority in electronics.[2, 3] While these multichip package structures have admirably met the challenge of higher interconnection density, they have unfortunately not addressed as well, the challenge of meeting the signal integrity requirements for higher speed relative to their interconnection on the circuit boards to which they are joined. It is thus apparent that there is need for new approaches to designing and manufacturing interconnections to meet the current future needs of high performance electronic systems and desirably deliver those systems at lower costs. (See Figure 1.)

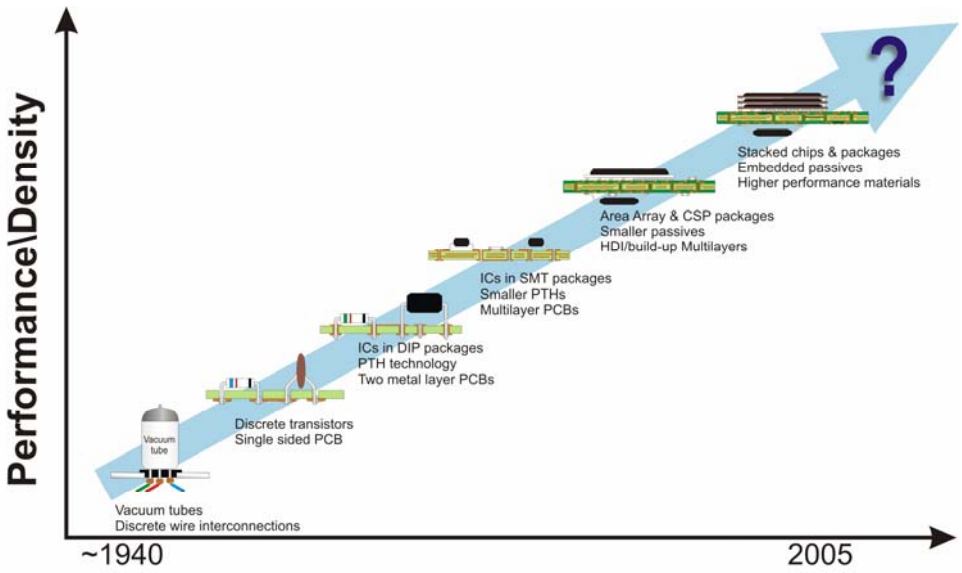

Figure 1 - The Evolution of the Printed Circuit has been Paced by the Demands of IC Technology

Complexity has increased significantly over the years but there are limits to what extrapolated technologies can offer in terms of cost and performance.

Rethinking Chip Package and PCB Design

Chip-to-chip interconnection is the fundamental objective of electronics system board level design. That basic task is made even more complicated in recent years as the need for higher switching speeds are now a matter of increasing importance. The present and future challenge in interconnection design is to get ever higher performance at ever lower cost. Compounding and expanding the scope of the problem is the fact that the power density from all of the various high speed signals is becoming significantly greater and thus thermal management is simultaneously moving to the top of the problem list. Much to their credit, system-in-package developers are developing some very clever solutions for getting the heat out of these densely packaged silicon structures. Even so, system in package devices carry with them appreciable risk.

The resulting and seemingly never ending tension between performance demand, product size and cost and ultimate system reliability makes for hard design choices. If the devices are relatively inexpensive and manufactured using mature and predictable semiconductor technologies, where one knows approximately what infant mortality is likely to be, SiP technology will likely appear very attractive. However, in cases where the IC die are cutting edge and expensive, the system designer will likely and correctly want to be a bit more circumspect and perhaps more hesitant before jumping directly into SiP solutions. Moreover, while hand-held electronics continue drive much of interconnection technology owing to the demand for ever greater functionality in a small space, the sort of applications where highest operating performance is sought are typically not so space constrained as hand held electronics. Such systems are thus open to other solutions that can provide the needed benefits in a cost effective manner.

The convergence of clashing objectives has created significant challenges but within those challenges lays the opportunity to rethink the long held approach to circuit assembly design and how and where chips are interconnected. It is a simple and easily asserted fact that the standard materials and design processes will no longer meet the performance needs for high speed interconnections. While silicon technology continued to double performance every 18-24 months in accordance with Gordon Moore's postulate from the 1970s, copper interconnection technology was largely unchallenged until the processor transitioned into the multi gigahertz range. Today's PCB bus speed is pegged at 800MHz using standard materials and design practices due to the many features of concern commonly found in the signal path (see Figure 2). Some relief can be found in exotic materials. However, they will offer only temporary relief and they increase cost. There is another path to relief by reconsidering the design, manufacture and assembly of PCBs. The solution is conceptually simple: route the highest speed signals between chips designed to communicate with one another using a more direct path preferably through a controlled impedance channel. The question is how can this best be done. The answer is quite simple: establish signal paths in all three dimensions of space.

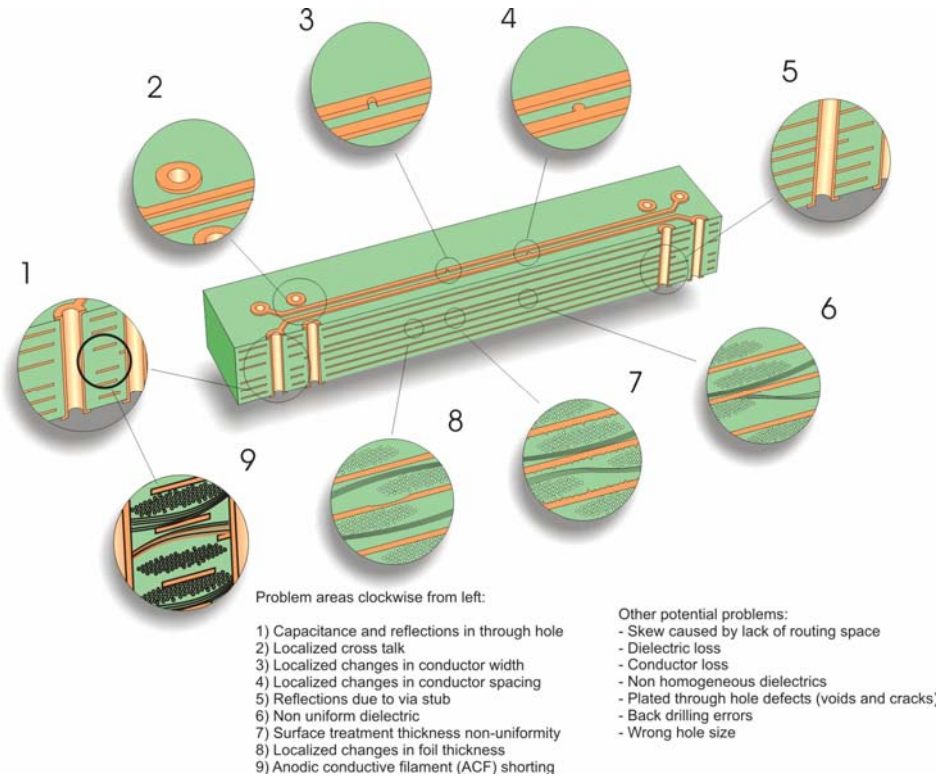

Figure 2 - Standard PCB Materials and Processing Methods have a Significant Number of Potential Impediments Relative to High Speed Signal Processing

Many of the items enumerated have little impact for lower speed signals, however at higher speeds, their impact can be major.

OTT Packaging Technology

While traditional PCB design has signals routed on, in and through the PCB, an improved approach to design has signals routed both through and above the substrate with critical routes transmitted directly from chip-to-chip by means of controlled impedance interconnects mounted to the upper surface of the packages. This “elevated highway bypass” concept avoids the traditional paths thought the PCB for high speed signals and thus all of the other circuit elements and features that are a part of the design which contribute signal degradation and poor high frequency performance. As mentioned earlier, there are a significant number of potential design feature and material and processing concerns in traditional board design and manufacture. The list includes: the metal conductor path including its height, width and length and their proximity to other circuit paths; the signal path’s own various interconnection vias encountered over the course of the circuit path. In addition, there are other interconnection elements such as connectors and solder joints, etc., all of which are capable of creating signal discontinuities and disturbances reducing performance capability. There is also the matter of signal skew which contributes significant routing challenges for designers trying to exactly match signal path lengths. Moreover, in high speed signal propagation, the signal rise time is degraded due to signal loss in the materials of construction, manifest in the form of dielectric loss. Finally, conductor loss must be factored in, in addition to the numerous design features that can create impedance discontinuities previously accounted for.

These parasitic inducing design artifacts have been of little consequence in lower speed circuit applications (typically below 100 MHz). They are critical as signal speeds for digital systems enter the multiple gigahertz range. And while improvements in materials and manufacturing processes have yielded some performance gains, it is clear that there has been need for improved methods to address the underlying high frequency impediments.

The OTT (“Off the Top”) packaging design approach partitions the high and low speed design elements and routes them on different planes, with low speed, power and ground signals routed down through the package and into the PCB substrate while the high speed signals are routed directly off the top of one package to the top or tops of one or more other packages. The result is a very high performance interconnection path that does not require pre or post emphasis of signals. This is possible because of the clarity offered by the improved signal channel. Figure 3 provides a cross sectional comparison of the old and new approaches and Figure 4 provides a comparison of the simulation based eye diagrams for the two different methods over a common distance of 3 inches at 25Gbps.

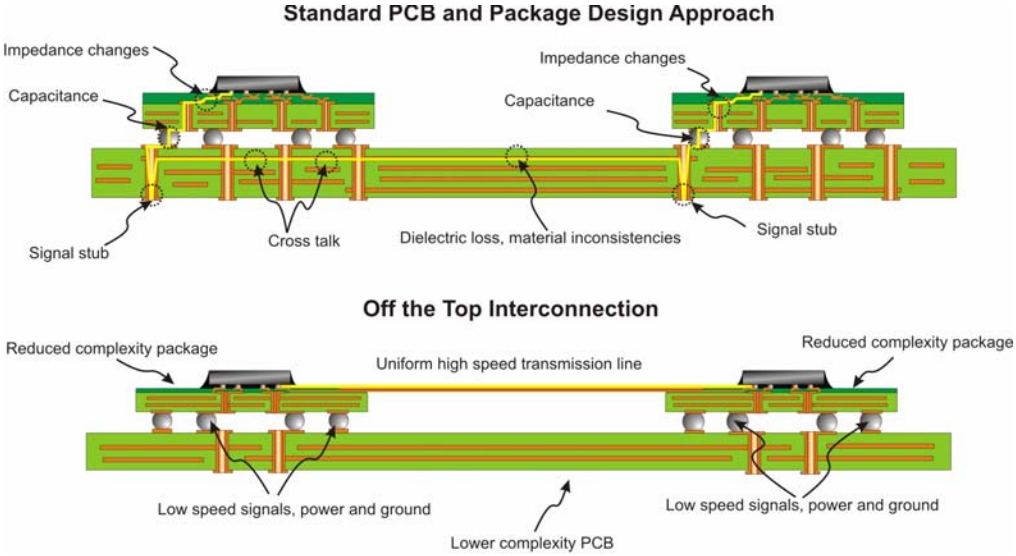

Figure 3 - The OTT Packaging Approach Significantly Improves Performance and Simplifies the Construction of Both Package and PCB, while Bypassing the Parasitic Effects Associated with Most Traditional Design Layouts

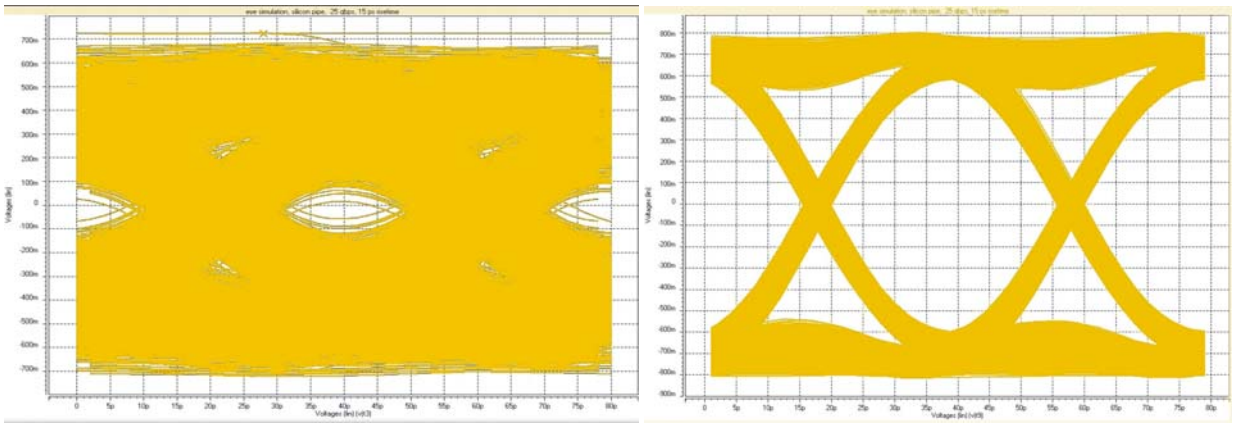

Figure 4 - The Eye Diagram Comparison Based on 3D Field Solver Simulation Data Show an Exceptional Improvement is Possible Using the OTT Technology (Right) Compared to the Standard Design Approach[8]

Because the upper surface of a typical chip pack is largely wasted space, except in case where devices are designed for stacking to improve density, there is an opportunity to use this space for selective interconnection between circuit devices which can benefit from high speed signals. By analogy, while old methods route signals on the equivalent of city streets and subways, (and high rise buildings in the case of stacked packages) the new proprietary approach[4] allows for signals to be routed on the equivalent of controlled impedance, high-speed elevated superhighways, thus eliminating the circuitous and undulating circuit routes necessitated by traditional approaches. Perhaps the most obvious electronic interconnection medium for creating such a structure is a controlled impedance flexible circuit but it is not so limited as there are many other interconnection structure embodiments which can serve. (See Figure 5.)

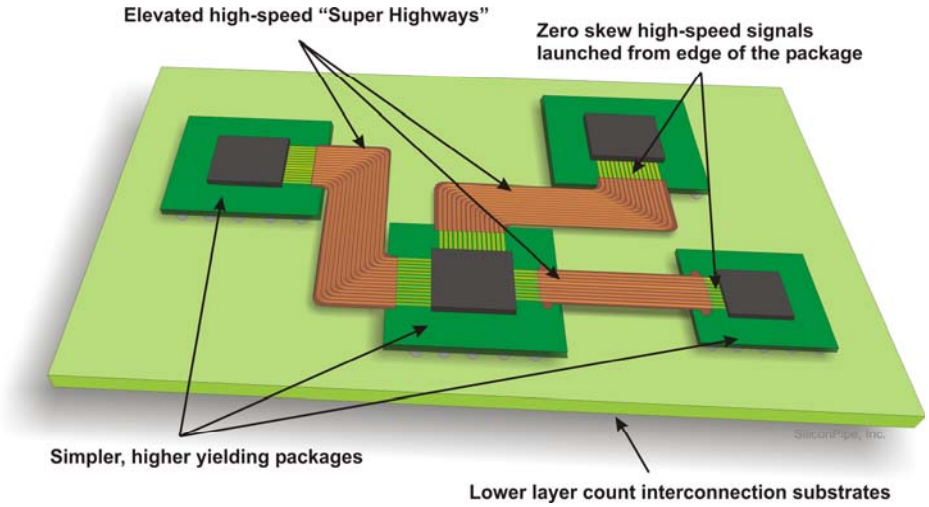

Figure 5 - The Use of OTT Packaging Concepts Provides Significant Reductions in Signal Skew and Assuages Many of the Other Challenges of High Speed Circuit Design by Segregating High and Low Speed Signals thereby Interconnecting Simpler, More Manufacturable IC Packages and Substrates

Despite its compelling advantages, OTT will likely take some time to become mainstream. There are, as of now, no conventions or standards for such packages even though IC packaging foundries generally see no significant challenge to the manufacture of such devices. That said, there is opportunity to employ the technology today, for those who wish to gain the benefits more quickly and have two or more IC chips to communicate at native silicon speed. The patent pending solution is relatively simple and is illustrated in the Figure 6. As is shown, an existing package can be easily adapted to the high speed task by simply attaching a rigid or flexible over lay extension to the surface of the existing package and ignoring the old signal paths and instead making direct connection from the chip to the high speed bypass. This technique also allows for the addition of separate driver chips to boost performance for longer distance transmission. Such devices could take the form of pre-tested IC packages joined and interconnected within another package.[5]

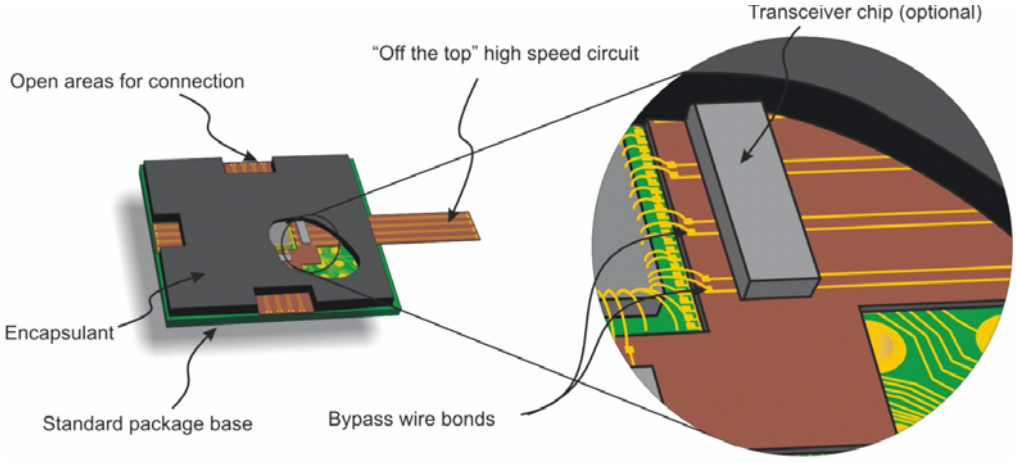

Figure 6 - The OTT Packaging Benefits Are Realized Using Existing Packages and Mounting and Interconnecting a Controlled Impedance Circuit to the Top of a Standard IC Package

High speed signals are bypassed on the existing package interconnections in favor of better controlled circuits on the cable. In cases where higher performance or longer distance is required, separate driver chip can be interposed.

Applications for OTT Packaging Technology

The concepts associated with off the top interconnection give rise to a range of other areas of potential application. A brief presentation of some of those applications, illustrated in Figure 7, assists in understanding the potential of the technique and is likely to spark other ideas. One of those areas found in the direct interconnection multiple chips such as FPGAs in a structure fashion.[6] Such solutions allow a product designer to create an unlimited "sea of gates" with little loss of time and without the need for expensive mask sets. Another area of application is in memory. The clean channel offered by the technology allows for a wide range of improved memory architecture design options (Figure 8). One proposed approach

allows standard DDR-II memory to be operated at a rate equivalent to 12.8 Gbps, with silicon design modifications the rate could be 2 to 4 times faster, [7] yet another area of potential application is in chip to connector constructions, which is an area of current development activity.

Direct interconnection between chip and connector provides a short path and relatively inexpensive solution to a range of current challenges from electrical test to telecommunications. The latter is the area of current development and demonstration. Construction of a chip-to-connector solution increases the overall performance of current generation switches, routers and memory storage farms by as much as 20% without the need for a "forklift upgrade" to a new system. Relatively simple design modification of daughter cards to allow direct interconnection between the controller chip and the connector obviates the need for more exotic and more expensive substrates while reducing system power needs.

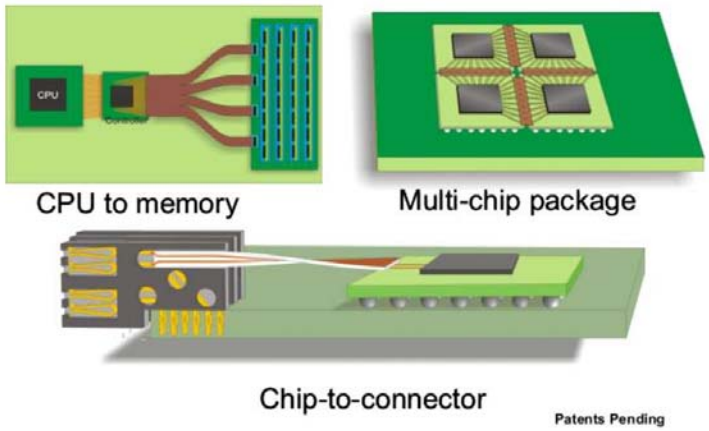

Figure 7 - OTT Packaging Technology Opens the Door to a Range of New Interconnection Opportunities Including New Memory Architectures, Ganging of FPGAs to Create an Unlimited "Sea of Gates" and Higher Performance Chip-to-Connector Solutions for Line Card Applications

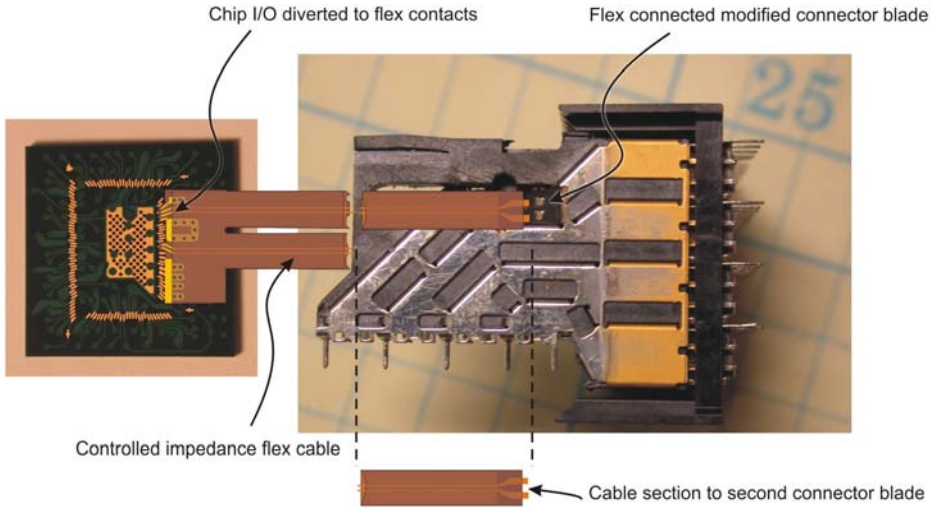

Figure 8 - Provides a Close-Up View of the Elements of the Test Vehicle Construction

Simple modifications to existing interconnection elements provide a cost effective path to creating high performance interconnections. (Note: The controlled impedance flex cable was being fabricated at the time of writing)

Discussion

While the concepts presented are presumably attractive for a range of applications, there are still a number of puzzle pieces, which must be put in place before broad scale adoption is achieved. With respect to IC packaging design, there is a need to establish appropriate methodologies and protocols in different areas. For example with respect to I/O planning and sequencing, there are no tools which address the matter of considering the creation of high speed interconnections between two distinct packages separately from those connections which are to be made through the PCB. Put into other words, with the OTT approach, all of the I/O are not considered for interconnection at the same time and this will require a new

methodology. Coordination of what is effectively two different designs, must accommodate high speed fixed interconnections so that they can be considered once the packages are mounted on the PCB.

The PCB design and manufacture may well be less complex, due to the fact that those steps have been relieved of the challenge of making and maintaining the critical circuit paths. However, in PCB assembly there will be some areas of new challenge. For example, depending on the approach chosen, IC package alignment may need to be tightened so that the flex circuit or other interconnection schemes can connect reliably to one or more other packages once they are mounted on the PCB. There will also be a need to represent the top surface interconnections in three dimensional space and presently PCB tools are two dimensional. Still in the realm of IC packaging some of these 3D issues are being addressed in stacked wire bonded structures.

Another area not yet discussed is that of electrical testing of IC packages and assembled systems. Testing procedures can be simplified by OTT packaging. Having unfettered access to high speed signals makes full characterization of IC packages much less of a challenge and is an attractive alternative for future high performance package validation.

Summary and Conclusions

In summary, the roadblocks to high speed signal transmission from chip-to-chip can be addressed by a new approach to interconnection that takes advantage of the normally unused space that exists on IC packages. This method facilitates the creation of shorter, cleaner signal paths offering higher performance at lower power, fewer layer count packages and substrates, and ultimately lower cost systems. These alternative approaches to design significantly improve the performance of electronic products with minimal disruption to the manufacturing infrastructure. The move to high speed interconnections requires rethinking the electronic industry's standard approach to overall architecture. The partitioning of PCB circuit layout, segregating high speed circuits from low speed and power and ground circuits is an approach that will likely be seeing more use in the years ahead.

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