What to Consider when Designing a Universal Test Strategy Tool

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Abstract
Selecting an optimal test strategy is a complex task today. There are many test inspection and test methods available. The most common choices to find manufacturing defects on printed circuit boards are manual visual inspection (MVI), solder paste inspection (SPI), automatic optical inspection (AOI), automatic x-ray inspection (AXI), in-circuit test (ICT), and functional test (FT). This paper presents the key attributes to consider when designing a test strategy selection tool and how such a tool should work. Among the key attributes when selecting an optimal test strategy are: defect spectrum and defect levels, where in the manufacturing process defects are introduced, different test and inspection systems' test effectiveness, cost of test and inspection systems including programming and fixturing, cost of finding defects at different stages in the manufacturing process or in the field, and of course the complexity of the printed circuit board. Outputs from the tool should include yield calculations, DPMO (Defects Per Million Opportunities) at different stages of the manufacturing process, cost impacts, and defects captured and defects escaping. These predictions should be made for the different test strategies selected for analysis. The paper will describe how such a Test Strategy Tool can be design and also results in using a tool described in the paper.

Observations that impacted design of the tool
Over the years we have done a lot of research on the Printed Circuit Board Assembly (PCBA) manufacturing process. Results from this research [1, 2, 3, 4, 5, 6] and observations made are the key background on what was needed for a test strategy tool. These key factors will be explored first.

Defect levels
There are often claims made in the industry that companies have defects at the rate of only 50 – 100 Defects Per Million Opportunities (DPMO). Our studies suggest that these defect levels are probably obtained only on the board types with the lowest defect levels and probably only when everything is working to the advantage of that company. The average actual defect levels are typically significantly higher. A very comprehensive study [1], with production data from about six months of production at fifteen different companies and over one billion solder joints in the study, indicated an average defect level of between 650 to 1,100 DPMO. These numbers are probably closer to the real defect numbers in the industry, especially on medium and high complexity boards that are manufactured in smaller batches. The European SMART PPM Monitoring Project also reports these higher defect levels. Average DPMO levels for the whole project can be seen in Figure 1 [7].

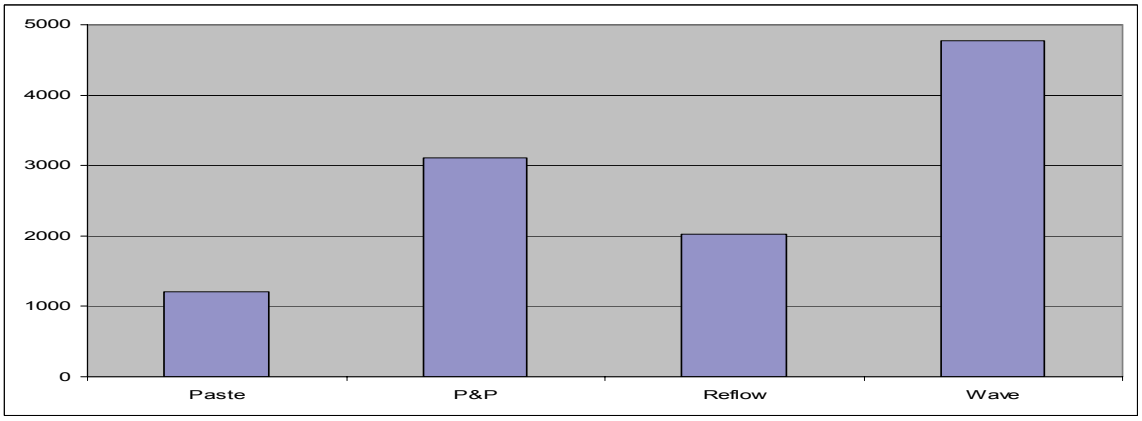

Figure 1 - Average PPM values from the SMART group study May 2002 to December 2003.

Board types manufactured in higher volumes on the same SMT line for several days typically have lower defect levels, between 200 DPMO to 600 DPMO, because process adjustments can be made to achieve lower defect levels.

A key point is that optimal test strategy is very different if the general defect levels are around 50 DPMO versus 500 DPMO. Therefore accurate DPMO data should be gathered; it should be the real values, not the marketing numbers used.

Test Effectiveness studies
A test or inspection system's capability to find defects is measured in a test effectiveness study. The Test Effectiveness study is done on a smaller sample of boards, typically between 20 to 100 boards. The lower number is used if the study is done on a very complex board with many defect opportunities. The higher number of boards is used for medium complexity boards with fewer defect opportunities. For optimum results a total of 100 to 200 defects should be found. The same set of boards is tested / inspected by different methods, such as AOI and / or AXI, ICT, and sometimes Functional Test.

For example, if we are doing a Test Effectiveness study of AOI, AXI, and ICT, the boards are first inspected by the AOI system. All calls that the AOI system makes are classified as either true defects or false calls. A log is kept of all defects classified as true defects, but they are not repaired at this time. In the test effectiveness studies, typically only one defect per component is counted, even if, for example, one QFP component has three open pins. After AOI the boards go to the AXI system and we repeat the process. All AXI calls, classified as true defects, are noted in the log. Again no repairs are done at this time.

After AXI the boards go to the ICT system and are tested again. At ICT we are still trying to isolate the true defects from false calls. Since ICT is the last step in our example study, we can now start to do repairs. In a Test Effectiveness study we are only keeping track of defects. It is also important to note that it is not the engineers from the automated test equipment (ATE) vendor who make the judgment on what is a defect and what is not. This is done by the EMS's and / or OEM's engineers.

Let's assume that after this process we have found a total of 100 defects. Let's also assume the AOI system found 59 of those defects, the AXI system found 91 of the defects, and the ICT system 52. Then the AOI system's Test Effectiveness is 59% (59 out of a total of 100 known defects), the AXI Test Effectiveness is 91%, and the ICT 52%.

From the result of the study good estimations of each systems capability to detect different type of defects such as missing components, solder bridges, opens, insufficient solder, etc. can be done. Results from test effectiveness studies have been presented in other papers [2, 3].

Where in the manufacturing process are defects introduced?
In our studies we have seen that the reflow oven can change many defects; we often call it the defect transformation box. Many defects go into the reflow oven and many defects come out of the reflow oven, but they may not always be the same ones. Examples of defects that change are: misaligned parts that self-align, insufficient solder that can make acceptable joints, parts that fall off, apparently good parts that do not solder, solder bridges that open up, and open areas that get bridged. At the same time some defects are the same both before and after the reflow oven. Examples are: missing parts that are still missing, parts with no solder paste that will not solder and will be open, gross misalignments that will still be misaligned, reversed parts that will still be backwards, and some misaligned that are still misaligned. This information is important to include in the test strategy selection.

We also observed in many studies that a wave or selective wave process contributes around 50% of all defects, information that should be considered.

Field failures and warranty costs
It is obvious that the selected test / inspection strategy will have an impact on the number of defects found by the end customer and also on warranty costs. An analysis of different test strategies impact on warranty defects for real production has been presented in other papers [4]. In short, the test strategy tool should be able to incorporate this into the analysis.

Complexity of the PCBA
The last major influence of the test strategy that we have observed is the board complexity. The more components and joints that need to be defect-free, the more difficult it will be to manufacture. Also a double sided board is more difficult to manufacture because there are more process steps required. Also some test methods like AOI only inspect one side at the time, so we need to keep track of defect opportunities on each side of the board, and if inspection is implemented whether it is applied to only one side of the board or to both sides.

How many defects and where
The first thing the tool needs is DPMO information so it can calculate how many and where defects can be detected. DPMO values for each defect, where they can be detected, and number of defect opportunities are needed. To describe how this can be done, a simple example will be used. Let's assume we have a simple PCBA with components on only one side. To make the calculations easy to follow, let's assume that the board has 100 SMT (Surface Mount Technology) components and 1,000 SMT solder joints. There are no through-hole components or press-fit components on this board. Also to calculate the total

number of defects, we will assume that the total board volume for this example board is 2,000. The manufacturing process can be in seen in Figure 2. Since it is a single sided board without any through-hole or press-fit components the only PCBA manufacturing steps are paste application, component placements, and the reflow process. Test and inspection steps (see Figure 2) are AOI pre-reflow, ICT, Functional test, and the end customer. It is important to view the end customer as a tester, because it is here that field failures will be detected which will impact warranty costs and overall customer satisfaction.

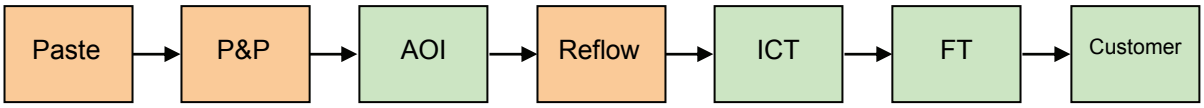

Figure 2 - Manufacturing, test and inspection steps for the example.

Different defects are introduced at different places in the manufacturing process and also different test / inspection systems have different capability to detect different type of defects. Therefore the tool should be able to differentiate between different defect types. In our simple example we only include four defect types: solder bridges, opens, insufficient solder, and missing components. Let's assume that the defect levels for bridges are 100 DPMO, for opens 200 DPMO, for insufficient solder 200 DPMO, and for missing components 500 DPMO. In Table 1 you can also see where defects are introduced and can be detected. For bridges 20% can be detected after the paste application process, another 10% can be detected after the component placement process, and the remaining 70% can be detected after the reflow process.

Table 1 - Defects, defect levels, and where introduced and detectable.

			Introduced AND can be detected		
Defects	**Defect type**	**DPMO**	**Paste**	**P&P**	**Reflow**
Bridges	Joint	100	20%	10%	70%
Opens	Joint	200	10%	30%	60%
Insufficient solder	Joint	200	30%	10%	60%
Missing component	Component	500	0%	90%	10%

Note that bridges, opens, and insufficient solder are joint type defects, and missing components are a component type defect. From the above information we can calculate the number of defects of each defect type we will have for this batch of boards. For solder bridges we will have 100 (DPMO / 1,000,000) * 1,000 (solder joints per board) * 2,000 (board volume) = 200 bridges. In similar fashion we can calculate that there will be 400 opens and 400 insufficient solder defects. Since missing component is a component type defect there are only 100 defect opportunities per board and the total number of missing components are 500 (DPMO / 1,000,000) * 100 (components per board) * 2,000 (board volume) = 100. We can use the information in Table 1 to also calculate where defects first can be detected. For bridges 20% can be detected after the paste application process so the total number of bridging defects at this step is 200 bridges * 20% = 40. After the placement operation an additional 10% can be detected or 10% * 200 = 20 and finally after reflow the remaining 140 bridges (70% * 200) is now detectable. So for this example we now know how many defects we have and where they first can be detected. See Table 2 for complete information.

Table 2 - Number of defects and where they are introduced and can be detected.

		Introduced AND can be detected		
	Defects	**Paste**	**P&P**	**Reflow**
Bridges	200	40	20	140
Opens	400	40	120	240
Insufficient solder	400	120	40	240
Missing component	100	0	90	10

Test effectiveness for different defects

The next piece of information needed by the test strategy tool is the effectiveness of different test and inspection systems at finding different defects. See Table 3 for values used in this example. AOI is typically very good at finding component placement type defects; therefore we have used 99% effectiveness in this example. For ICT we have assumed that 100% electrical access is available (the tool needs to have a way to describe if that is not the case). Also note that electrical test has a low effectiveness on solder quality defects. Electrical test will only detect these if they become a fault. The effectiveness for Functional test is higher than what we have typically seen in our test effectiveness studies [2,3] but keep in mind that this is only an example. The last "tester", the customer, is very often overlooked in test strategy selections and economic models; however it can be argued that it is the most important "tester". If the end customer experiences a defect, that will increase warranty cost and/or will impact customer satisfaction. If the "End customer" is included in the analysis, then warranty cost

and customer satisfaction issues will at least be exposed. Typically it is very difficult to get accurate test effectiveness numbers for this "tester", but try to get data from warranty data and/or use engineering judgment.

Table 3 - Test and Inspection System Test Effectiveness for the Different Defect Types.

	AOI	ICT	FT	Customer
Bridges	70%	90%	60%	40%
Opens	60%	60%	40%	30%
Insufficient solder	30%	0%	10%	10%
Missing components	99%	50%	40%	30%

How test strategy tool should work to estimate defect capturing and escapes

With the data above, which all should be input values to the tool, the overall test effectiveness for the selected test strategy can be calculated. In Figure 3 we can see the manufacturing steps and the selected test and inspection options selected. The first inspection step is AOI placed pre-reflow. First we need to estimate how many defects are available for detection at this stage. In Table 2 we can see each defect type and where defects can be detected. For AOI we need to add defects detectable after the paste and the placement operation (P&P). In this example we have 60 bridges (40 + 20), 160 opens (40 + 120), 160 insufficient solder (120 + 40), and 90 missing components (0 + 90). To find out how many defects AOI will detect we need to multiply the number of defects available with AOI's test effectiveness for each defect type. For bridges we have a test effectiveness of 70% that means that 70% of the 60 defects will be detected by AOI and that is 42 defects. This also means that 18 bridges will escape this test step. For number of other defects detected by AOI in this example see Figure 3, in the box under AOI.

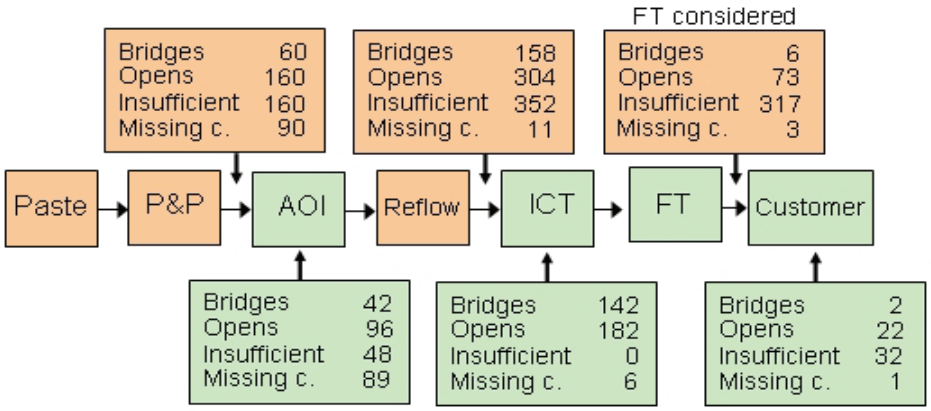

Figure 3 - Simple Example with Defects Introduced and Detected at Different Test Stations.

After AOI, the boards go to reflow where new defects will be introduced. Also, some defects whose root cause actually occurred earlier will now be detectable. For solder bridges we have an additional 140 defects "introduced" at this manufacturing step. In addition to the 140 bridges we also have 18 bridges that escape the AOI; therefore we have a total of 158 bridges at the beginning of the next test step, which in this case is ICT. In Figure 3 you can see all defects available to ICT in the box in front of and above the ICT box.

Now ICT will have a chance to detect these defects, so we have to apply ICT test effectiveness numbers on all defects available to it. For the bridges it has 90% effectiveness, so 142 bridges out of 158 will be detected here (90% * 158). How many opens, insufficient solder, and missing components will be detected can be seen in Figure 3 in the box below the ICT box.

For functional test the same calculation is done. First we need to calculate how many defects are available to functional test. There may be no box in Figure 3, but consider the escapes from the ICT process since no manufacturing steps are between ICT and functional test. In Figure 3 the number of defects that still remain after functional test can be seen in the box above the FT box. These are the defects that escape the whole test process and are "shipped" to the end customer. Note that not all of these defects will be detected by the customer, because not all will become faults. To estimate how many defects will be detected, the customer effectiveness numbers need to be multiplied by defects available. This is done in the same way we have done for AOI, ICT, and functional test in this example. The number of defects detected by the end customer can be seen in Figure 3 in the box under the "Customer" box. These numbers may be acceptable or they may not be acceptable. If they are not acceptable we need to improve the test strategy. In this example we see that many insufficient solder and opens defects are escaping and are likely to be detected by the end customer. We know that Automatic X-ray Inspection (AXI)

typically has very good effectiveness for these types of defects, so we would run the tool adding AXI to the test strategy and see the result.

In the example above we have shown how many defects are detected and how many may escape a certain test strategy. That is very important information, however it is not enough. We also know that adding more test / inspection steps increase the test effectiveness, but it also adds test costs, so we need to include economics into the test strategy selection tool.

Test economics

From an economic point of view, the most significant impacts on overall cost are cost of finding and repairing defects at different stages of the manufacturing process, capital cost and programming of test / inspection systems, cost of running tests including false calls, and last but not least warranty cost and field failures.

Let's consider the cost to find and repair defects at different steps in the process. We know that inspection systems have the best diagnostic resolution so their cost is mainly to decide if it is a true call or false call and do the repairs if necessary. ICT has good diagnostic resolution but not as good as inspection systems, for example a short reported by the in-circuit system may take some time to locate so the cost of finding and repairing is higher than for the same defect detected by an inspection system. As we move down the manufacturing line the cost typically increases mainly because the test systems used have less diagnostic resolution. For field failures and warranty cost we also have to add shipping costs or traveling costs for a service engineer. In this type of analysis, costs for false calls should also be considered. This should be estimated and average cost per defect at each test step should be available for the test strategy tool. Depending on which test strategy is selected, different numbers of defects will be detected at different test / inspection steps. With this information available, and the number of defects and escapes calculated as explained above, a cost estimate can be done.

Programming and fixture cost are typically easier to estimate from board types of similar complexity. Also estimated run times and re-test rates should be considered, because this will impact capital cost and costs from operators if needed. This data should be entered into the test strategy tool. If a test step is included in the test strategy, then these costs should be included. If the test step is not included, then the cost should not be included.

The tool described in this paper has been used over several years and what we have seen is that warranty costs have the biggest impact on identifying the most economically favorable test strategy.

Outputs from the tool

So far we have described all the inputs needed to do a test strategy selection, including how many defects will be captured and will escape different steps. DPMO levels, test effectiveness data, and cost of finding defects and false calls do not need to be updated for each board type. With all the information available, a lot of interesting calculations can be made. Typically when an analysis is performed, three to four different test strategy options are selected. For those test strategies, the total cost for a specific board should be calculated for each scenario. Number of defects and escapes and also true DPMO and measured DPMO values should be calculated at each test / inspection stage for each test strategy selection. The true DPMO value is how many defects are available at a certain stage. The measured DPMO is what a test or inspection system is detecting. Since no test or inspection system has 100% effectiveness, the measured DPMO value will always be lower than the real DPMO value. Yields for the different scenarios should also be calculated. Calculating yield correctly is difficult[8]. Most formulas assume that defects are randomly distributed which typically is a reasonable assumption when defects levels are very low. However for medium to high defect levels we know that defects tend to cluster to some boards, making the true yield higher, than which is calculated using normal distribution assumptions. Both non-clustered and clustered yield models should be available in the tool [8].

The objective with this tool is to use it very early in a project. It can be used before a detailed bill of material (BOM) is available. As with all predictions tools, the more accurate the available input data, the more accurate the results will be. The tool is available with default values from all the research mentioned in the paper and will give reasonable results given those default values. All input data to the tool can be changed. Again the objective is to give the big picture of different test strategy options very early in the process. Later in the project when a BOM is available and test programs are available, an analysis of program coverage is in place. A tool to do that type of analysis was described in another paper[9].

Summary

The test strategy tool described in this paper is based on research and studies done on defect levels, test effectiveness, and test strategies. Given reasonably accurate input data, the tool is the most effective way to analyze different test strategy scenarios and their economic impacts. The tool has shown that it is also a very valuable learning tool, to gain insight into what really happens: when defect levels changes, when defect coverage changes, for different test strategies, and for defects introduced at

different stages in the manufacturing process. The tool has been used in many test strategy decisions and as a very objective input to test strategy discussions between EMS and OEM companies.

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