Fluxless Sn-Ag Solder Joints between Silicon and Ag-Cladded Copper with Reliability Evaluations--MEJ

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Abstract
A fluxless bonding process between silicon and copper using Sn-rich Ag-Sn-Au multilayer composite has been developed. The copper substrate is plated with a silver layer as stress buffer. We bond 5mm x 5mm silicon chips onto Ag/copper substrates using electroplated lead-free Ag-Sn-Au solder. Electroplating method becomes an attractive deposition technique in that thicker films can be fabricated. It also has an economical advantage over vacuum deposition technique. To achieve high quality joint with few voids, a fluxless bonding process is developed in vacuum environment (50 militorrs) to suppress tin oxidation. Comparing to bonding in air, the oxygen content is reduced by a factor of 15,200. Nearly void-free solder joints are made. Initial joints comprising of three distinct layers of Sn-rich layer, Ag_3Sn intermetallic compound, and Ag layer have been achieved. Microstructure and composition of the joint are studied using optical microscope and Scanning Electron Microscope (SEM) with energy dispersive X-ray spectroscopy (EDX). This technique becomes an innovative success for overcoming the very large mismatch in thermal expansion between silicon of $3x10^{-6}$ppm/°C and copper of $17x10^{-6}$ppm/°C. To evaluate the reliability of the solder joint and the bonded structure, samples will go through thermal cycling test and failure modes will be evaluated in the future. Microstructural changes of the solder joints during thermal cycling test will be investigated and assessed. Based on the results obtained, design recommendation can be made for producing joints with high re-melting temperature.

Introduction
For high power electronics, it is highly desirable to attach semiconductor device chips on highly thermal conductive substrates. Due to its high electrical and thermal conductivities, copper has been widely used as substrates to mount device chips [1-2]. It thus has been a long term pursue for industries to develop processes to bond silicon to copper using metallic joints that have high thermal conductivity and possibly high melting temperature. The great challenge in Si-Cu structure is to deal with and manage the very large mismatch in thermal expansion between silicon of $3x10^{-6}$ppm/°C and copper of $17x10^{-6}$ppm/°C [3]. So far, we still have not seen such a bonding process reported in the publications.

In this paper, we report our initial technology success in bonding large silicon chips (5mm x 5mm) on copper using Sn-rich Ag-Sn-Au alloy. The copper substrate is plated with a thick silver layer as stress buffer. The yield strength of silver is close to that of Sn-Ag eutectic alloy and is one-tenth of that copper. We thus expect the silver layer to absorb the high stresses developed in the bonded structure. Fig. 1 displays the Ag-Sn phase diagram [4].The γ phase is the well known Ag_3Sn compound. The Ag-rich ξ phase and (Ag) phase both have high melting temperature. After the initial bonding, if the joint can be converted to (Ag) phase by an annealing step to cause sufficient solid-state inter-diffusion between the Sn-rich Sn-Ag joint and the Ag layer on the copper substrate, the melting temperature of the joint can be increased to 720°C. The thin upper Au layer plated over tin is used for preventing the oxidation of inner Sn layer. This is very important for achieving fluxless feature. Nucleation mechanism of thin Au plating over Sn layer has been studied previously in our group [5].

Regardless of what solders are used, flux is almost always necessarily used in the soldering processes in electronic industries to remove oxides on the molten solder and on the base metal, and to shield the contact solder surface from further oxidation. In most applications, the flux residues have to be removed afterwards by employing solvents that are environmentally unfriendly. In small scale applications, flux residues are embedded or trapped in the material system. In this connection, we envision the need of fluxless soldering processes in the packaging applications. Especially for the devices where the gap between the chip and the substrate becomes very small, it might be very difficult to completely remove flux residues that result from the use of fluxes. The flux residues trapped in the gap can degrade the performance of the device and may also cause long-term reliability problems [6]. We thus expect the increasing need of fluxless processes and set out to develop these fluxless processes. The applications requiring fluxless processes seem to have been expanding recently. Our research group has been pioneering on fluxless bonding process that was performed using various binary and ternary multilayer composite structures deposited in high vacuum such as gold-tin, gold-indium, silver-tin, and tin-bismuth-gold [2, 7-10]. There also have been several successes in fluxless bonding to fabricate the multilayer structure for high re-melting temperature application produced at low process temperature using vacuum deposition method [11-13]. For all of these processes, the multilayer solder materials are deposited on the wafers or substrates in high vacuum chamber ($2x10^{-6}$ torr) to prevent oxidation. While these processes work well for achieving uniform and clean film, the vacuum deposition process is costly to maintain and hard to deposit solder layers thicker than 10μm due to film stresses and long evaporation time. To provide an alternative solder

manufacturing process, we turn to electroplating technique mainly due to its low cost and ability to produce thicker layer. In this connection, instead of using vacuum deposition to fabricate the multilayer structure for bonding application, we turned to electroplating processes to build the bond structure in order to reduce cost and to obtain thick layers.

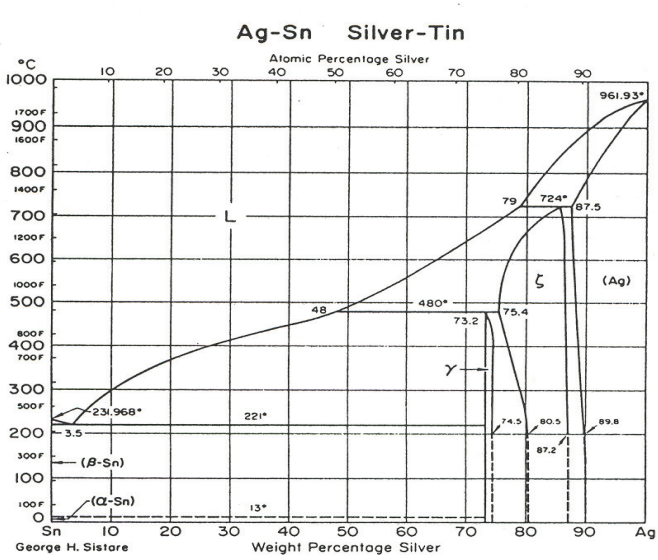


Figure 1 – Equilibrium Phase Diagram of Tin-Silver System [4]

In our initial design, 60μm Ag is electroplated over Cu substrates followed by 10μm Sn, and 0.1μm capping layer of Au. The purpose of thin Au capping layer is to prevent oxidation of inner Sn so that fluxless feature can be accomplished. It is known that electroplated Au readily react with Sn to form $AuSn_4$ intermetallic compound as soon as it is plated [5]. 5mm x 5mm silicon chips are bonded to 6mm x 6mm copper substrate. The joint cross-sections are studied using SEM and EDX to find the microstructure and composition. The joints will also be examined using SAM to confirm the bonding quality to see internal microvoids. After achieving high quality joint, thermal cycling test will be performed to evaluate the reliability of the joints and the bonded samples.

In this specific study, we first focused on achieving high quality joints using Sn-rich Ag-Sn solder layer. After achieving high quality joint, we will move onto the next project of achieve high temperature joints by proper annealing steps. High temperature joints made without flux at low temperature have critically important applications for emerging packaging semiconductor devices such as AlGaN/GaN-based field-effect transistors and heterojunction bipolar transistors [14, 15] that can operate at high temperature. There is no good technique to attach these high temperature chips onto substrates or packages that would sustain continuous high temperature operation such as 300°C. Thus, these high performing chips cannot be put into real use without solving the chip bonding difficulty.

In what follows, we first present the experiment design and procedures. Experimental results are reported and discussed. A short summary with future plan is then given.

Experiment Design and Procedures

In our design, we start plating thick Ag on 10mm x 12mm Cu substrates to build electroplated multi-layer solder structures for bonding. The purpose of Ag layer is to absorb high stresses in the bonded structure caused by large thermal expansion mismatch between Si and copper. Another purpose is to provide enough Ag to form Ag-rich joints in a follow-up annealing step. The Cu substrates are made of alloy 110 with 99.9% pure Cu, and one-side was mirror-finished. The Ag plating bath is a cyanide-free, mildly alkaline plating solution at pH 10.5 and performed with mild stirring. A plating area of 10mm x 12mm is defined by stop-off lacquer to prevent deposition on the backside, which is removed after plating. The current density and process temperature were 4mA and room temperature respectively. 60μm of Ag layer is electroplated on Cu substrate in 165 minutes. It is followed by 10μm of Sn plating in a stannous Sn based bath at 21.5mA/cm^2 at 46^{o}C. In the final step of the plating, thin layer of Au (0.1μm) is electroplated on Cu/Ag/Sn substrate as a barrier for preventing inner Sn layer from being exposed to air to be oxidized. Prior to the Au plating process, the sample is chemically treated to reduce the possibility of an oxide layer over the Sn. This Cu substrate (10mm x 12mm) is cut into half later for bonding sample. To perform the bonding, a Si wafer is deposited with 0.03μm Cr, followed by 0.1μm Au by E-beam evaporation in one vacuum cycle, and diced into 5mm x 5mm chips. Cr layer is for better adhesion between silicon and gold. Gold layer is for preventing Cr oxidation. The Si chip and Cu substrate are held together with a static pressure of 50 psi in a graphite fixture to ensure intimate contact.

Fluxless bonding is carried out in 50 mtorr vacuum inside a vacuum bonding chamber built in house to greatly reduce oxidation. Comparing to bonding in air, the amount of oxygen available to oxidize the molten solder is reduced by a factor of 15,200. Two different bonding conditions are used. First fluxless bonding is conducted for short reflow time with relatively low peak temperature. The bonding platform is heated to 235°C and the reflow time is less than 2 minutes. Secondly, longer reflow time with higher peak bonding temperature is used. i.e. 15 minutes reflow time and 250°C peak temperature. The temperature of the fixture is monitored with a thermocouple attached to it. After reaching peak temperature, the furnace is turned off and the assembly is allowed to cool naturally to room temperature while still in the vacuum chamber.

To evaluate the quality of the joints, SEM and EDX are employed to characterize the composition and microstructures of cross-sectional solder joints. Bonded samples under two different conditions are compared and discussed. Based on the results that we get, reliability evaluations such as annealing and thermal cycling tests are being performed.

Experimental Results and Discussions

Bonding Mechanism and Solder Joint Formation - Condition I (Shorter reflow time)

Figure 2 depicts the schematics of the bonding principle. As was mentioned earlier, the electroplated Cu substrate (with Ag/Sn/Au) and vacuum deposited Si chip (with Cr/Au) are placed together in the vacuum furnace to form a joint. Chamber is pumped down to and kept at 50mTorr vacuum to reduce oxidation. In the electroplated solder structure on the Cu substrate, Au capping layer reacts with Sn to form $AuSn_4$ compound layer that acts as a barrier for preventing inner Sn layer from oxidation. Our bonding peak temperature is about 235°C, which is just above the melting temperature of pure Sn. Reflow time is just about one and half minute, and this is for preventing all the Sn layer to be consumed by thick Ag layer underneath it. As temperature increases towards the bonding temperature of 235°C, the Sn layer melts first at around 230°C and this molten Sn dissolves the upper $AuSn_4$ layer, as shown in Figure 2(b). Simultaneously, the Sn layer would react with thick Ag layer underneath to form Ag_3Sn intermetallic compound layer. With relatively short reflow time, there is still Sn rich layer remained between Si/Cr and Ag_3Sn intermetallic layer. While this happens, final joint would be comprised of Sn-rich layer, Ag_3Sn layer and Ag layer as displayed in Figure 2(d).

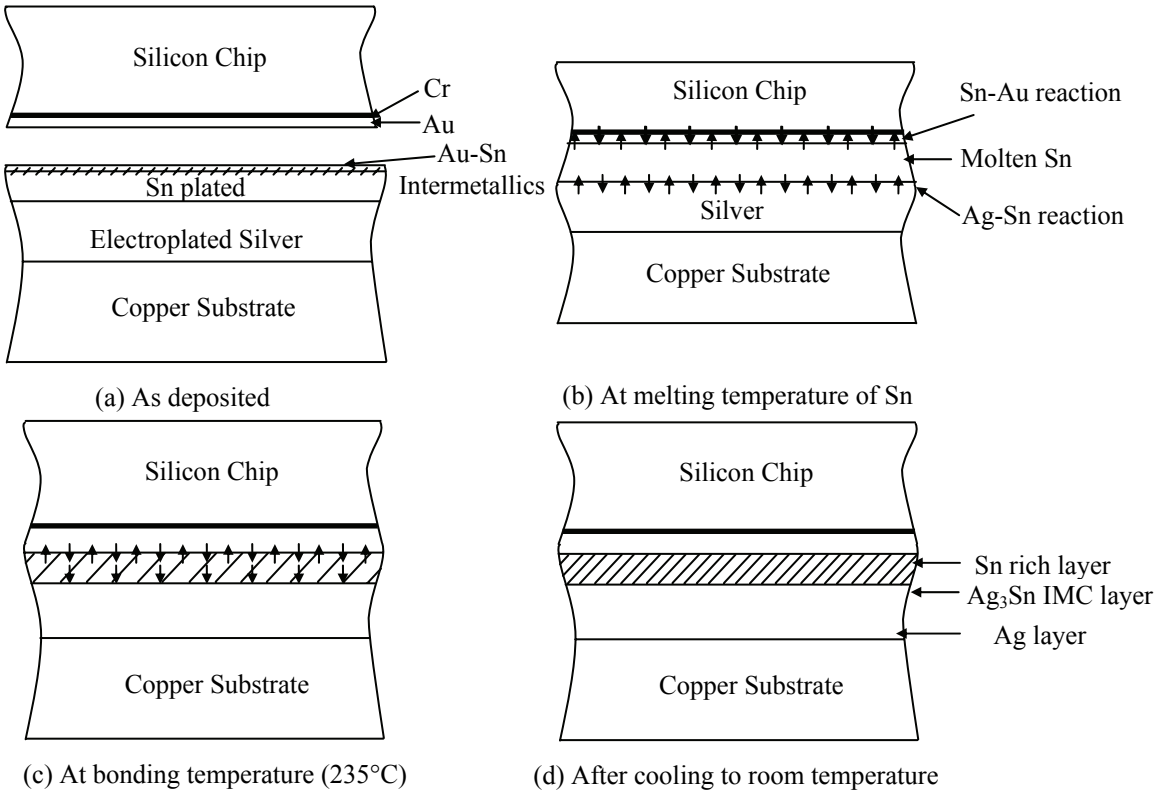


Figure 2 – Principle of the Fluxless Bonding between Silicon and Copper Using Ag-Sn-Au Multilayer Structure (Condition I)

To study the microstructure of the joint, several samples are cut in cross section and polished. Optical microscope, SEM, and EDX analysis are used to examine the cross section of these samples. Fig. 3 is the secondary electron image of a joint cross section. We can clearly see three distinct layers forming nearly perfect joint without any large void. The solder joint is quite strong. We tried to break the joint with a hand tool but the silicon chip always broke first. Layer composition is confirmed

with EDX analysis as shown in Table I. It is surprising to find that the Ag layer contains small amount of Sn, indicating that Sn atoms already penetrated through the Ag_3Sn layer and diffused into the Ag layer. Scanning Acoustic Microscope analysis will be also done to confirm this void-free joint. Re-melting temperature of the joint is expected to be around 230ºC due to the existence of Sn-rich layer.

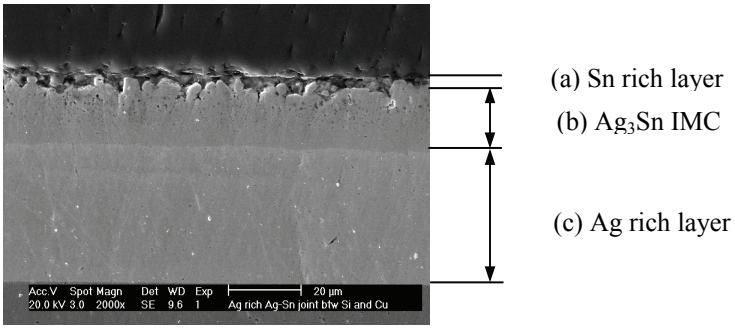


Figure 3 – SEM Cross-Sectional Image of the Initial Joint Showing Three Distinguished Layer (a) Sn Rich Layer (b)Ag_3Sn IMC Layer (c) Ag Rich Layer

Table I – EDX Spectra of Three Bonding Layers

	Atomic %		Weight %	
	Sn	**Ag**	**Sn**	**Ag**
(a) Sn-rich	**75~78 %**	**5~15%**	**73~84%**	**2~13%**
(b) Ag_3Sn	**26~27%**	**63~64%**	**27~29%**	**60~62%**
(c) Ag-rich	**4~8%**	**84~87%**	**4~8%**	**82~85%**

Bonding Failure – Condition II (Longer reflow time)

Figure 4 shows the schematic figures of the same structural bonding with longer reflow time. The bonding peak temperature is increased up to about 250°C, which is 15°C higher than that of condition I and the reflow time is about 15 minutes. As temperature increases towards the bonding temperature of 250°C, the Sn layer melts first at around 230°C and this molten Sn dissolves the upper $AuSn_4$ layer, as shown in Figure 2(b). Simultaneously, the molten Sn would react with thick Ag layer underneath to form Ag_3Sn intermetallic compound layer. However, with long enough reflow time, the entire molten Sn is consumed in liquid-solid interaction to form thick Ag_3Sn layer. Thus final joint is comprised of Ag_3Sn intermetallic layer and Ag-rich layer. As a result, there is an interface of Si/Cr and Ag_3Sn layer, which turns out to be the weak link of the structure and the joint breaks along this interface, as displayed in Figure 4 (d). While Sn-rich Sn-Ag alloys bond well onto Si/Cr surface, the Ag_3Sn layer does not seem to bond strongly to the Cr layer deposited on the Si chip. On the other hand, we need to keep in mind that there are high stresses developed in the bonded structure, simply because of the large thermal expansion mismatch between Si and Cu. The bond between Ag_3Sn layer and Cr layer on Si chip may be quite strong, but just not strong enough to resist the high stresses. Finite element analysis will be performed to compute the stresses developed. Further investigation is needed to evaluate the failure mechanism.

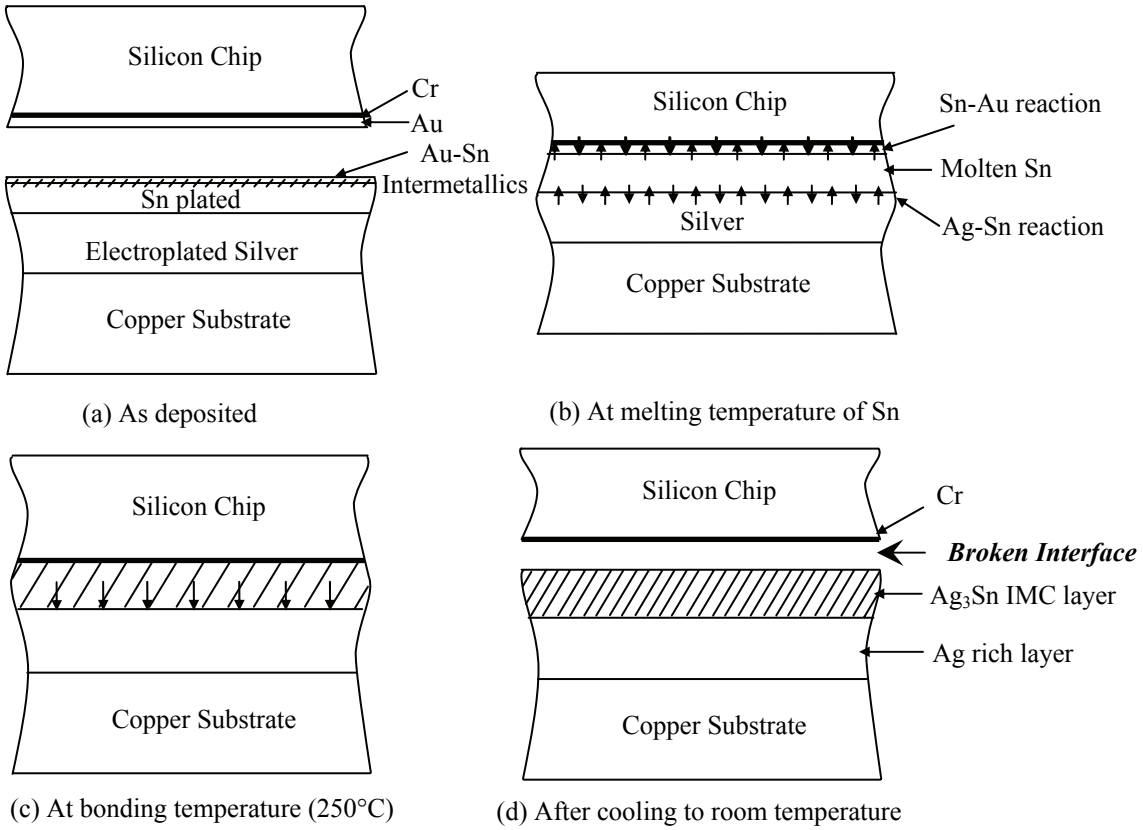
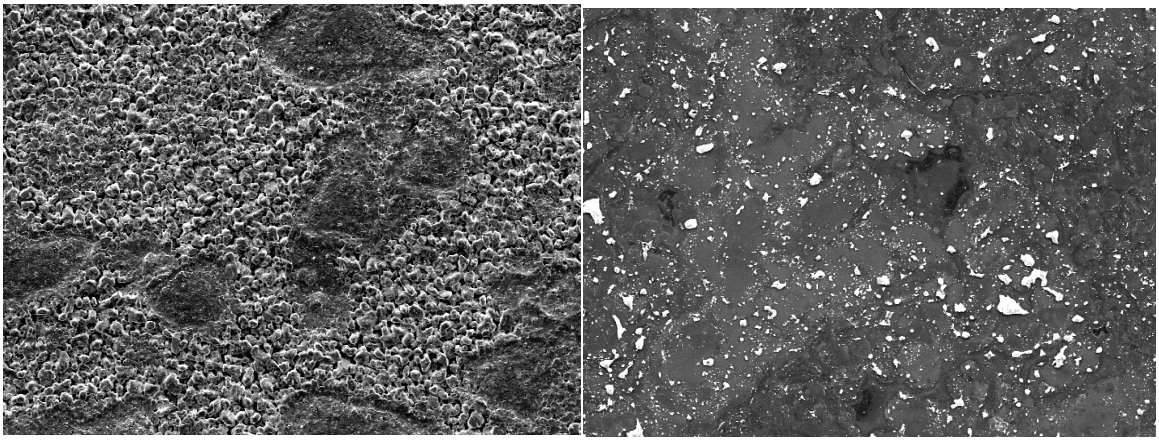


Figure 4 – Principle of the Fluxless Bonding between Silicon and Copper using Ag-Sn-Au Multilayer Structure (Condition II)

Broken interface between Ag_3Sn and Cr layer is confirmed with EDX and SEM analysis as shown in Figure 5 and Figure 6. Figure 5 (a) shows the top surface of the broken interface on copper substrate side, and Figure 5 (b) shows the outer surface of the broken interface on silicon side. EDX data are displayed in Table II (a) and (b). On copper substrate side, we can easily detect Ag_3Sn compound. On silicon side, EDX mainly detects silicon with very little chromium, but this is due to very thin Cr layer comparing to the E-beam penetration depth of more than 1μm. Figure 6 displays the SEM image on the cross section of a broken sample. It is seen that the Si chip is detached completely from the joint. For the remaining joint left on the Cu substrate, the Ag_3Sn layer has grown to 45μm. The microstructure of this layer and the broken upper surface will be carefully examined. We would then come up with a new design that would either strengthen the weak interface or eliminate it.



(a) (b)

Figure 5 – SEM Image (Top View) of the Broken Interface (a) Copper Side (b) Silicon Side

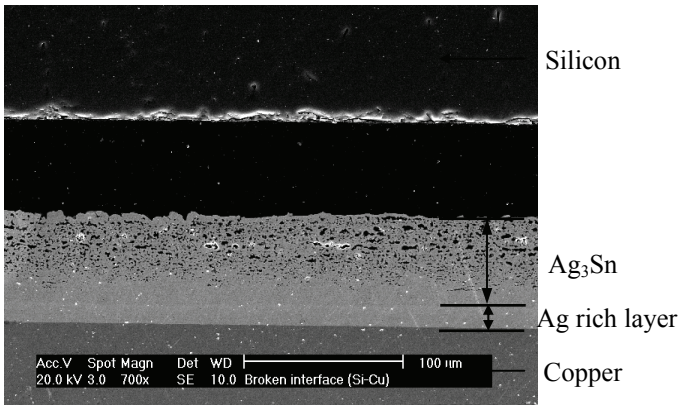


Figure 6 SEM Image on the Cross Section of a Broken Sample

Table II (a) EDX Spectra on Broken Cu Side

	Atomic %	
	Sn	Ag
(a) copper side	64~67 %	24~27%

Table II (b) EDX Spectra on Broken Si Side

	Atomic %	
	Si	Cr
(b) silicon side	90~95 %	5~10%

Summary and Future Work

In this study, fluxless bonding between silicon and copper using Sn rich Ag-Sn-Au alloy has been successfully developed. The Cu substrate is coated with a thick silver layer as stress buffer. It is proven that proper design and bonding condition can overcome the severe thermal expansion mismatch between silicon and copper, while more reliability tests need to be done. Electroplating method becomes useful in depositing thick solder layer and this method seems more cost effective comparing to the evaporation technique in vacuum. The fluxless process developed in this project offers the packaging industries attractive means for devices that cannot be exposed to fluxes. The reliability tests such as thermal cycling will be performed. Further study on microstructural change with proper annealing condition is also necessary to delve into. We hope that our initial works on this fluxless bonding between silicon and copper provide an innovative method to the packaging industries for many applications.

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