Accelerated Reliability Testing and Analysis of Lead Free Solder Interconnects

Jim Wilcox
IBM Corporation
Endicott, NY USA

Glenn Dearing
Endicott Interconnect Technologies
Endicott, NY USA

Brian Smith
Celestica Ltd.
Holmes Chapel, Cheshire, UK

Thomas Skoczowski
Siemens
Bruchsal, Germany

Thilo Sack
Celestica, Inc.
Toronto, Ontario, Canada

Bob Sullivan
HDPug International
Scottsdale, AZ USA

Abstract
The Pb-free solder interconnect reliability performance of a wide variety of common SMT component types was measured in an IPC-9701 TC1 thermal cycle (0-100°C / 40 min cycle). Seventeen different Pb-free SMT components were evaluated, including PBGAs, CBGAs, CCGAs, power modules, QFPs, PLCCs, CSPs, chip capacitors and resistors. All were attached to a six layer PCB using SAC387 solder paste according to the HDPug GPLF defined assembly process. This study specifically compares the reliability behavior of these various component types when subjected to expected Pb-free assembly process extremes such as minimum peak reflow temperature and extended reflow soak times. Microstructural features of as-assembled SAC solder connections are first explored. Failure data is reported for the various component types and assembly conditions. All SAC solder thermal cycling data was collected along with eutectic SnPb solder controls.

Introduction
High Density Package User Group (HDPug) is a collaborative consortium of industry members intent on identifying and resolving technical challenges associated with producing higher complexity electronic products. The HDPug General Purpose Lead Free (GPLF) initiative evaluates the performance of higher complexity PCBAs through realistic assembly manufacturing conditions. It necessarily incorporates a substantial range of expected process variability, exploring the minimum solder reflow temperature requirement for reliable SnAgCu (SAC) board level interconnects. It explores the relation between peak reflow temperature, reflow soak time and the resultant solder interconnect reliability. It evaluates the compatibility of a variety of component surface finishes, both Pb free and Pb bearing, that may be encountered in the industry transition to Pb-free card assembly. It further is intended to generate a set of Pb-free assembly process recommendations supported by appropriate reliability data.

This paper comprises an interim status report of the HDPug GPLF project. Specifically, it provides some metallurgical highlights of the Pb-free solder interconnects on the as-assembled GPLF test boards along with a description of the electrical failures resulting from 6000 cycles of an IPC-9701 TC1 accelerated thermal cycle.

GPLF Test Vehicle
As recounted in a companion process study [1], the HDPug General Purpose Lead Free (GPLF) test vehicle is designed to simulate a moderately complex PCBA product and be processed through a realistic manufacturing environment. It consists of a

2S4P, 1.7 mm thick, high Tg, printed circuit board (PCB) with stitch nets through the component solder interconnects. Components are wired on front and back to monitor the interconnect reliability in a total of (72) components. The stitch circuitry on the PCB is routed primarily on the external planes to minimize confounding of solder joint failures with internal PCB via failures. Consequently, the test results reported here cannot be used to assess the overall reliability of a fully assembled Pb-free circuit board. They should be viewed as an assessment of solder joint performance only. PCB via reliability following Pb-free assembly exposure has been explored in a separate HDPug study and reported in [2].

By design, the GPLF test board samples a broad spectrum of industry package types and surface finishes. It is populated with (17) different testable SMT component types provided by eight different suppliers and other non-testable passives and components from four additional suppliers. Testable leadframe packages include QFP, LQFP, SOIC, and PLCC using six different surface finishes. Array packages include both ceramic (CBGA, CuCGA) and laminate based (PBGA, CSP) of varying body sizes. All components were attached to the immersion Sn finish PCB with a double side SMT assembly process. Both front and back side were populated with various chip resistors and capacitors that were not electrically monitored. Components were arranged on the PCB with high and low density regions to simulate the range of process thermal history that could be expected in functional board designs. (Testable component types and surface finishes are listed in Tables 2 and 3 below.)

Sample Process History

One fundamental objective of the GPLF project was to establish PCBA reliability performance over a range of process thermal exposures that might be experienced in a volume manufacturing environment. A variety of process thermal exposures were therefore designed into this experiment. As described in [1], a standard SAC reflow profile was defined as one producing a peak temperature in the range of 232 to 250°C for all solder joints with a time above the SAC liquidus (217°C) ranging from 60 to 90 seconds.

Several realistic manufacturing deviations from the nominal SAC reflow profile were examined as individual experimental cells. These include two different minimum peak temperature profiles along with an extended soak profile. The profiles are tabulated in Table 1 along with the minimum temperature of the largest component solder joint and the maximum temperature of the small components; two temperatures that bound the overall reflow profile. See [1] for additional details. Increasing board design complexity clearly raises the process temperatures required and, to the extent that SAC microstructure is dependant on peak reflow temperature; increased complexity boards presumably encompass a wider range of solder joint microstructures.

Table 1 - T_{peak} of Solder Joints on Large and Small Components for The GPLF Experimental Reflow Profiles

Increasing Peak Reflow Temperature →				
GPLF SAC Reflow Profile:	Minimum Peak T (small components)	Standard SAC	Minimum Peak T (large components)	Extended Soak (large components)
Largest mass component:	PLCC 68	PLCC 68	CBGA 1657	CBGA 1657
T_{peak} , largest component:	224°C	231°C	225°C	232°C
T_{peak} , small comp. (Al cap):	236°C	246°C	252°C	259°C
Component Temp. Range (□T):	12°C	15°C	27°C	27°C

GPLF test boards were assembled by Siemens (Bruchsal, Germany) with five different SAC reflow conditions (the four of Table 1 and a 231°C vapor phase reflow) along with four conventional eutectic SnPb assemblies. Two different no-clean solder paste formulations, both using a Sn3.8Ag0.7Cu solder composition, were included in the design of experiments [1].

Fifty boards were evaluated in the first phase reliability evaluation being reported here. Phase I boards were subjected to Accelerated Thermal Cycling in the as-assembled state. No thermal aging was done prior to thermal cycling. An additional fifty boards were set aside for a second phase of reliability testing that will be reported elsewhere.

As-Assembled Solder Interconnects

Prior to reliability testing, representative microstructures of the solder interconnects in the as-assembled state were examined for all component types. With the exception of solder joint geometry views, the photomicrographs included in this section are all secondary electron SEM images scaled to a constant marker length for direct visual comparisons of microstructures. Several different categories of component solder joints are discussed: leadless passives, leadframe components, and area array interconnect. On a typical PCBA, these classes of components can have substantially different surface finishes, joint geometries, and solidification cooling rates and therefore may exhibit noticeably different solder microstructures.

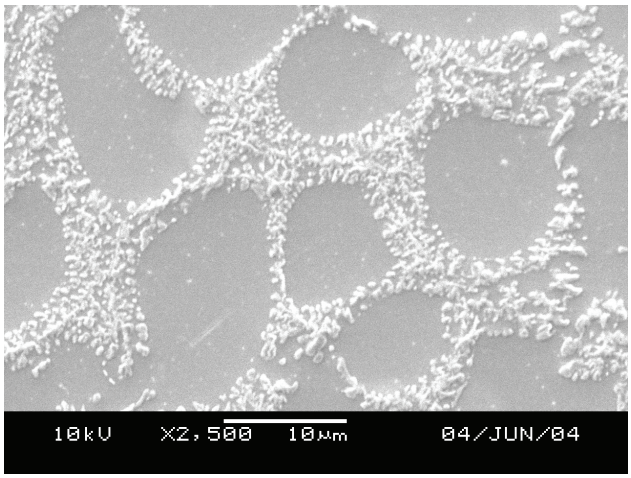
Basic SnAgCu Microstructure

The solidification behavior of near-eutectic SnAgCu solder has been previously described by Henderson, et al. [3]. The ternary eutectic phases that form on solidification are primary □-Sn and two intermetallic phases, Ag_3Sn and Cu_6Sn_5. The □-Sn takes

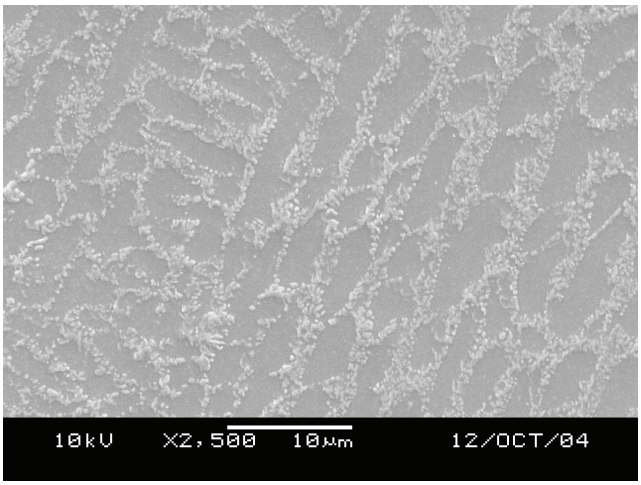
the form of primary solidification dendrites. The two intermetallic phases precipitate in the interdendritic spaces on final solidification, usually with a fine particulate morphology.

Of primary consideration in the evaluation of solder joint microstructure is the overall solder composition, the substrate surface finishes, the peak reflow temperature, and the cooling rate through the liquidus temperature. A fusible surface finish may slightly change the bulk solder composition, as would be the case for a SnPb or SnBi finish. It could also influence the nucleation kinetics of the primary □-Sn phase. Delayed Sn nucleation results in a large undercooling of the liquid which produces extremely rapid crystallization of Sn, often producing very large grain—even single crystal—solder joints. (Recognize though that one cannot deduce Sn grain size from the SEM photos used in this report. A single Sn grain encompasses large numbers of crystallographically identical dendrite arms. Individual Sn grains can be best viewed using optical microscopy with cross-polarizers. [4])

It is important to recognize that while we have defined a 'Standard SAC reflow profile' for the GPLF study, every solder joint on the board experiences its own unique thermal history. This is clearly evident when comparing different size solder joints from any given board. Figure 1 compares a large (~900□m) BGA solder joint and much smaller 0402 chip capacitor solder joint formed on the same board. Both exhibit an obvious dendritic solidification. The dendrite morphology remains largely unchanged between the two, it simply varies in scale. Dendrite arms become finer as heat is extracted at a faster rate.



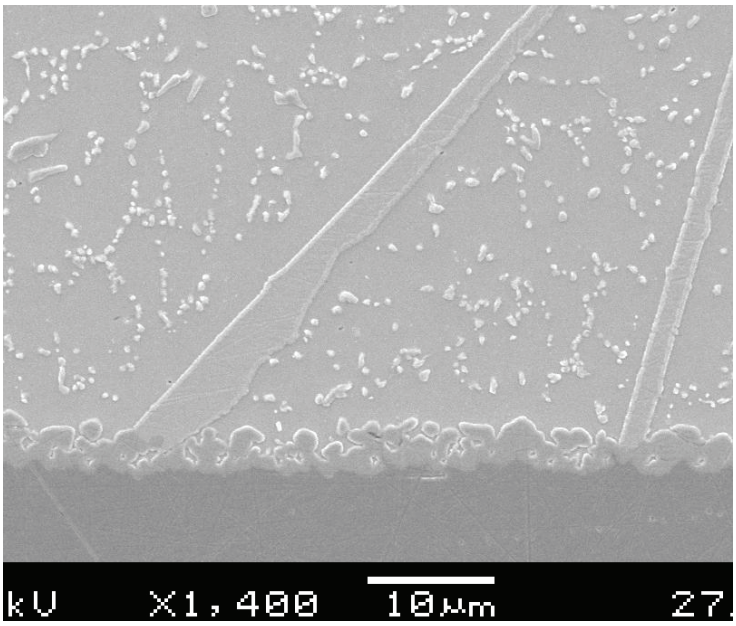
[33:D4] PBGA 420, Standard SAC reflow – front side
(a)



[33:C22] 0402 Chip Capacitor, Standard SAC reflow
(b)

Figure 1 - Effect of Solidification Thermal Gradient on □-Sn Dendrite Morphology: Large and Small SAC Solder Joints on The Same Board

Using the GPLF standard SAC reflow profile, □-Sn secondary dendrite arm spacing of roughly 12□m is produced in the BGA ball (Figure 1a) while an approximately 3□m spacing is produced in more rapidly cooled 0402 chip capacitor solder joint on the same board (Figure 1b). Dendrite arm spacings are known to be inversely proportional to the solidification cooling rate to roughly the ½ power [5], implying a factor of about 16X in cooling rate between these two joints. Despite the difference in microstructure scale, the relative volume fractions of intermetallic phases in the interdendritic spaces are relatively unchanged. That volume fraction is determined by the bulk solder composition at solidification, not the cooling rate.



[85:D16] CBGA 937 / Minimum T_{peak} (large components)

Figure 2. Ag_3Sn plates in a SAC387 BGA solder ball. Volume fraction of interdendritic phases has been reduced through Ag consumption in the plates.

During the solidification of higher Ag content SAC alloys (such as the Sn3.8Ag0.7Cu alloy used in the GPLF study), the Ag_3Sn phase may crystallize first. Delayed nucleation of the □-Sn phase can allow time for significant growth of proeutectic Ag_3Sn platelets into the liquid before the Sn ultimately crystallizes. As reported by Snugevsky et al. [6], higher peak reflow temperatures of SAC solder increases the observed undercooling of liquid before Sn crystallization on subsequent cool down. Such increased liquid undercooling allows more time for Ag_3Sn plate formation before its growth is halted by the solidification of Sn. Ag_3Sn plates are thus likely to be associated with a thermally massive component, (*e.g.*, CGBA), using high Ag content solder balls, heated to high peak reflow temperature. As shown in Figure 2., Ag_3Sn platelet formation can indeed be seen in the SAC 387 solder balls of the CBGA components.

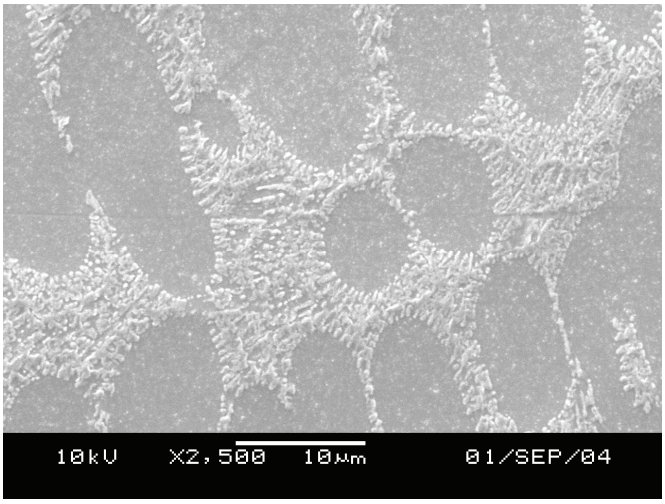
Extensive Ag_3Sn platelet formation removes Ag from the bulk liquid solder and reduces the formation of the fine interdendritic Ag_3Sn particles. Comparing the microstructures of Figure 2 (with Ag_3Sn plates) to Figure 1 (without Ag_3Sn plates), the volume fraction of interdendritic intermetallic phases can clearly be seen to have been reduced through the growth of proeutectic Ag_3Sn plates. Reducing the volume fraction of interdendritic Ag_3Sn particles (a primary bulk strengthening phase) will produce a softer solder joint.

With this basic review of SnAgCu metallurgy as foundation, we can explore the range of microstructures possible in a typical printed circuit board assembly as represented by the GPLF test vehicle.

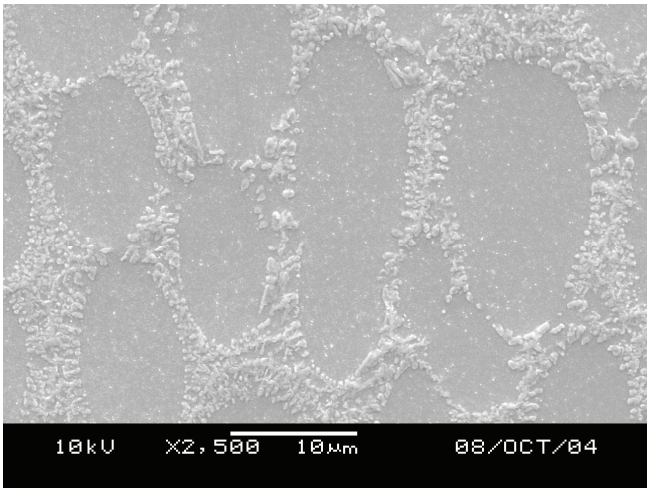
Array Components

Large BGA components are often the most thermally massive component on a board and therefore determine the minimum reflow profile required for adequate assembly. They often have the lowest peak solder joint reflow temperature and the least dwell time above liquidus on the board. They likely experience the slowest cooldown rate as well.

The 35x35 mm plastic BGA package (PBGA 420) with SAC solder balls was assembled to both front and backsides of the GPLF test board. These sites were populated for nearly all of the experimental SAC reflow profile trials (omitting Min. T_{peak} – small). SAC solder microstructures from all reflow cells exhibit a notable similarly in morphology with perhaps minor variations in characteristic scale based on the individual joint thermal history. Very few proeutectic Ag_3Sn plates were observed in these PBGA solder joints, such that effectively all the Ag remaining in the solder at Sn crystallization precipitates in the interdendritic regions as Ag_3Sn particles. A typical PBGA SAC solidification microstructure is shown in Figure 3a.



[38:D4] PBGA 420, Standard SAC reflow – front side
(a)



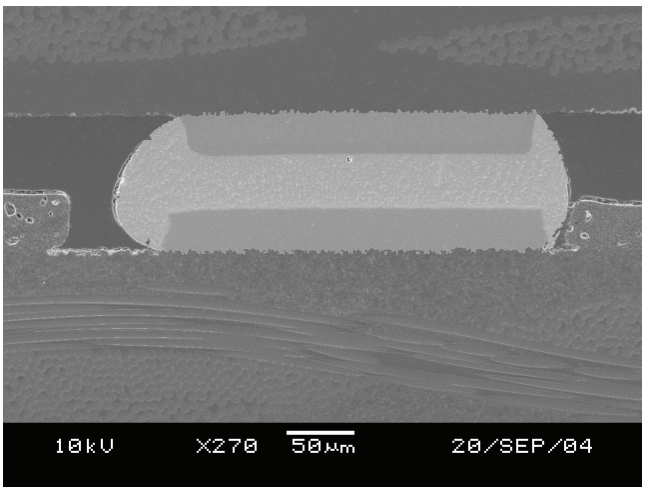
[33:D35] PBGA 420, Standard SAC reflow – back side
(b)

Figure 3 - PBGA 420 Solder Joint Microstructures (SAC BGA Ball Attached with SAC387 Paste) Attached with Standard SAC Profile on Front and Back Side of GPLF Board

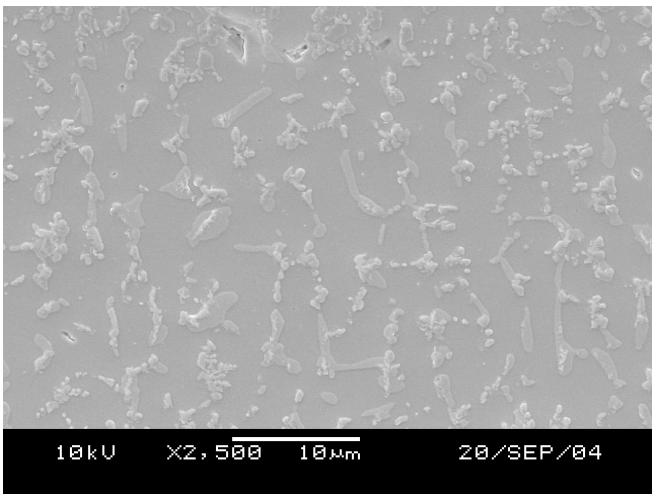
The final solidification microstructure is characteristic almost solely of the bulk solder composition and the thermal history (time, temperature, and temperature gradients.) Note for instance in Figure 1a, the identical microstructure is replicated on a different board using the same reflow profile but with a different SAC387 solder paste formulation. Similarly, if the solder composition remains unchanged, the solidification microstructure should be replicated on multiple reflows with the same profile. This characteristic is illustrated in Figure 3b. comparing the backside PBGA solder joint with that on the front side (Figure 3a) and realizing that the backside component has been reflowed twice to accommodate the second side assembly. The second reflow can be seen to produce effectively the same microstructure as the single reflow.

At the opposite extreme of the array component scale is the 24 I/O land grid chip scale package. The CSP 24 is a very small component (3.5 x 4.5 x 1.0 mm) located in an isolated region on the corner of the GPLF test board. It therefore experiences the largest extremes of temperature during a reflow operation. It heats rapidly, reaches extreme peak temperatures and then cools rapidly. Given the limited length of the seven zone reflow oven used here, the higher peak temperatures must correspond to faster cooling rates as the component exits the heating zone.

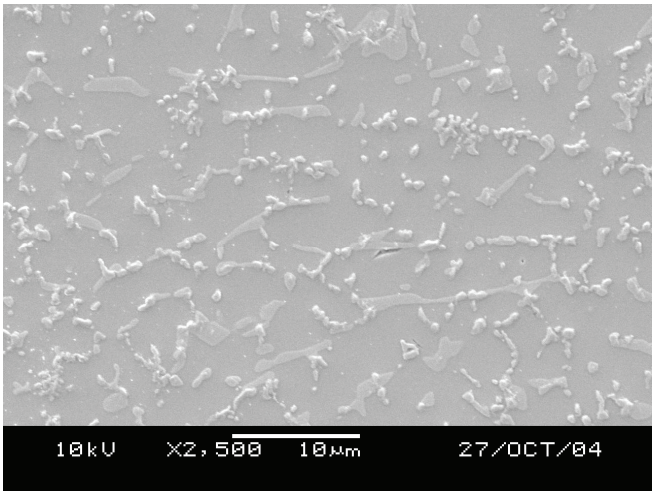
Using samples from the various GPLF reflow profiles arranged in sequence of increasing reflow temperature, Figure 4 illustrates the metallurgical consequences of increasing peak temperature and cooldown rate. Most notable is the absolute difference in microstructural scale in a CSP solder joint from that of the larger, slower cooling PBGA solder joints shown above in Figure 3. Clearly visible are the two distinct eutectic solidification intermetallics, Ag_3Sn and Cu_6Sn_5, that precipitate between the primary □-Sn dendrites (*cf.*, Figure 4c). But also apparent in Figure 4 is the slight but measurable decrease in dendrite spacing on progressing from 243°C cooldown structure in (b) to a 253°C cooldown structure (d).



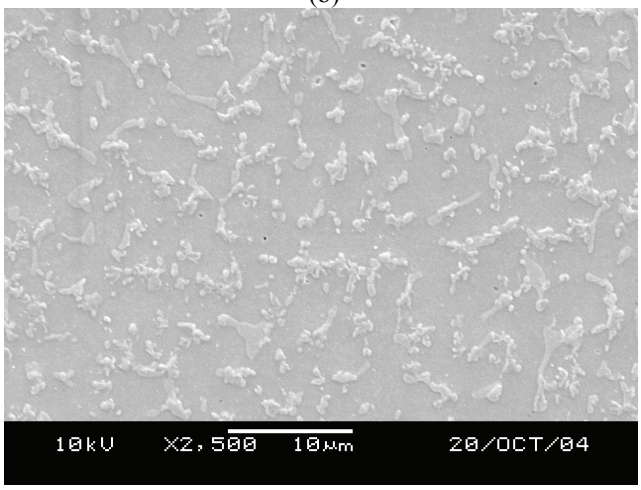
[106:D12] CSP 24 Landgrid solder joint.
(a)



[106:D12] CSP 24 Landgrid / Minimum T_{peak} (small)
(b)



[85:D12] CSP 24 Landgrid / Minimum T_{peak} (large)
(c)



[49:D12] CSP 24 Landgrid / Extended soak reflow
(d)

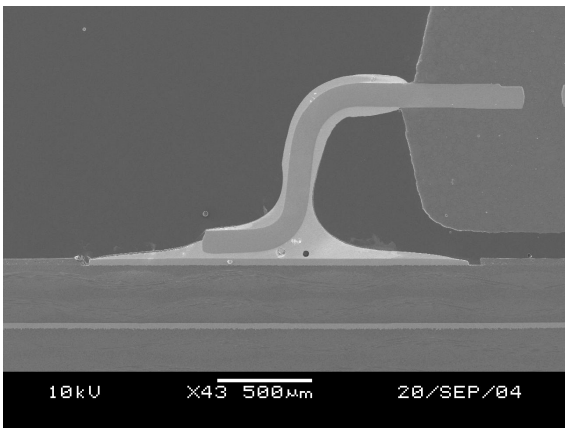
Figure 4 - CSP 24 Land Grid Solder Joints (a) Typical Solder Joint Geometry, (b) Minimum Peak (Small Components), T_{peak} = 243°C, (c) Minimum T_{peak} (Large), T_{peak} = 246°C, (d) Extended Soak Profile, T_{peak} = 253°C.

Leadframe Components

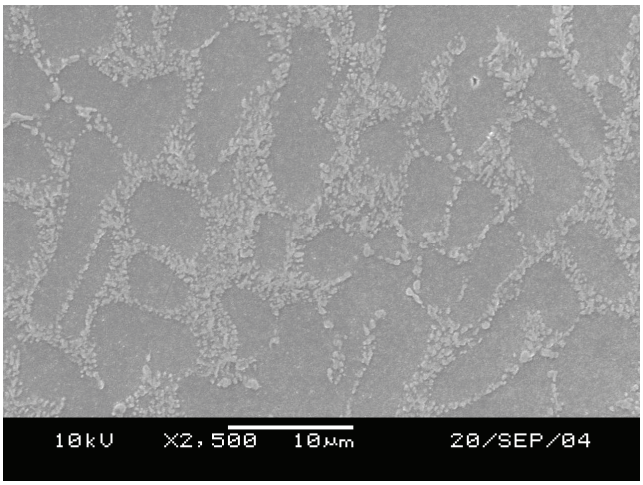
Leadframe components, with fine pitch metal leads soldered to the PCB external to the package footprint, can impart a significantly different thermal process history to SAC solder joints than do area array components. They often reach higher peak reflow temperatures, have longer reflow dwell times and impose higher cooling rates. They are supplied to the industry with a wider array of surface finish options. And, based simply on solder volume considerations, leadframe solder joints may be prone to a greater impact of fusible surface finishes on the bulk solder composition and the microstructure of the solder joint.

The GPLF test board is populated with five different leadframe component types. These fall roughly in two size classes, relatively small: LQFP48 (74 mm^3), LQFP100 (333 mm^3), SOIC28 (338 mm^3), and relatively large: QFP208 (2509 mm^3) and PLCC68 (2813 mm^3). Representative solder joint microstructures from these size classes are shown in Figures 5 and 6.

Figure 5a shows the package leadframe solder joint in a 100 I/O, 0.5 mm pitch, LQFP. Using the Minimum T_{peak} reflow profile (for small components) on a GPLF board, these joints reach a peak reflow temperature of 232°C. The resultant SAC microstructure for Sn surface finish is shown in Figure 5b. A dendrite arm spacing of ~4 □m implies a solidification temperature gradient intermediate to the PBGA and chip passive solders joints examined in Figure 1.



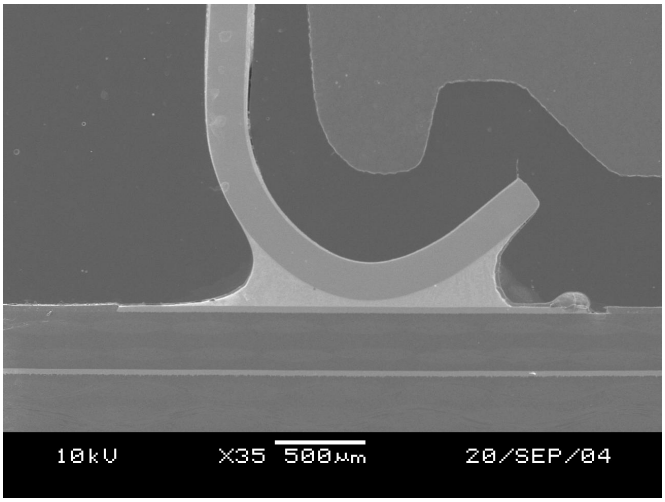
[106:D6] LQFP 100 Sn finish / min. T_{peak} (small) reflow
(a)



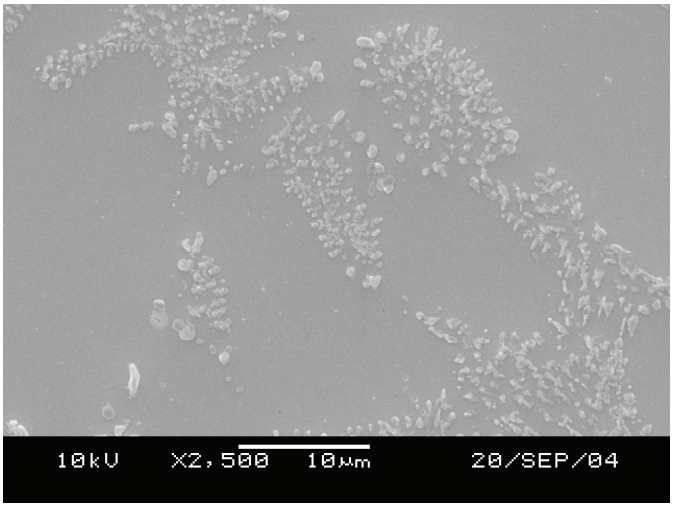
[106:D6] LQFP 100 Sn finish / min. T_{peak} (small) reflow
(b)

Figure 5 - SAC Solder Joints – Small Body Leadframe Package

The 28x28 mm^3 PLCC 68 is a relatively massive leadframe component. The solder joints formed on the ends of the PLCC leads are thermally shielded by the package body (Figure 6a). This configuration limits the peak reflow temperature of the solder (in this case to 224°C) but also impedes the cooldown rate. As can be seen in Figure 6b, the resulting □-Sn dendrites are very coarse indeed. Larger in fact than those observed in the larger footprint 35x35 mm^3 PBGA 420 joints (Figure 3). This can be rationalized simply by comparing the effectiveness of the thermal shielding provided by the package body in both cases. The thickness of the molding compound above the PLCC joint is 3.2 mm, while the package thickness of the PBGA body is closer to 2.0 mm.



[106:D24] PLCC 68 Sn finish / min. T_{peak} (small) reflow
(a)

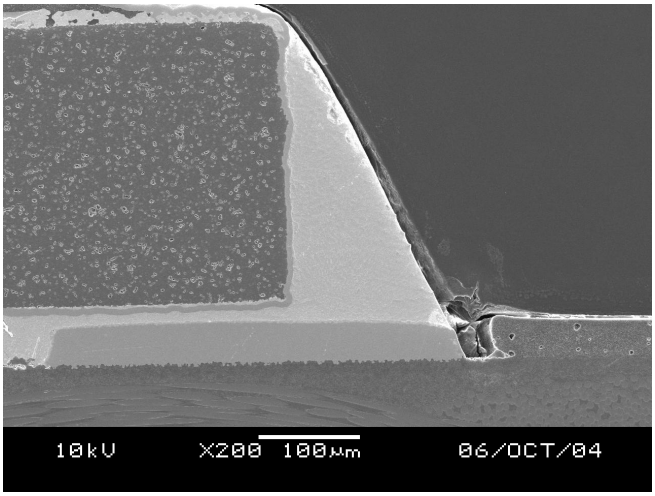


[106:D24] PLCC 68 Sn finish / min. T_{peak} (small) reflow
(b)

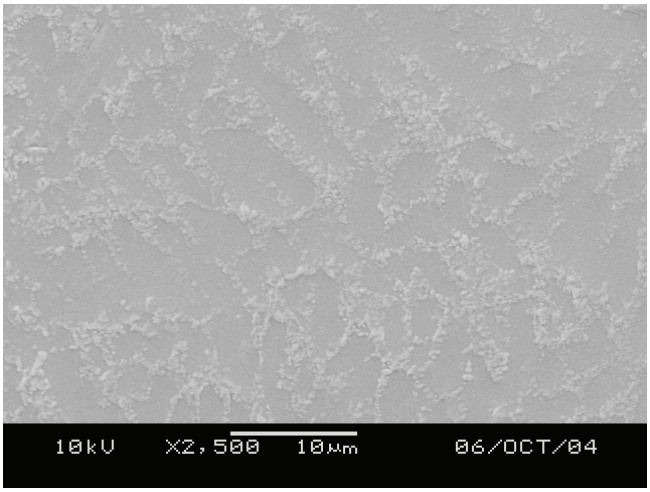
Figure 6 - SAC Solder Joints – Large Body Leadframe Package

Leadless Passives

The GPLF test board includes a variety of passive components such as aluminum capacitors, chip resistors, and tantalum chip capacitors, all of varying sizes. Most produce SAC solder joints with fine dendritic microstructures indicative of solidification through a steep thermal gradient. The relative volume fraction of intermetallic phase formed on final solidification is similar to the seen in other SAC387 joints on the GPLF boards. Typical might the 0402 chip resistor solder joint shown in Figure 7.



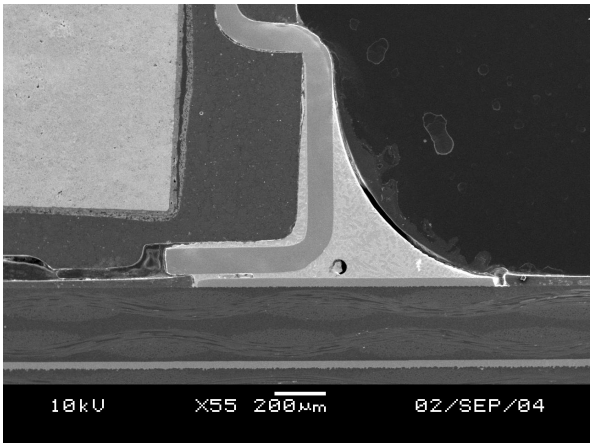
[33:R1] Chip Resistor 0402, Std SAC reflow -- front side
(a)



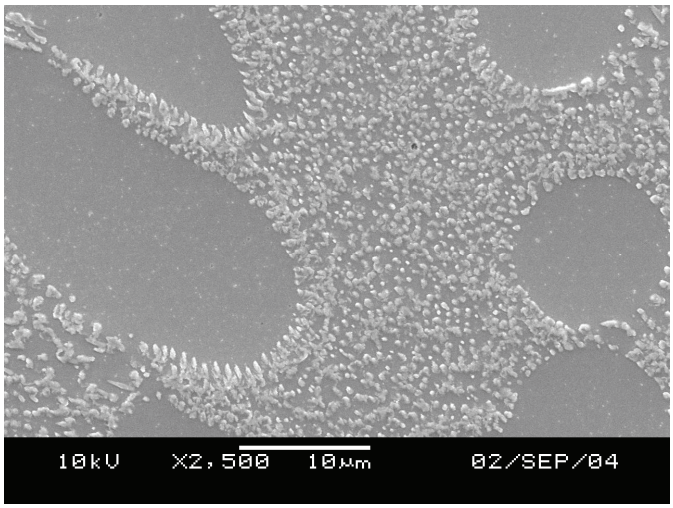
[33:R1] Chip Resistor 0402, Std SAC reflow -- front side
(b)

Figure 7 - 0402 Chip Resistor Solder Joint

The tantalum chip capacitors also produce the typical SAC dendritic solidification structure but on a markedly different scale. These capacitors were included at three dimensions, A, B, and C. (See Figure 8a). Solder joints on this component all had microstructures with widely spaced, small diameter primary □-Sn dendrites along with a clearly much larger volume fraction of interdendritic second phases when compared to other SAC joints on the GPLF boards (*c.f.*, Figure 1). This increased intermetallic volume fraction is shown in Figure 8b. It was apparent with all three sizes of Ta capacitor and at all reflow conditions. Despite having a Sn finish on the component soldered surface, the bulk SAC solder composition is evidently enriched in Cu, Ag or both. The source of this apparent compositional change is unclear at this time but it would indicate a much harder solder joint then is produced on other components in this study.



[38:F1] Ta chip capacitor A, Sn finish/Standard SAC Reflow
(a)



[38:F1] Ta chip capacitor A, Sn finish / Standard SAC Reflow
(b)

Figure 8 - Tantalum Chip Capacitor A Solder Joint

Interconnect Mechanical Integrity

An evaluation of the Pb-free solder joint mechanical integrity was performed in the as-assembled state. Leadframe components (QFP, LQFP and SOIC) were subjected to leadpull measurements using a Dage 4000 tester. Typical sample size was (30) leads per condition (component type, reflow, and surface finish). Mean pull strength (gms) is shown in Figure 9 for these components assembled at various experimental reflow conditions. Direct comparisons of solder joint strength can obviously only be made within a constant lead geometry and component type. Effects of lead surface finish and reflow profile can be seen in Figure 9 within the individual component types QFP208, LQFP100, and SOIC28.

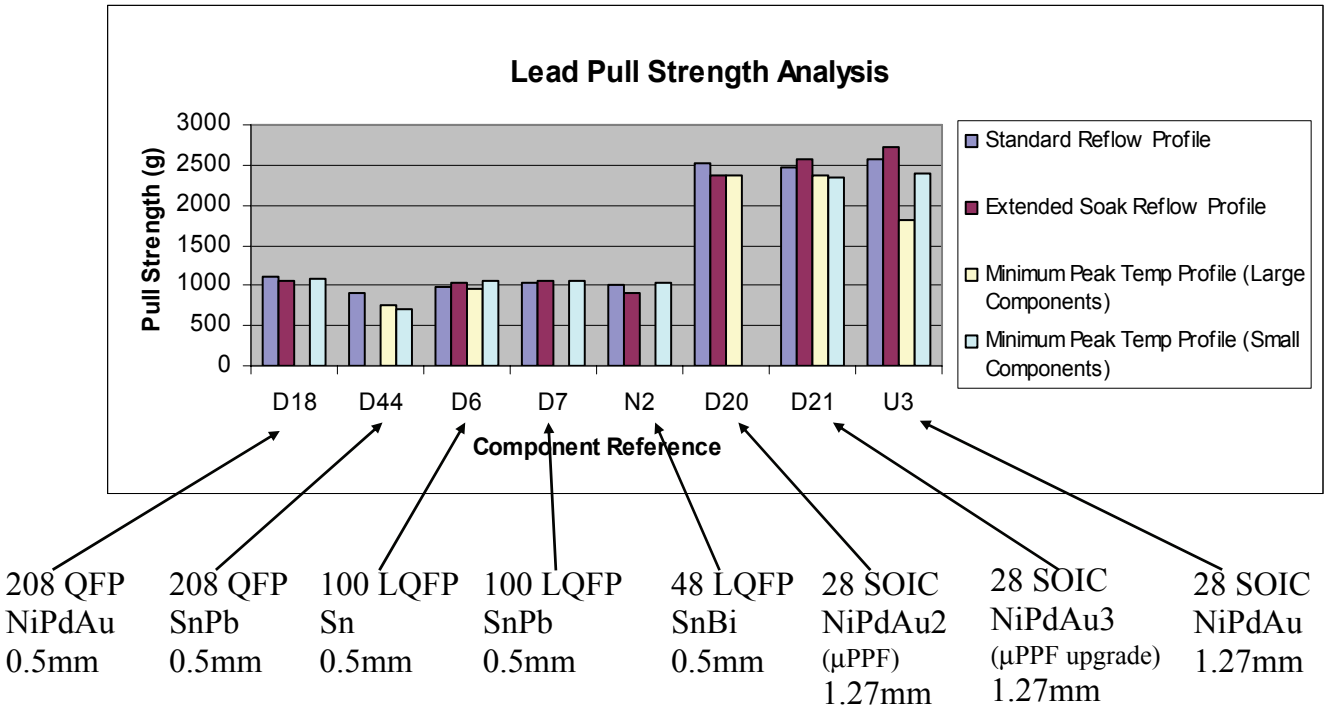
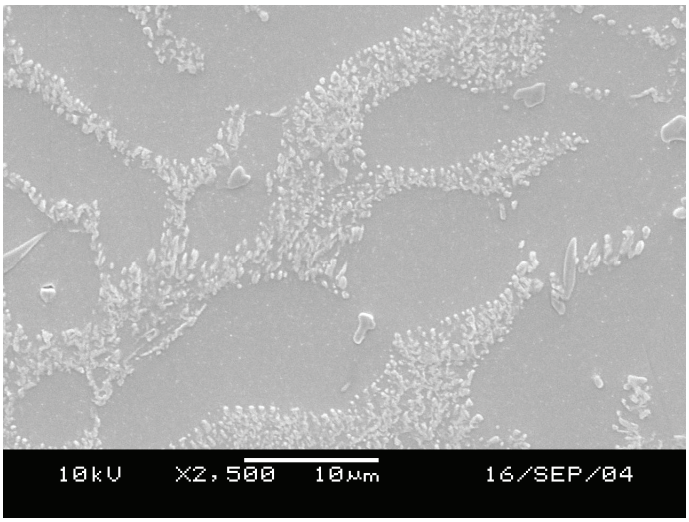


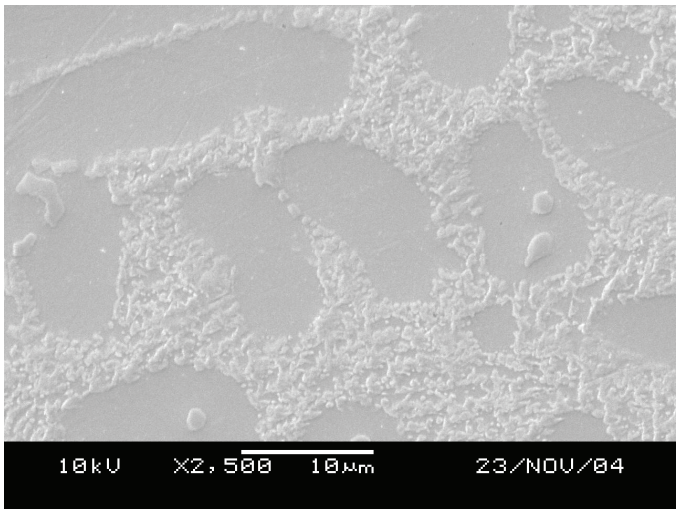
Figure 9 - Mean Lead Pull Strength (gms) for Selected Components, Lead Surface Finishes and Reflow Profiles in The As-Assembled State (No Thermal Aging)

Recognizing that the typical standard deviation for these results was in the range of 8 to 10 percent of the mean, it can be seen from Figure 9 that no significant effects of surface finish or reflow profile were evident in the mechanical strength of fully Pb-free solder joints. Perhaps not surprisingly then, little difference was noted in the SAC solder microstructures for a given component type when compared across these variables.

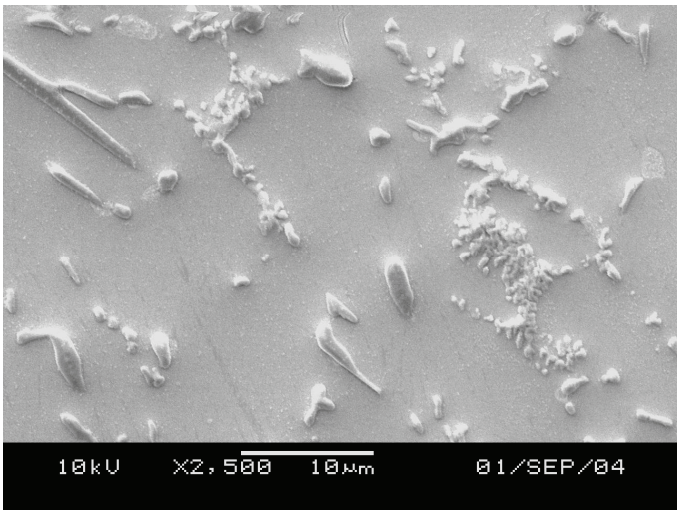
The QFP208 does exhibit some decrease in pull strength for the mixed assembly case (*i.e.*, SnPb surface finish attached with SAC solder) relative to that of a NiPdAu lead finish. The solder joint microstructures corresponding to these QFP 208 lead pull data are shown in Figure 10.



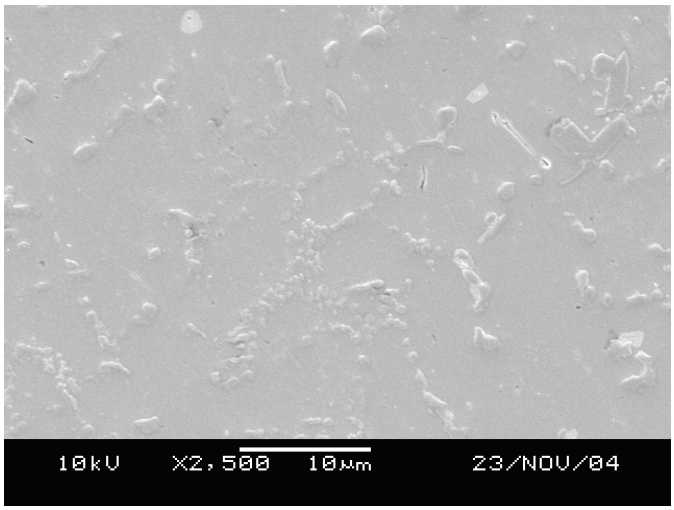
[38:D18] QFP208, NiPdAu finish / Standard SAC reflow
(a)



[106:D18] QFP208, NiPdAu /Minimum T_{peak} (small)
(b)



[38:D44] QFP 208, SnPb finish / Standard SAC reflow
(c)



[106:D44] QFP 208, SnPb finish /Minimum T_{peak} (small)
(d)

Figure 10 - Microstructures of QFP 208 Solder Joints with NiPdAu (a, b) and SnPb (c, d) Leadframe Finishes

Fine particulate intermetallic phases that precipitate in the interdendritic spaces provide a primary strengthening mechanism for the SAC solder alloy. Comparing QFP208 solder joint microstructures formed on the NiPdAu finish for both standard SAC reflow (Figure 10a) and the minimum T_{peak} reflow (Figure 10b), with those formed on SnPb finish leads, (Figures 10c and 10d), clearly reveals a much higher volume fraction of the strengthening phases with the Pb-free finish. The final solidification structure between the □-Sn dendrites with the SnPb finish also includes a soft, globular, Pb rich phase.

Similarly, shear removal loads were measured for a variety of chip resistors and capacitors in the as-assembled state. Again, the measured mechanical strength of these SAC solder joints was found to be insensitive to the reflow process variations evaluated.

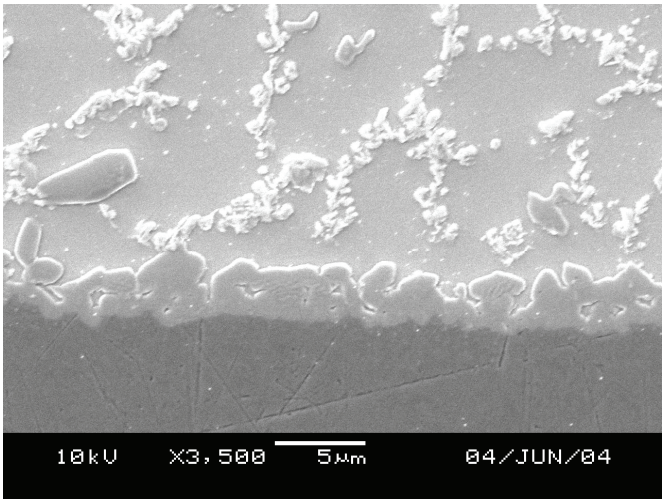
Intermetallics and Interfaces

PCB Interfaces

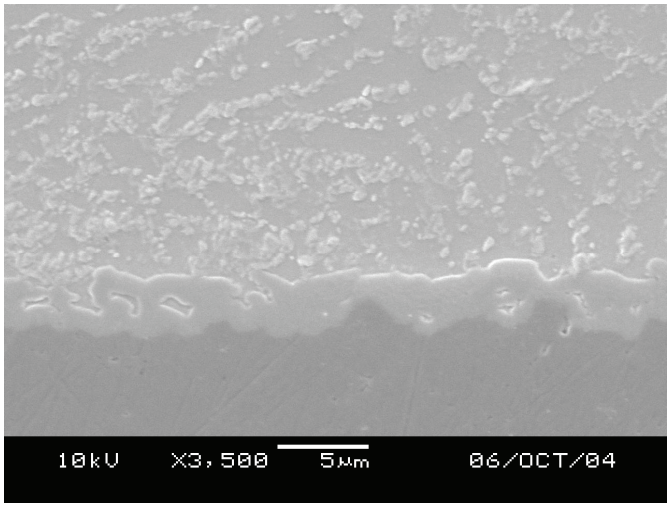
SAC387 solder was observed to uniformly wet the GPLF immersion Sn finish PCB pads. Solder intermetallic formation on these PCB pads using the Standard SAC reflow profile is illustrated in Figure 11. Included are the slower cooling joints of large components (Figure 11a) and the faster cooling joints of small components (Figure 11b). The solder joints shown are still

in the as-assembled state, without any additional thermal aging. The visible intermetallic layer is Cu_6Sn_5; no intervening layer of Cu_3Sn is yet visible.

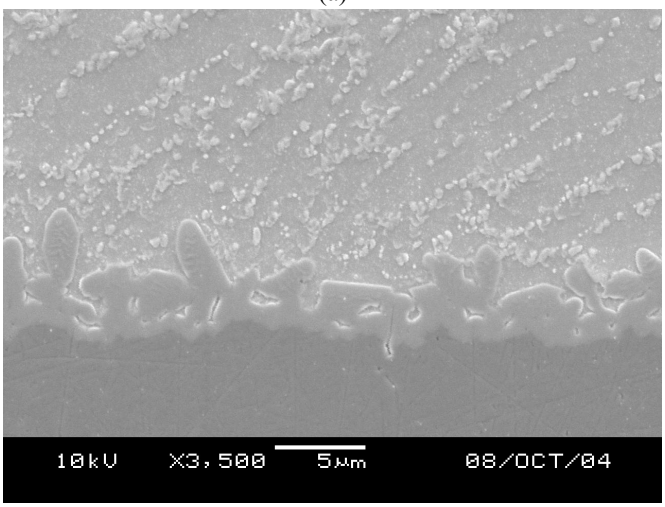
The other experimental SAC reflow profiles included in this study all produce PCB intermetallic structures that are fundamentally similar in thickness and morphology, demonstrating a relative insensitivity to that range of time and temperature variations. This relative insensitivity of intermetallic morphology to liquid contact time can be illustrated by examining the effect of multiple reflows. Comparing the PCB interfacial intermetallics arising from two reflows on the backside (Figure 11c to those experiencing a single reflow profile on front side (Figure 11d).



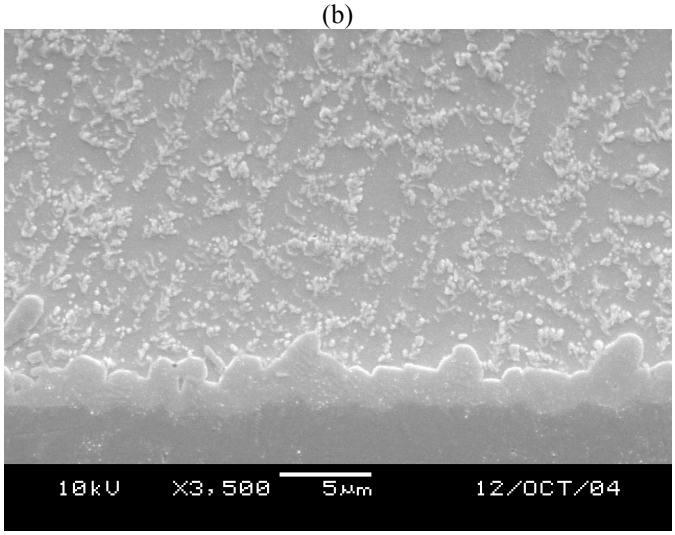
[33:D4] PCB pad intermetallic; large component – front side
(a)



[33:R1] PCB pad intermetallic, small component – front side
(b)



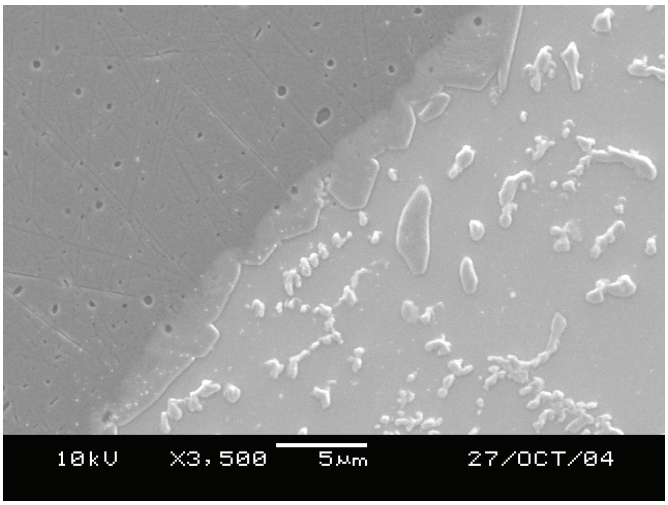
[33:D35] PCB pad intermetallic; large component –back side
(c)



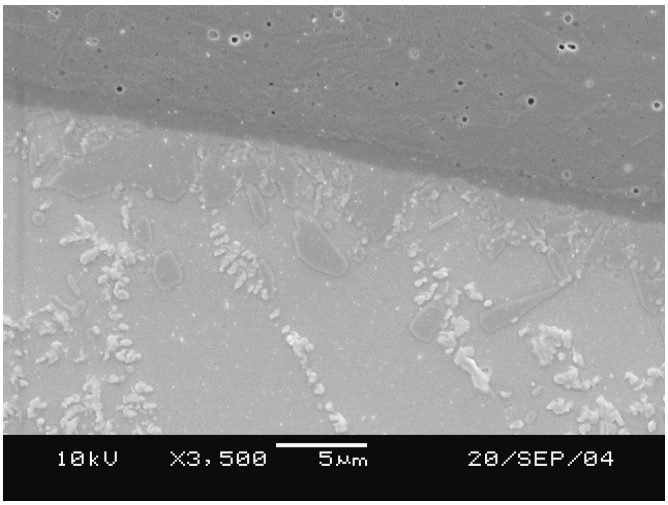
[33:C22] PCB pad intermetallic; small component – back side
(d)

Figure 11 - PCB Copper Pad Intermetallic Formation with The Standard SAC Reflow Profile. Cu_6Sn_5 Forms in a Continuous Layer to Approximately 3□m Thickness.

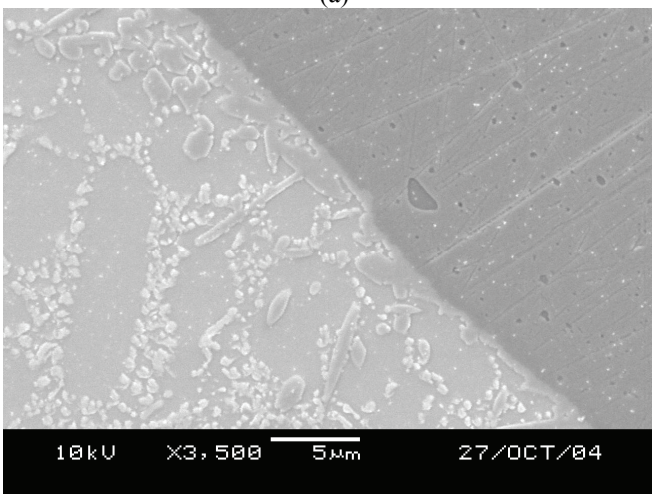
Leadframe Intermetallics



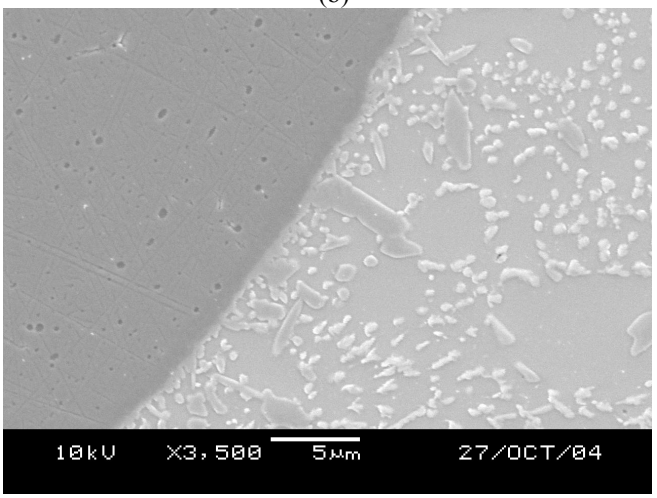
[85:U1] SOIC 28 SnPb finish /minimum T_{peak} (large)
(a)



[85:U3] SOIC 28 NiPdAu finish /minimum T_{peak} (large)
(b)



[85:D20] SOIC 28 NiPdAu2 finish /minimum T_{peak} (large)
(c)



[85:D21] SOIC 28 NiPdAu3 finish /minimum T_{peak} (large)
(d)

Figure 12 - Intermetallic Formation with SAC Solder on Alloy 42 Leadframes with Various Surface Finishes. All Component Leads Shown were Soldered to The Front Side of The PCB.

The 28 I/O Small Outline IC package was procured with Alloy 42 leadframes having a variety of different surface finishes The leadframe finish soldered in Figure 12a was SnPb. Soldering to this finish with SAC387 solder produces an interfacial intermetallic, presumed to be Cu_6Sn_5, which is continuous. Three other NiPdAu leadframe finishes were included in the GPLF study. The resultant SAC soldered interfaces on these NiPdAu are shown in Figures 12b, 12c and 12d. The sequence of leads shown were specified with progressively thinner base Ni layer with the average Pd layer thickness roughly the same for all.

All solder joints pictured in Figure 12 were selected from identical package bodies on the front side of the same PCB, so therefore can be assumed to have experienced nearly identical thermal histories. All intermetallic differences can be attributed to the initial surface finish of the leads. All the NiPdAu finishes are seen produce a much thinner, more erratic intermetallic layer than does a SnPb finish of Figure 12a.

Reliability Stress Test

The IPC-9701 TC1 thermal cycle test, a 0-100°C 40 minute cycle, was selected for the HDPug GPLF reliability evaluation. The actual thermal cycle profile was defined and monitored using (8) thermocouples mounted to the boards, sampling (2) cards per rack on (4) chamber racks along with (4) thermocouples mounted to the 42.5mm ceramic substrates on the center cards to capture the most thermally sluggish locations.

Measured ATC thermal profiles are plotted in Figure 13. Dwell times at the temperature extremes were approximately 10 and 12 minutes at hot and cold extremes, respectively. Slight temperature overshoots are noted at both temperature extremes, with board temperatures reaching -5°C at the lower limit and 105°C on the upper limit. The scheduled test duration was 6000 cycles.

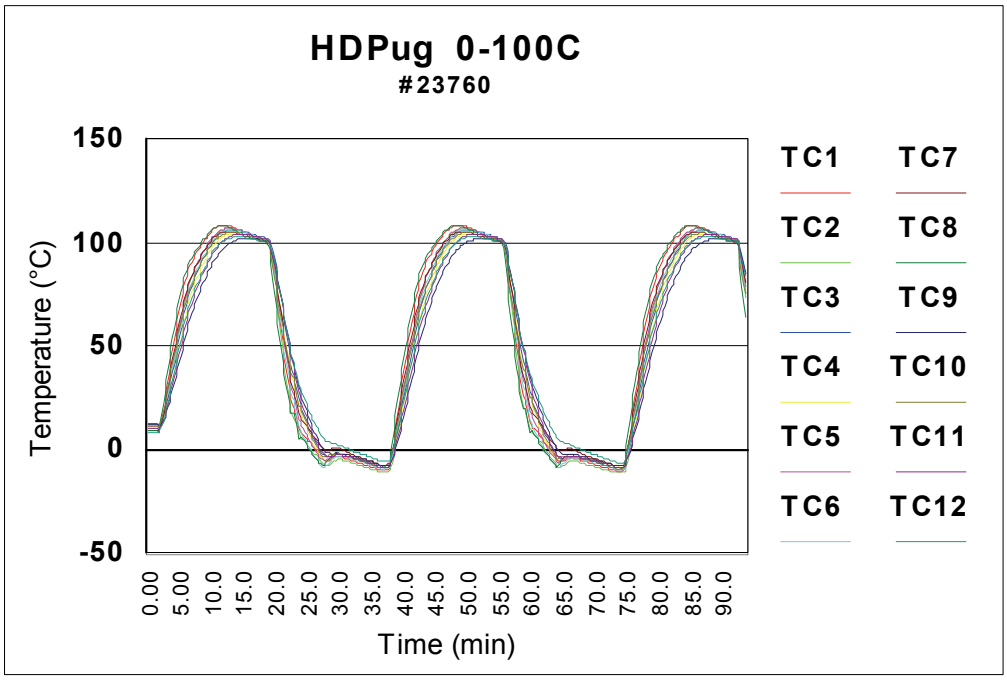


Figure 13 - Measured Thermal Profiles of ATC Cycle at Various Board Locations

In-situ electrical monitoring was employed for eleven of the component types on the GPLF test board. Several are monitored from both front and backside of the board. Monitored components are listed in Table 2. The continuity of electrical nets stitched through the board level interconnects of these components was monitored throughout the thermal cycle using a two wire event detection system. Failure of any given net was defined as (15) events of greater than 1000□ total net resistance.

Component Type	I/O Count (Pitch)	Lead Finish or Ball Composition
PBGA	420 (1.27 mm)	SnAgCu
PBGA	928 (1.0 mm)	SnAgCu
TE PBGA	928 (1.0 mm)	SnAgCu
CBGA	937 (1.0 mm)	SAC387
CuCGA	1657 (1.0 mm)	Cu column
QFP	208 (0.5 mm)	NiPdAu
LQFP	100 (0.5 mm)	NiPdAu3 (□PPF)
LQFP	100 (0.5 mm)	Sn
CSP landgrid	24 (0.5 mm)	CuNiAu
SOIC	28 (1.27 mm)	NiPdAu
SOIC	28 (1.27 mm)	NiPdAu3 (□PPF)

Table 2 - SMT Components Monitored with in-situ Event Detection (2-Point Probe)

Component Type	I/O Count (Pitch)	Lead Finish or Ball Composition
PBGA	304	SnPb
PBGA	420 (1.27 mm)	SnZnAl
QFP	208 (0.5 mm)	NiPdAu
CSP landgrid	24 (0.5 mm)	CuNiAu
SOIC	28 (1.27 mm)	NiPdAu
SOIC	28 (1.27 mm)	NiPdAu2 (□PPF)
LQFP	100 (0.5 mm)	Sn
LQFP	100 (0.5 mm)	SnPb
LQFP	100 (0.5 mm)	NiPdAu
LQFP	100 (0.5 mm)	NiPdAu2 (□PPF)
LQFP	100 (0.5 mm)	NiPdAu3 (□PPF)

Table 3 - Components Monitored with Benchtop Interval Probing (2-Point Probe)

Interval continuity testing of all component package types was included to monitor those additional components for which in-situ monitoring channels were unavailable (Table 3.). Benchtop electrical probing of component nets during interval testing included those components that were also being monitored with event detection.

Cards were detached by unplugging the individual wiring harness connectors at the card, removed from the chamber, and allowed to reach room temperature. The resistance of the test nets was measured with a 2-point probe system. Such interval measurements were targeted for approximately 200 cycles, again at 1000 cycles and then every 1000 cycles thereafter. Shorted 0402 chip passives were also probed during interval testing. Other passives components on the board were not probed. No cards were removed for destructive analysis during the scheduled duration of the test.

Accelerated Thermal Cycle Results
After 6000 cycles of Accelerated Thermal Cycle testing, a majority of the (25) components – surface finish combinations tested, many had no electrical fails when probed at room temperature. Results presented are primarily electrical observations with analytical confirmation of failure mechanism still pending. Highlights from each tested component family are detailed below. Weibull analyses of failures are included were sufficient failures were observed to justify this treatment.

LQFP 100
The 0.5 mm pitch (100 I/O) LQFP interconnects proved very robust in thermal cycle. It was represented in the DoE with five different leadframe surface finishes and assembled with all five SAC reflow profiles (n=281). No fails were detected through 6000 cycles.

QFP 208
Tested with a single NiPdAu leadframe finish, the 0.5 mm pitch 208 I/O QFP proved reliable with all SAC reflow profiles (n=54). No fails were detected through 6000 cycles.

PBGA 304
The 1.0 mm pitch PBGA package was tested with a very limited sample size, predominately with the extended soak SAC profile (n=8). No fails were detected.

TEPBGA 928
TEPBGA, a 1.0 mm pitch PBGA 928 package with an embedded heat slug, was tested predominately with the two elevated temperature SAC reflow profiles (Extended soak; Minimum T_{peak}-large) (n=26). No fails were detected.

PBGA 420
The 35x35mm PBGA (1.27 mm pitch) package with SAC solder balls was tested on the front (n=36) and back (n=13) side of the GPLF test board. All SAC reflow profiles except the lowest temperature profile (Min. T_{peak} – small components) were sampled with the PBGA 420 package. Ignoring four front side components misoriented at initial assembly (also omitted from reported sample size), no other SAC PBGA 420 fails were detected through 6000 cycles.

The PBGA 420 package was also used in the GPLF program for an exploratory evaluation of an alternate Pb-free SnZnAl BGA solder ball alloy. SnZnAl PBGA packages were assembled on the GPLF test board with SAC387 paste along with other SAC based BGA components. The resultant mixed BGA solder alloy proved highly unstable in ATC. Despite a small sample size (n=19), all nets were open by 4000 cycles; with some packages separating completely from the board.

SOIC 28
The 1.27 mm pitch Small Outline IC package was tested with three different Pb-free leadframe finishes, all based on NiPdAu: NiPdAu (n=75), NiPdAu-□PPF (n=46) and NiPdAu-□PPF/upgrade (n=57). All three finishes were tested on both front and back of the board, with the front side sample size about three times that on the back for each of the three cases. A single anomalous fail was observed at 332 cycles; presumed at this point to be due to an assembly defect. No other SOIC 28 fails were detected through 6000 cycles despite the relatively large total sample size for this component type.

PBGA 928
The 40x40 mm PBGA 928 package was tested in relatively small numbers (n=12). This large body component is located on the GPLF board very near the connector used for in-situ monitoring of an ATC test. This connector requires repetitive mating to accommodate the scheduled benchtop interval testing during the ATC test. Four failures were observed in this PBGA population after the 5009 cycle interval readout. All four failures occurred in the same corner of the PBGA; that nearest the center of the cabling connector. Thermal mismatch induced failures would presumably have equal likelihood of failing in all corners of the package. Actuation of this particular cabling connector is such that maximum board flexure will occur exactly at the failing corner of the PBGA component. Pending further analysis, these four corner failures are deemed due to mechanical

overload associated with repetitive connector actuation and do not warrant the statistical treatment of a reliability wearout mechanism. No such connector proximity failures were seen in the SnPb solder control boards (n=2).

CSP 24 Land Grid

The CSP 24 package was attached to both sides to the card, with the front (n=36) having roughly three times the sample size of the backside (n=10). Five fails were detected in the CSP 24 nets starting at 229 cycles and reaching the fifth fail by 5588 cycles. All five electrical fails occurred on front side components with four of the five fails being associated with the Minimum T_{peak} (small components) reflow boards. The measured solder joint peak temperature in that case is only 3°C less than the next hotter profile.

A composite data set of all SAC attached CSP failure data are fit to Weibull statistics in Figure 14. No fails were detected in SnPb attach controls (n=5).

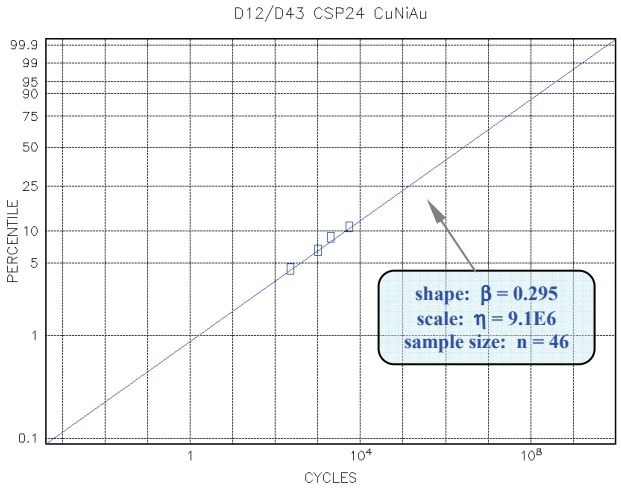


Figure 14 - Weibull Plot of Landgrid CSP 24 ATC Electrical Failures (Include Front and Back Side Populations)

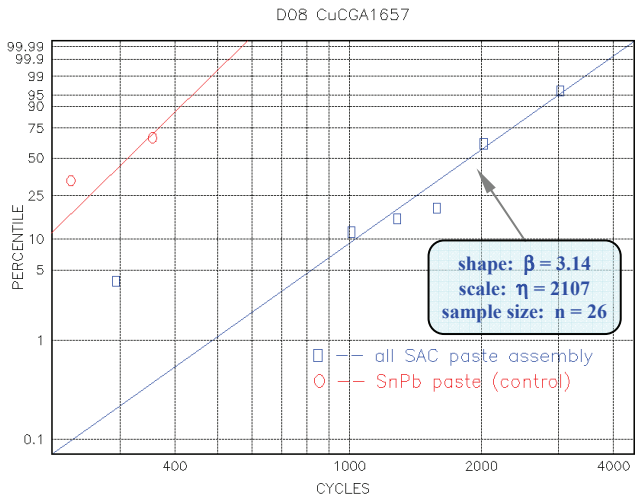


Figure 15 - Weibull Fits of all SAC Attached CuCGA 1657 ATC Rlectrical Failures

CuCGA 1657

The ceramic copper column grid array (CuCGA), a package designed solely for use in Pb-free solder assemblies, fails prematurely when attached with SnPb eutectic solder. All SnPb attach samples (n=3) failed by 680 thermal cycles. When attached with SAC387 solder, the CuCGA survived considerably longer, but still constituted the earliest failing component on the GPLF test board. With the exception of a single module assembled by Fujitsu, all CuCGA modules had failed by cycle 3022. These data plotted in Figure 15.

CBGA 937

The 32.5x32.5mm CBGA module was tested with two different BGA ball compositions: the traditional Pb10Sn ball and the newer, Pb-free, Sn3.8Ag0.7Cu version. These were assembled onto various GPLF boards, either with SAC 387 or eutectic SnPb solder paste, creating four different final solder joint compositions. The control condition is the traditional Pb10Sn ball with eutectic SnPb paste (n=2). Two other cells produce mixed solder BGA joints: Pb10Sn balls with SAC387 paste (n=14) and SAC387 balls with eutectic SnPb paste (n=2). The final cell is fully Pb-free; SAC387 balls attached with SAC387 solder paste (n=12).

ATC test results are plotted in Figures 15 and 16 for the Pb10Sn ball and SAC387 ball components, respectively. Each figure includes data from both solder paste assembly options. An obvious sensitivity of CBGA ATC fatigue life to the SAC reflow profile parameters could not be resolved with the current sample sizes and inherent variability in response data. In Figure 16 therefore, failure data from the various GPLF SAC solder paste reflow profiles are combined into a single composite data set for (forward compatible) mixed assembly (n=14). Similarly, electrical failure data from all SAC reflow profiles are fit as a common Pb-free data set in Figure 17 (n=12). For both BGA ball compositions, the ATC performance with SAC solder paste assembly exceeds that with eutectic SnPb assembly.

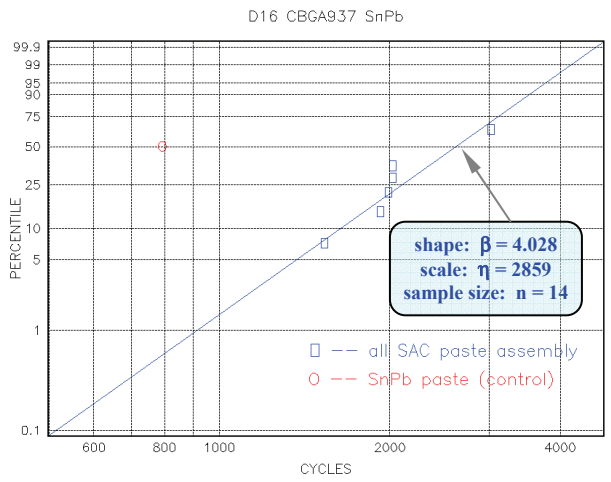


Figure 16 - Weibull Fits of CBGA 937 (Pb10Sn Ball) ATC Electrical Failures

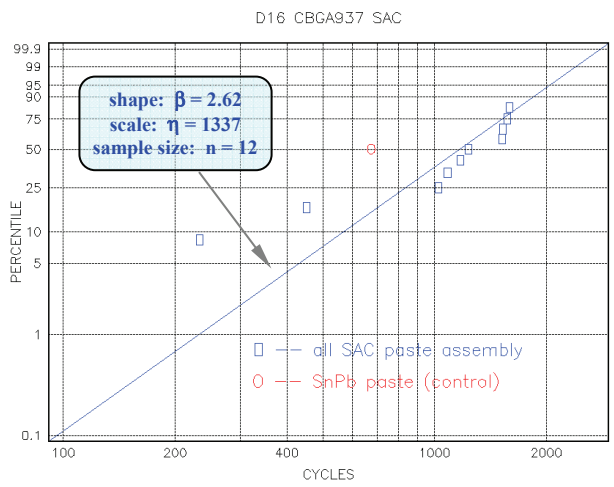


Figure 17 - Weibull Fits of CBGA 937 (SAC387 Ball) ATC Electrical Failures.

Connector Failures

Repeated matings of the GPLF board connector following the benchtop interval probing lead to eventual failure of many connector PTH solder connections in the board. These pin-in-hole solder connections had been made using a conventional SnPb solder fountain attach after the other Pb-free SMT attach processes. Connectors which had not been fully inserted into the board prior to solder fountain attach proved incapable of withstanding the ten or more insertions required for interval testing. A substantial number of these pin-in-hole solder connections failed. This condition produced false fail signals throughout the duration of the test, but ultimately all electrical fails were confirmed with manual probing at test termination.

At this stage, it cannot be ruled out that the same board flexural stresses leading to the failure of these board connector solder joints would also impact the life of other component interconnects near these connectors. While this superimposed handling stress has been identified above as a significant contributor to the PBGA 928 failures, it may contribute to the measured response of other components as well. Excessive handling stress associate with connector manipulation would produce additional scatter in the thermal cycle failure data, or, using the Weibull methodology, greater shape factors.

Ongoing Analyses

The HDPug GPLF project is an ongoing experimental effort. Further metallographic analyses of solder microstructures and failure sites after thermal cycling along with additional Phase II reliability results will be reported as HDPug continues to pursue the definition of a General Purpose Lead Free card assembly process.

Conclusions

Recognizing that the final physical analysis of the HDPug GPLF hardware is still pending, several conclusions are still possible with regard to the performance of SAC solder interconnects in an IPC-9701-TC1 accelerated thermal cycle.

SAC solder joint microstructure can vary significantly across any given PCBA due to the wide variation in process temperature history experienced by individual solder joints. Manufacturing variations in the SMT reflow profile can impart further variability to the solidification microstructure of SAC solder joints. Despite the obvious visual differences in solder microstructures from reflow profile changes though, no significant effect of SAC reflow profile parameters on the as-assembled solder joint mechanical strength was evident for leadframe or leadless solder joints. Mixed assembly with a SnPb leadframe finish does however appear to have a measurable weakening effect on the SAC solder joint.

Adjusting the profiles in a seven zone reflow oven proved ineffective at reducing the component □T across a complex Pb-free circuit board. It was however capable of modifying the maximum reflow temperature and dwell time such that subsequent metallographic analysis of the solder joints produced under these conditions revealed quantifiable differences in microstructure. With the exception of the ceramic BGA components and the land grid CSPs, the characteristic fatigue life of all component SAC solder joints exceeded the scheduled test duration of 6000 cycles and could not be determined.

The only component on the GPLF test board whose reliability demonstrated sensitivity to SAC reflow profile was the 24 I/O landgrid chip scale package. Eighty percent of the CSP fails detected were in components attached with the minimum

temperature reflow profile. The effect of SAC reflow profile on the life of 928 I/O plastic BGAs are uncertain at present due the confounding effects of a repetitive, superimposed mechanical loading from an adjacent connector.

SnZnAl solder alloy BGA connections cannot be recommended as a viable industry Pb-free BGA alloy at this time. Their thermal cycle reliability performance was found to be wholly unacceptable when attached with a SAC387 solder paste.

Acknowledgements
The authors graciously acknowledge the extensive and exemplary metallographic analyses performed by Adam Ryder and Robert Horsley of Celestica.

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