# Optimization of Lead Free SMT Reflow & Rework Process Window

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**Abstract**
Elevated SMT reflow temperatures for Pb-free soldering are placing excessive thermal demands on certain families of electronic components. The High Density Package Users Group, HDPUG, Consortium conducted an extensive study on optimizing the time / temperature profile for reflow to reduce temperature variations from high to low thermal mass components and to identify the minimum peak temperatures that will produce acceptable solder joints. This paper details the preliminary findings of profile characterization work for a range of PCB design types, assessing the impact of adjusting both time and temperatures. Development of thermal profiles for rework of SMT components is also included. Results of metallurgical analysis are given to support provisional recommendations on minimum peak temperature requirements. These were subsequently used for the build of the GPLF (General Purpose Lead Free) test vehicle to assess reliability of Sn/Ag/Cu solder joints produced at the limits of the process window.

**Introduction**
Much of the Pb-free assembly and evaluations done to date have been in support of early adopters whose products are typically characterized as being simpler in complexity from a thermal mass, component mix or reliability perspective. One of the big challenges facing many of the member companies within the HDPUG consortia is that their products are larger, thicker, use a broad variety of component packaging styles and have long field life/reliability requirements. This pushes the limits of current assembly technology from a soldering materials, equipment and components perspective; both for primary attach and rework. This project is part of the broader HDPUG GPLF (General Purpose Lead Free) initiative looking at several of the remaining challenges preventing further industry transition to Pb-free for the manufacture of printed circuit boards in the high complexity/high reliability product space. This paper specifically:

- Presents results assessing the minimum temperature required to produce mechanically sound Sn/Ag/Cu solder joints from a metallurgical perspective.
- Reviews the design features incorporated into the GPLF test vehicle used in the assembly, build, rework and subsequent ATC reliability testing.
- Describes the DOE performed to intentionally create solder joints at the extremes of the Pb-free process window. These assemblies were then thermal cycled to assess whether the temperature affected solder joint reliability and provided a reference library of grain structures under the various assembly conditions and component finish combinations.
- Looks at factors to help reduce peak reflow temperature variation across an assembly

**Determining Practical Limits of Process Window**

The upper limit (i.e. maximum temperature) of process window is generally dictated by J-STD-20. J-STD-20 is the specification used by most component suppliers during the qualification of new packages. In simplified terms, it specifies the minimum temperature which components must be tested to during the qualification phase and by corollary therefore, dictates the maximum temperature the components should encounter during assembly. The specification recognizes the fact that during the typical forced convection reflow process, larger components will generally run cooler than smaller ones also on the board due to their difference in thermal mass, i.e. it takes more energy to heat up a larger component then a smaller. This difference in the rate of thermal energy absorption dictates the temperature gradient or “delta T” seen across the assembly. One of the challenges when assembling larger more complex products is minimizing this delta T to stay within the prescribed allowable process window. At the time when the work detailed in this paper was conducted, J-STD-20B was the applicable revision. As shown in Table 1, peak component temperatures were limited to $245^0$C and $250^0$C for larger and smaller components respectively. As stated earlier, in a typical product with a mix of both small and large components, the small components will always dictate the maximum temperature the process will need to control and manage.

**Table 1 - J-STD-20B Peak Component Temperatures**

| Package Thickness | Volume $mm^3$<350 | Volume $mm^3$>=350 |
|---|---|---|
| <2.5 mm | 250 +0/-5 °C | -- |
| >=2.5 mm | 245 +0/-5 °C | 245 +0/-5 °C |

For this assembly, therefore the maximum allowable temperature was $250^0$C.

It should be noted that J-STD-20C, which has subsequently been released, further refines the package volume differences and also widens the process window by $10^0$C. This aids the assembly task but puts additional strains on the other materials and equipment to be able to deliver and withstand these higher temperatures.

**Table 2 - J-STD-20C Peak Component Temperatures**

| Package Thickness | Volume $mm^3$ <350 | Volume $mm^3$ 350 – 2000 | Volume $mm^3$ >2000 |
|---|---|---|---|
| <1.6 mm | 260 +0 °C | 260 +0 °C | 260 +0 °C |
| 1.6 mm - 2.5 mm | 260 +0 °C | 250 +0 °C | 245 +0 °C |
| 2.5 mm | 250 +0 °C | 245 +0 °C | 245 +0 °C |

At the opposite extreme, the minimum allowable solder joint temperature also needs to be determined. Here it is not so much dictated by a specification as was the maximum temperature, but through a careful balance of soldering material selection, flux performance, wetting characteristics of both the component lead and board finish, and reliability data. This value is generally understood for Sn/Pb soldering because the industry has had many years of field performance to assess whether the current assembly parameters yield reliable interconnects. However, for Pb-free assembly this is not yet the case since few products by comparison are in the field. Some earlier consortia initiatives, with input from materials suppliers, have tried to establish the minimum solder joint temperature required to achieve an acceptable and reliable solder joint for Sn-Ag-Cu (SAC) based Pb-free alloys. The current consensus from this work is that $232^0$C to $235^0$C be the minimum value that should be targeted. One must keep in mind however, that relative to Sn/Pb, very little reliability data exists to backup that datapoint. Part of the HDPUG work was to understand the relative performance of SAC based Pb-free alloys assembled at various minimum peak temperatures, thereby exercising the limits of the process window. Although the ultimate outcome of this work is not to refute the data previously gathered from a minimum solder joint temperature perspective, it will help to define and articulate the available process margin should the assembly temperatures drift below $232^0$C. It will also define the risk of permitting a lower temperature in the event that a board is so complex that the minimum and maximum temperatures cannot be kept within the current process window. Lastly, it might permit a lower maximum temperature to be used, which would be beneficial from the perspective of the overall strain on all parts of the system.

Several experiments were conducted to assess the current soldering equipment and material’s ability to keep the temperatures on the board within the minimum of $232^0$C and maximum of $250^0$C. In fact, for small assemblies, keeping the peak temperature below $240^0$C is generally not a problem. For larger more complex assemblies however, the current limits did present a challenge. The broader component mix from a thermal mass perspective drove a larger temperature delta across the assembly during forced convection reflow soldering. In certain instances, ovens with more zones had to be used or the belt speed reduced by as much as 20-30% thereby extending the overall reflow cycle time in order to stay within the temperature specification. This increase in overall cycle time could present a challenge depending on the product being built, since a decrease in conveyor speeds equates directly to a reduction in line throughput. For very complex products, reflow is generally not the gating operation, so this decrease in throughput would be inconsequential. However, several boards run as part of the experiment were impacted dramatically from this change and thus would push or exceed the limits of current manufacturing/process capability.

All of these experiments were run in a controlled environment where the same ovens, profile cards and measurement equipment were used. In practice however, this might not be the case. Boards will be run across multiple lines, multiple profile cards will be used and different temperature measurement equipment employed; each of which will introduce additional variability into the "perceived" solder joint or component body temperature achieved. This normal production variability must be taken into consideration when establishing the available process window. Oven process tolerance and measurement error can be established through individual experimentation on specific assembly lines and temperature measurement equipment. Based on production experience, typical achievable values are presented in the table below:

**Table 3 - Temperature Tolerances Observed during Reflow Soldering[4]**

| Source of Variability | Typical | Worst Case |
|---|---|---|
| Furnace Repeatability | ±0.4$^0$C | ±0.6$^0$C |
| Furnace To Furnace | ±1.5$^0$C | ±2.3$^0$C |
| Load vs. No Load | ±1.4$^0$C | ±1.8$^0$C |
| Thermocouple | ±1.1$^0$C | ±2.2$^0$C |
| Total | ±4.4$^0$C | ±6.9$^0$C |
| Total (RMS) | ±2.4$^0$C | ±3.7$^0$C |

From the results, the reflow minimum and maximum temperature setpoints should be adjusted by **4$^0$C** to account for the tolerance stack-up. For several of the complex assemblies where it was already difficult to stay within the process window, this variability presents additional challenges. In fact, incorporating the minimum and maximum temperatures and deducting the process variability leaves an available process window of approximately **10-15$^0$C** in which to contain all the components on the board. This provides additional reason to explore the need for understanding the effects of a lower soldering temperature since this would provide for additional process margin and would reflect the temperatures which might "actually" be achieved when running at the limits of the process window if the variability were not accounted for.

**Determining Minimum Reflow Temperature Limits**

A set of preliminary trials was run to assess the practical limits of the minimum reflow temperature that would yield a "reasonable" solder joint from a metallurgical and structural perspective. This minimum temperature would then be targeted for subsequent reliability testing in the broader GPLF build.

A set of boards was assembled at temperatures near and slightly above the melting point of the SAC alloy. As was to be expected, results around the liquidus of 217$^0$C were not successful at yielding solder joints exhibiting either good structure or metallurgical bond as the cross sections below depict.

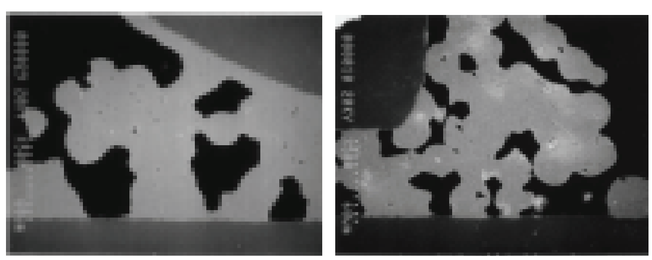


**Figure 1 - Unmelted Solder near 217$^0$C Melting point of SAC Alloy**

In fact, it was not until the temperature approached 222-224$^0$C that a reasonability formed solder joint was created. As such, 224$^0$C was set as the minimum temperature that would be used in the next set of trials using leftover boards and components from phase 1 of the earlier HDPUG Pb-free program[6,7,8]. The board appears in the figure below:

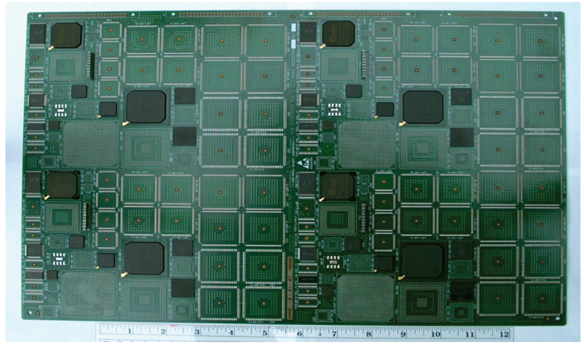


**Figure 2 - HDPUG Phase 1 Pb-free Test Vehicle**

For this trial, solder joints in the range of 224$^0$C to 232$^0$C were created. Enough parts were available to permit 3 specific temperature setpoints to be reasonably evaluated over that temperature range. The chosen temperatures were: 224$^0$C, 228$^0$C and 232$^0$C. Boards were panelized 2 up. Board surface finish was OSP. All boards were assembled using Sn-3.8%Ag-0.7%Cu solder paste. Both images were populated with the available components.

Figure 3 below depicts how the cards were run through the reflow oven and where the thermocouples were mounted. The "leading edge" indicates the side of the card that entered the reflow oven first. From practical experience, it was anticipated that the largest BGA device would be the coolest component since it had the largest thermal mass of the all the components placed. As such, the minimum temperature was targeted for that device. For all BGA components, thermocouples were mounted up through the bottom of the board and connected directly to the BGA balls of the devices, thereby providing the most reasonably accurate determination of achieved solder joint temperature.

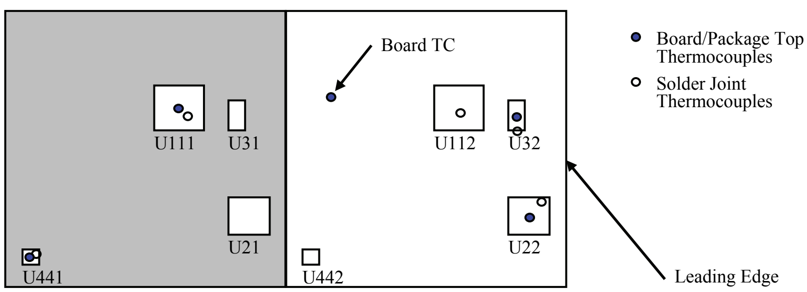



**Figure 3 - Reference Designators and Location of Thermocouples**

The measured solder temperatures for the three target profiles appear in Table 4. As expected, the largest BGA, namely BGA-388P, was the coolest component for all three runs while the bare PWB experienced the highest temperature.

**Table 4 - Actual Recorded Solder Joint Temperatures**

| Package | Location | 224$^0$C Run | 228$^0$C Run | 232$^0$C Run |
|---|---|---|---|---|
| BGA-1.27-256P | U22 | 226.7 | 231.1 | 234.4 |
| TSOP-0.5-48 | U32 | - | 233.3 | 236.7 |
| BGA-388P | U112 | 226.1 | 231.1 | 235 |
| BGA-388P | U111 | 223.3 | 228.9 | 232.2 |
| BGA-48P | U441 | 226.1 | 230.6 | 234.4 |
| PWB | - | 229.4 | 233.9 | 237.2 |

As can be observed in the table, solder joints for component BGA-388P were created in 2$^0$C increments from 223$^0$C to 235$^0$C. By performing cross sections over this temperature range, detailed analysis could be performed to better understand the effects of peak temperature on both the solder joint structure and intermetallic formation. For comparison,
Figure **5** and
Figure **6** show the differences in the external visual appearance of the BGA-388P solder joints between 223$^0$C and 232$^0$C. The rough surface of the high-temperature 232$^0$C reflowed solder joint, is characteristic of the crystallization of Sn dendrites and the

subsequent shrinkage of the pseudo-eutectic liquid [1,3] around the dendrite boundaries. Figure 5c shows a high magnification detail of a portion of a Sn dendrite depicting this behavior. This phenomenon does not appear to take place in any of the lower temperature reflowed BGA's. This difference in morphology was further investigated through some additional experimentation conducted in conjunction with the Department of Materials Science and Engineering at the University of Toronto and was published separately by Snugovsky et al.[1]. To summarize the findings, individual Sn-3.8%Ag-0.7%Cu solder balls were heated to varying peak temperatures and the resulting solidified microstructure analyzed. It was observed that the peak temperature dictated the amount of undercooling the liquid would experience before solidification began. This difference in undercooling dictated which phase was first to solidify out of solution. For higher peak temperatures, the needle-like $Ag_3Sn$ intermetallic crystals are the primary phase to solidify, whereas for the lower peak temperatures, the Sn phase nucleates first.

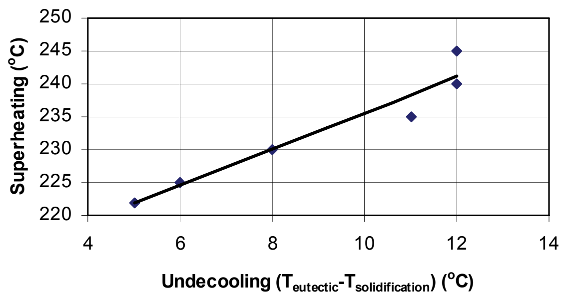



**Figure 4 - Effect of Peak Temperature on Observed Undercooling**

A model for the nucleation and growth kinetics was proposed based on potential solidification pathways to explain the differences in the observed microstructures.

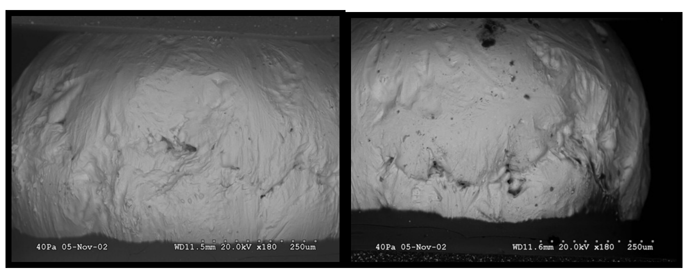


**Figure 5 - Visual Appearance of BGA Solder Joints Created at 223⁰C**

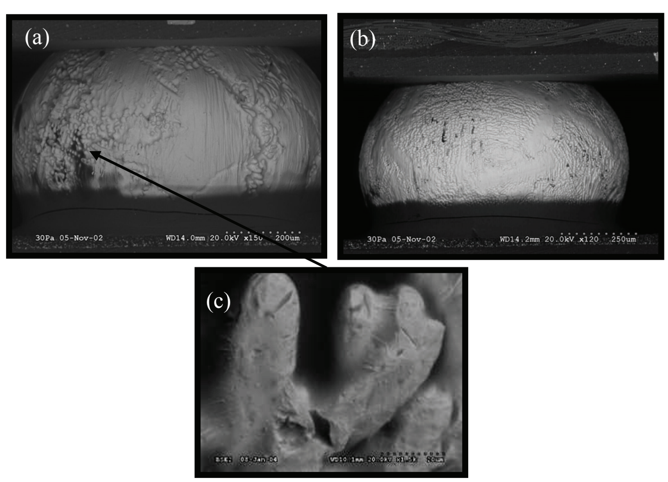



**Figure 6 - Visual Appearance of BGA Solder Joints Created at 232⁰C**

Cross-sectioning and optical microscopy of BGA-388P substantiated the findings of Snugovsky et al.[1] and thus explained the differences in the external appearance of the solder joints. The resulting cross-sections appear in the following series of figures (

Figure **7** to
Figure **11**).


**Figure 7 - Cross-section $223^{0}$C Reflow Temperature**

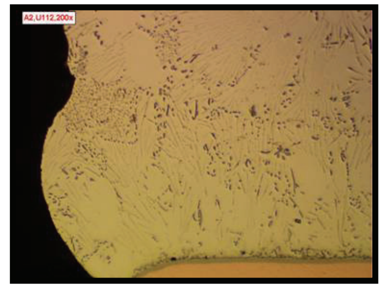



**Figure 8 - Cross-section - $226^{0}$C Reflow Temperature**

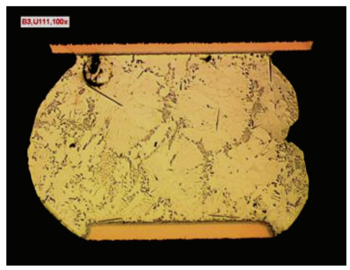



**Figure 9 - Cross-section - $229^{0}$C Reflow Temperature**

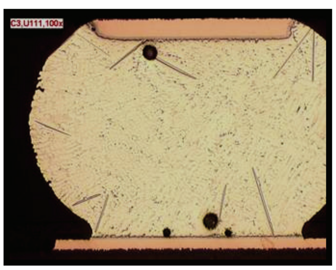



**Figure 10 - Cross-section - $232^{0}$C Reflow Temperature**

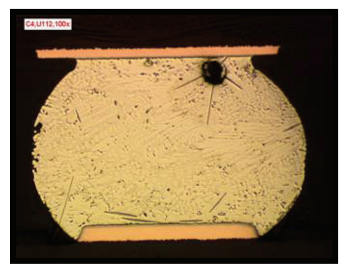



**Figure 11 - Cross-section - $235^{0}$C Reflow Temperature**

Although clearly different in structure, both phases appeared to form good metallurgical bonds as was observed when measurements of the resulting intermetallic at the ball to PWB pad interface were made.

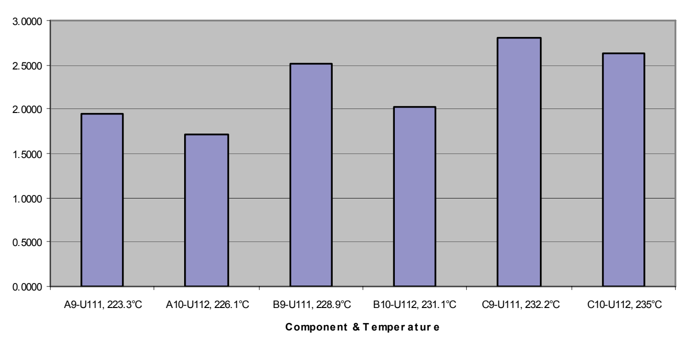



**Figure 12 - Measured Intermetallic Thickness (in µm) vs. Peak Temperature for BGA 388**

As was to be expected, the intermetallic increases on average with increasing peak reflow temperature (typically equates to longer time above liquidus [TAL] for the same conveyor speed); however, the intermetallic formed at even the lower temperatures indicates that a good metallurgical bond has been formed. The same trend held true for the TSOPs and µBGAs on the board as well. The next figure shows the resulting intermetallic formation on both the component and board side at the lower and upper temperatures for the BGA component.

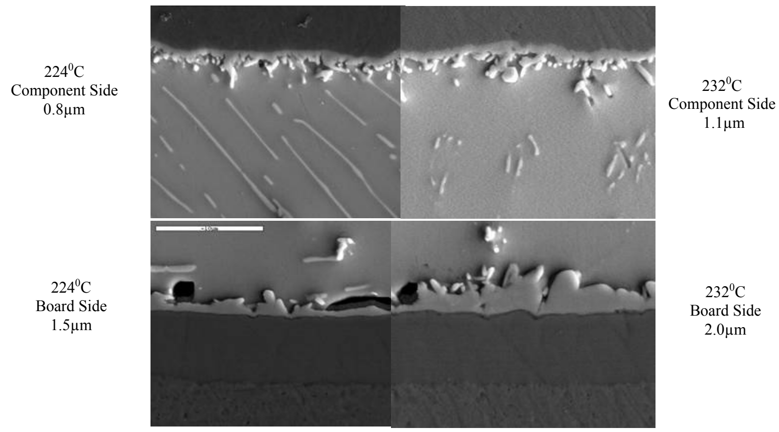



**Figure 13 - Detailed view of BGA Intermetallic Formation as a Function of Peak Temperature**

**Preliminary Reliability and Mechanical Testing**

All metallurgical analysis appeared to suggest that $224^0$C could be used as a good target minimum peak temperature for the GPLF builds to further assess the process window, however before proceeding, a limited set of mechanical and reliability tests were run using the Phase 1 samples to gain more assurance that this temperature could be successfully used. Several tests were performed including:

- Tensile lead pull tests on TSOP devices on the initially assembled ($T_0$) cards
- All remaining cards were put into accelerated thermal cycling (ATC). Since this was meant to be a preliminary assessment only, cards were put into the chamber unmonitored. Analysis was only performed after ATC was complete. ATC specification was: 2400 cycles, 0-$100^0$C, 45 minutes / cycle.
- Tensile lead pull tests on the TSOP devices after ATC
- Dye & Pry on all BGAs and µBGAs after ATC

**Lead Pull Test Results**

Lead pull testing was preformed on the TSOP devices (U31 and U32) to determine the tensile strength of solder joints. Samples were evaluated both before and after ATC to study the effects of thermal aging and processing temperature on the resulting joint tensile strength. Results for the TSOP lead pulls both before and after ATC are presented in
Figure **14**. From the results it can be seen that for the non thermally cycled parts, solder joints created at the lower temperature generally showed higher solder joint tensile strengths than those reflowed at higher temperatures and that ATC reduces the strength most likely due to the increase in intermetallic thickness from the ageing effects of ATC. The strength results link directly back to the intermetallic thickness differences cited previously. It should also be noted that of the TSOP lead pulls prior to ATC, approximately 30% of the fails were lifted pads, indicating that the solder joint between the lead and the pad was stronger than the PWB to pad adhesion. By comparison, after ATC, only a single lead exhibited a lifted pad failure mode, indicating a drop in overall solder joint strength.

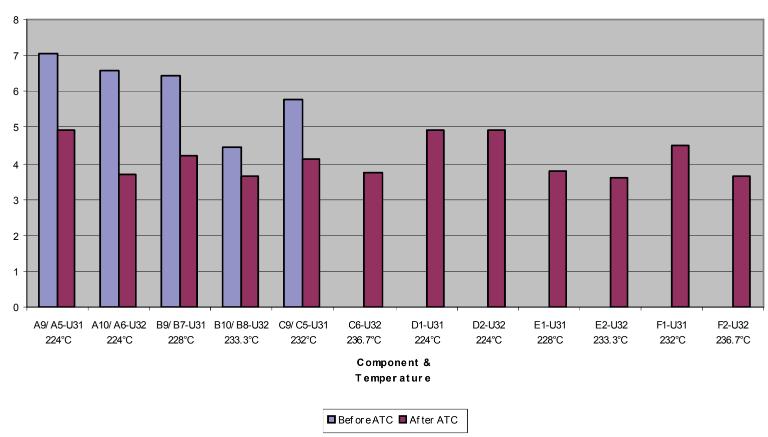


**Figure 14 - Tensile Pull Strength Results for TSOP Devices**

So, from a TSOP tensile strength perspective alone, nothing suggested that 224$^0$C could not be used as a minimum peak reflow temperature. However, it is to be noted that tensile pull tests alone are not sufficient to predict long term reliability of the solder interconnect under various loading conditions (including thermomechanical and mechanical shock).

### Dye & Pry Test Results

Dye & pry was then performed on all the BGAs and µBGAs devices after ATC. The analysis ranked the relative performance of the devices as a function of peak temperature. In this case, a failure was considered as any fracture surface that exhibited any signs of dye being present, indicating that a crack was present prior to the dye being introduced. For each device, the total percentage of solder joints exhibiting any dye was computed for comparison purposes. The dye & pry results appear in the following figures.

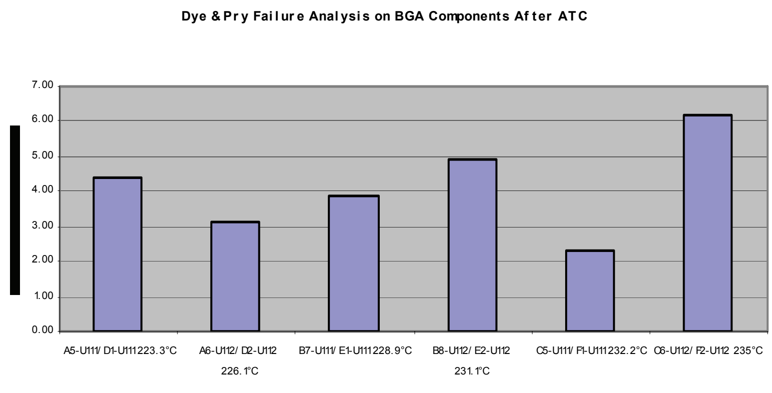



**Figure 15 - BGA Dye & Pry Results after ATC**

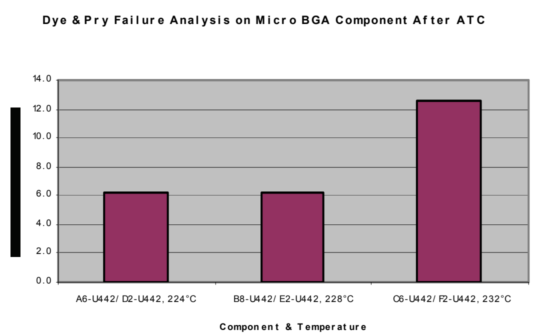



**Figure 16 - µBGA Dye & Pry Results after ATC**

As with all the other results, nothing from the dye and pry results seemed to indicate that the use of 224$^0$C as a minimum temperature would be an issue.

### Other Profile Considerations

Minimum and maximum temperatures were not the only process parameters considered. As was mentioned earlier, the reflow profile for more complex assemblies might dictate that the conveyor speed be reduced by 20-30% to achieve the required delta T. The key variables affecting the delta T are soak time and temperature. The longer the soak, the more time all the solder joints have at getting to a uniform temperature before ramping to above the melting point (see figure below).

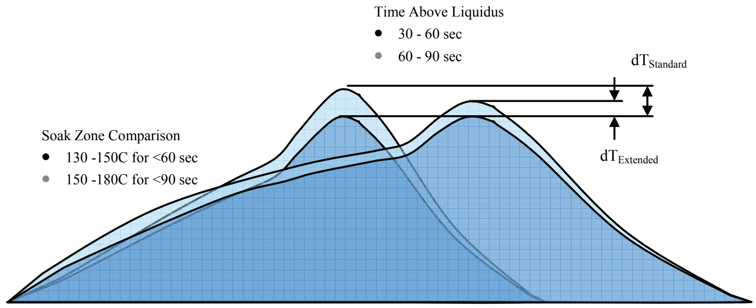



**Figure 17 - Profile Comparisons**

Extending the soak time and increasing the temperature however, will put additional strain on the flux in the soldering paste. Too high a temperature and too long a time will result in depletion of the flux prior to reflow leading to non wetting. Experiments were run to determine the practical limits of soak time and temperature for several Pb-free solder pastes. Since flux depletion is also a function of how much flux is available, initial paste volume deposited was also considered. Solder paste was printed on coupons and reflowed as per the matrix shown in Table 5. Aperture width was varied to control the volume of solder paste printed. The results clearly showed that good results could be achieved even for very long soak times at elevated temperatures for higher solder paste volumes. Once the volume decreased however, wetting performance started to degrade.

**Table 5 - Paste Evaluation Profile Parameters**

| Soak-Time Between 150~180C | Aperture Width | | | |
|---|---|---|---|---|
| | 0.22mm | 0.20mm | 0.18mm | 0.16mm |
| 60sec | G | G | G | G |
| 90sec | G | G | G | A |
| 120sec | G | G | A | U |

G – Good, A – Acceptable, U - Unacceptable

Figure **18** depicts some of the actual paste performance results. The lower right hand quadrant exhibits clear signs of flux depletion to the point where individual solder paste balls have oxidized resulting in non-wetting / non-coalescence of the solder paste.

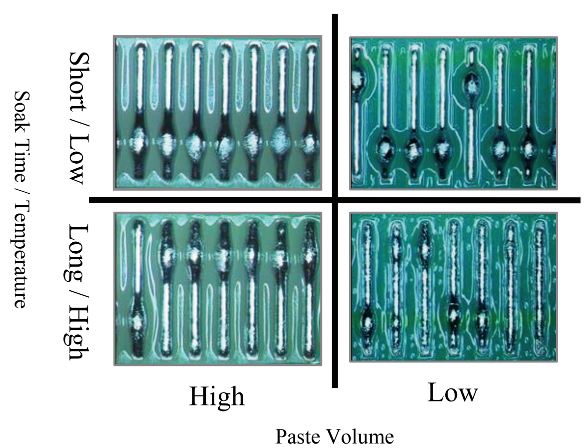



**Figure 18 - Paste Performance**

Although acceptable results were achieved for larger solder paste deposits irrespective of soak duration and temperature, it will be a challenge to build complex products where a diversity of components exist requiring a mix of large and small paste deposits on the same assembly.

Based on these results, a soak time of <90 seconds between 150-180$^0$C was selected for the GPLF builds.

### GPLF Test Vehicle Design

The GPLF Test Vehicle was designed to simulate many of the technical challenges observed during the complex product profiling trials described earlier. It would serve as the primary platform for evaluating the solder joint reliability of Sn/Ag/Cu across the entire process window. In was designed to enable continuous solder joint electrical resistance monitoring during thermal cycling and incorporated many varieties and styles of components as would be typical of a complex product. Components included: CCGA, CBGA, TEPBGA, PBGA, QFP, LQFP, PLCC, SOIC, SMT Power Modules, resistors and capacitors. In total, 40 different components from 11 vendors were evaluated. As a result, a broad set of component termination finishes were also part of the test matrix including: Sn/Pb, Sn, Ni/Pd/Au, Sn/Ag/Cu, Pb90/Sn10, Sn/Bi and Sn/Zn/Al. The mix of component finishes enabled assessment of forwards and backwards compatibility as well as full Pb-free conditions. Prior to performing the actual layout, a series of thermal simulations were run to make certain that the PWB design and layout would properly represent the challenges of a complex product from a thermal mass and temperature gradient perspective. The figure below represents the output from the simulation run used to verify the layout ultimately used for the GPLF test vehicle.

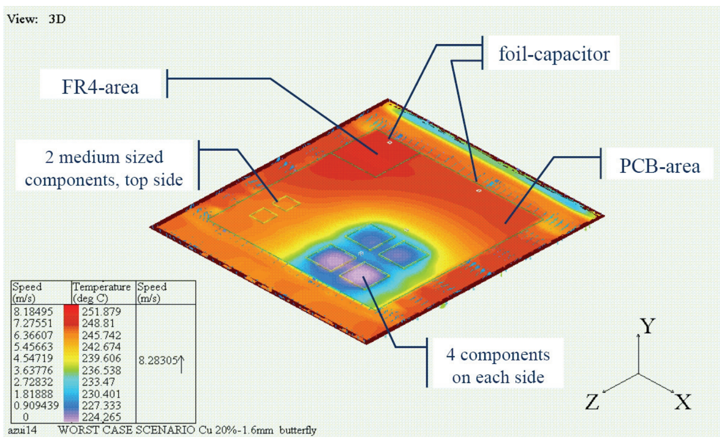



**Figure 19 - GPLF Thermal Simulation**

The board design incorporated the following design elements / features:

- 6 layer, high Tg PCB, 300mm x 240mm x 1.7mm
- IST Coupons
- 72 Daisy chains
- High and low mass regions (to simulate a large delta T) in conjunction with areas in the PWB with high and low thermal conductivity (no inner Cu planes)
- Double sided, including mirror imaged BGAs
- Immersion Sn PWB surface finish

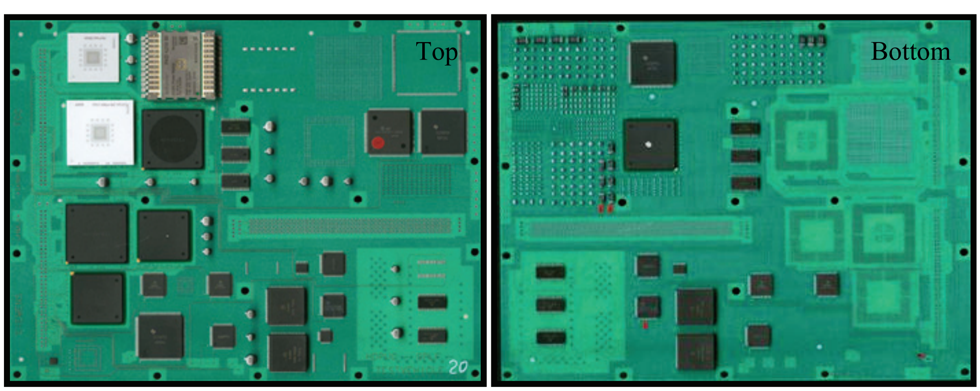


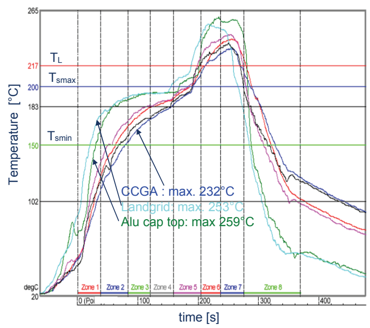

**Figure 20 - GPLF Test Vehicle**

## GPLF Test Vehicle Profiling Evaluations and DOE Matrix

A series of profiling trials were run to determine if the fully populated cards could be assembled using what would be considered "standard" Pb-free conditions:

- Temperature range 232-250$^0$C
- Soak: 150-180$^0$C, < 90 sec
- Time above liquidus: 60-90 sec

As can be observed in the profile below, it was not possible to create a standard Pb-free profile. Several of the above listed parameters were violated; namely soak time and maximum body temperature. The delta T for the board was measured to be **27$^0$C** that far exceeds the available process window of **9-13$^0$C** discussed earlier. This confirmed that the card design exhibited the same performance characteristics seen in the profile trials run on more complex product discussed earlier and would serve as a representative test platform in evaluating various options in establishing a useable soldering profile.




| Parameter | GPLF | J-STD- 20B |
|---|---|---|
| Ramp up rate ($T_L$ - Peak) | 3,2K/s | 3 K/s |
| Preheat (150-200°C) | 114 - 139s | 60-180s |
| Ramp up rate $T_{smax}$ - $T_L$ | < 2K/s | 3 K/s |
| Time maintained above (217°C) | 60-79s | 60-150s |
| Max. temperature | 259°C | 250°C |
| Ramp down rate | 8K/s | 6 K/s |
| Time 25°C to Peak | 311-321s | 480s max. |

**Figure 21 - Trial Profile**

As a result, several profiling and assembly options were evaluated:

- Intentionally lowering the minimum solder joint temperature to 224$^0$C, while keeping the upper component body temperature limited to 250$^0$C, thus widening the process window by approximately 8$^0$C.

- Increasing the soak duration to minimize the delta T across the assembly.

- Populating the assembly without the largest components to simulate a less complex product to see if a "standard" profile could be achieved.

- Again, populating the assembly without the largest components, but this time lowering the minimum solder joint temperature to 224$^0$C. This was to create solder joints for smaller thermal mass components at the lower limit of the process window for reliability comparison to the ones which would be created at the upper end of the process window on those builds which include the large components.

- Evaluating the use of vapor phase soldering as an alternative to forced convection reflow.

- A Sn/Pb control was also included for reliability comparison purposes.

The resulting DOE matrix incorporating all the above mentioned options appears below:

**Table 6 - DOE Matrix**

| Number of Boards | Project | Paste | Pick&Place | Profile |
|---|---|---|---|---|
| 10 | Rework | any | no placing | any |
| 6 | Extended | Omnix | Full | Extended |
| 6 | Extended | Senju | Extra full | HDPUG_B_extended |
| 6 | Extended | Senju | Full | HDPUG_B_extended |
| 5 | Extended | Omnix | Extra full | HDPUG_B_extended |
| 3 | Double sided Reflow | Senju | Full | HDPUG_B_extended |
| 3 | Double sided Reflow | Omnix | Full | HDPUG_B_extended |
| 5 | Power cycling | Senju | Power cycling | HDPUG_B_extended |
| 5 | Power cycling | Omnix | Power cycling | HDPUG_B_extended |
| 11 | Min.peak large components | Senju | Full | HDPUG_B_min_large |
| 12 | Min.peak large components | Omnix | Full | HDPUG_B_min_large |
| 11 | Min.peak small components | Senju | Min.peak small components | HDPUG_B_min_small |
| 12 | Min.peak small components | Omnix | Min.peak small components | HDPUG_B_min_small |
| 4 | SnPb | SnPb | Full | HDPUG_B_SnPb |
| 12 | Standard | Senju | Standard without CCGA,CBGA,PBGA928,PM | HDPUG_B_Standard |
| 11 | Standard | Omnix | Standard without CCGA,CBGA,PBGA928,PM | HDPUG_B_Standard |
| 1 | VP240 | Senju | Extra full | VP-240 |
| 1 | VP240 | Omnix | Extra full | VP-240 |
| 1 | VP240 | Senju | Full | VP-240 |
| 1 | VP240 | Omnix | Full | VP-240 |

Boards were assembled for each of the assembly conditions to better understand the effects of soldering profile on solder joint reliability. Assembly was performed using Sn-3.8%Ag-0.7%Cu solder paste from two suppliers. A 7 zone forced convection oven was used for all legs of the DOE with the exception of the vapor phase trial.

**Profile Discussions and Observations**

The following table summarizes the profiles achieved for selected components on the GPLF board for the various assembly legs of the DOE.

**Table 7 - Component Temperatures**

| Comp. Type | Standard Profile | Min. Peak – Small Components | Min. Peak – Large Components | Extended Soak |
|---|---|---|---|---|
| 1657 CCGA | n/a | n/a | Soak: 93s<br>TAL: 49s<br>Peak: $225^0$C | Soak: 114s<br>TAL: 60s<br>Peak: $232^0$C |
| Al. Cap | Soak: 94s<br>TAL: 72s<br>Peak: $246^0$C | Soak: 93s<br>TAL: 70s<br>Peak: $236^0$C | Soak: 111s<br>TAL: 95s<br>Peak: $252^0$C | Soak: 139s<br>TAL: 79s<br>Peak: $259^0$C |
| 928 CBGA | n/a | n/a | Soak: 100s<br>TAL: 52s<br>Peak: $230^0$C | Soak: 122s<br>TAL: 71s<br>Peak: $237^0$C |
| CSP LGA | Soak: 81s<br>TAL: 70s<br>Peak: $246^0$C | Soak: 104s<br>TAL: 74s<br>Peak: $243^0$C | Soak: 117s<br>TAL: 81s<br>Peak: $246^0$C | Soak: 131s<br>TAL: 69s<br>Peak: $253^0$C |
| 68 PLCC | Soak: 77s<br>TAL: 49s<br>Peak: $231^0$C | Soak: 79s<br>TAL: 36s<br>Peak: $224^0$C | Soak: 110s<br>TAL: 61s<br>Peak: $238^0$C | Soak: 126s<br>TAL: 70s<br>Peak: $244^0$C |
| QFP 100 | Soak: 81s<br>TAL: 65s<br>Peak: $231^0$C | Soak: 90s<br>TAL: 49s<br>Peak: $229^0$C | Soak: 116s<br>TAL: 69s<br>Peak: $248^0$C | Soak: 138s<br>TAL: 75s<br>Peak: $258^0$C |

Soak = Time from 150 to $200^0$C TAL = Time above $217^0$C

**Standard & "Minimum Peak - Small Components" Profile Discussion**

The standard profile repeated the work done on the earlier trials in terms of trying to stay within the "standard" Pb-free profile, however this time without the largest component being placed. As can be seen from the results, a useable Pb-free profile was achieved with minimum and maximum temperatures in the 231-246$^0$C range (delta T of 15$^0$C) . This is in line with many of the Pb-free consumer products already in production today not thermally burdened by large complex components.

The "minimum peak – small components" profile was also developed for the GPLF assembly built without the large components being placed. In this case, the minimum target temperature was reduced to 224$^0$C. In this case, the largest remaining component was the PLCC 68 which achieved the 224$^0$C minimum temperature while the maximum temperature was seen by the CSP (243$^0$C). The key benefit of running this profile was that it would provide data points for the standard leaded solder joints produced at the lower end of the process window compared to the same solder joints created when the large components were present on the assembly. For example, for the PLCC and QFP devices, there were solder joints created on the GPLF assembly across the entire process window from a low of 224$^0$C to a high of 258$^0$C. This will be useful when analyzing the ATC results to determine how the solder joint reliability is affected by the reflow peak temperature.

**Extended Soak Profile**

The extended soak profile was evaluated in an attempt to help minimize the delta T across the fully populated boards. Earlier profiling runs on more complex products did show that extending the soak permitted these types of products to fit within the minimum and maximum temperature window. However, for the GPLF board it was not successful. The theory is that not having a 10 zone oven limited the flexibility in generating an optimum profile that conformed to the J-STD-20B upper temperature specification. However, the profile achieved did fit into the more recent J-STD-20C so it will still provide a useful data point from a reliability perspective.

**Min Peak – Large Components Profile**

This leg of the trials used fully populated assemblies and targeted a minimum solder temperature of 224$^0$C while trying to maintain an upper limit temperature of 250$^0$C as per J-STD-20B. As was expected, the 1657 I/O CCGA was the coolest at 225$^0$C while the hottest was the aluminum capacitor at 252$^0$C resulting in a delta T for the assembly of 27$^0$C. This delta T is not much better than that achieved with the original profile trials as a result of the same heat transfer capacity of the oven used. An oven with more zones would have improved profiling flexibility.

**Vapor Phase Reflow**

The basic principle behind vapor phase soldering is that the vapor phase liquid is boiled and becomes a gas. The assembly to be soldered is submersed into the gas where the gas condenses on the assembly and begins transferring its heat. Condensation and heat transfer continues until all parts of the assembly are at the boiling point temperature of the gas thus guaranteeing that all parts are at the same temperature. It also means that no part of assembly can ever be overheated since it is gated by the boiling temperature of the vapor phase material. As an added benefit, the gas is also inert. Today perfluoropolyether (PFPE) has replaced CFCs as the vapor phase material of choice and is available with boiling points ranging from 155-260$^0$C.

Below is the resulting profile of the fully populated GPLF boards run through the vapor phase machine. At the peak temperature, the delta T across the product was 0$^0$C, a stark contrast to the initial 27$^0$C achieved during the initial profile trials (see
Figure **21**) using forced convection reflow. However, the application of vapor phase reflow may be limited by factors such as higher operating costs and throughput etc..

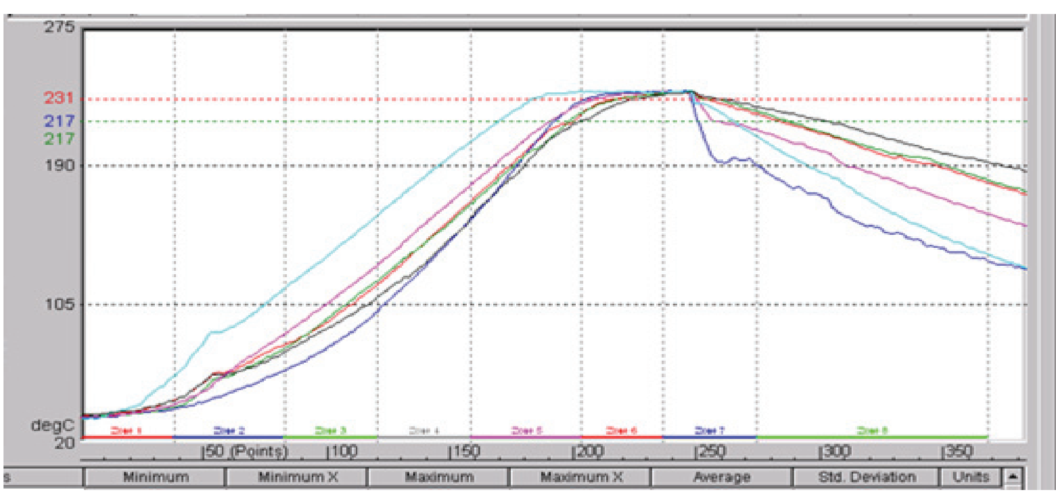



**Figure 22 - Vapor Phase Profile**

**Rework**

Rework was performed on area array packages on the GPLF test vehicle. J-STD-20C states that a Pb-free component **shall** be capable of being reworked at 260 °C within eight hours of removal from dry storage or bake. One of the challenges in creating the rework profile is maintaining the package temperature below the 260°C temperature rating of the component and minimizing the solder joint temperature of adjacent components during rework. Profiles for each of the area array components and the power module were created using a standard semiautomatic rework station. The rework station had a nozzle design that enclosed the component, and convection heaters for the top and bottom side. The bottom side heater is a general board heating unit while the top side heater would be localized to the component (see
Figure **23**).

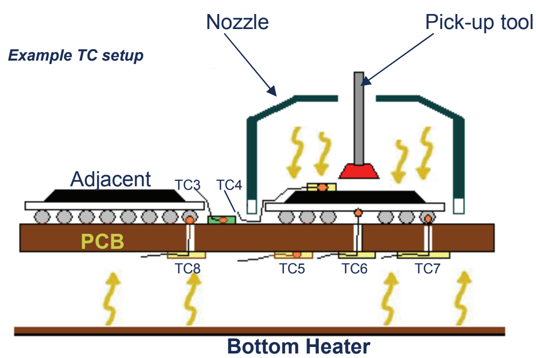



**Figure 23 - Rework Profile Set-up**

For each of the locations, a total of 6 thermocouples were monitored. The thermocouples are located at the following positions:

1) PCB surface
2) Top surface of the package
3) Bottom PCB temperature
4) BGA center temperature (located at solder joint)
5) BGA corner temperature (located at solder joint)
6) Adjacent component temperature (located at solder joint)

Table 8 shows the data captured from the best case profiles created. As can be seen, in most situations the reflow parameters could be met, with the topside package temperature below 260°C and the minimum solder joint temperature above 235°C. It is very difficult to maintain the solder joint temperatures of the adjacent components (at 5mm distance) below the desired temperatures. In real boards, this would be even more challenging as the Cu routing will conduct the heat through the board to the adjacent solder joints. Special techniques are needed to maintain the adjacent temperatures below the melting temperature of the solder alloy.

Figure **24** shows a typical rework profile that was created for one of the PBGA components. The delta T within the packages was 7 $^{o}$C maximum on the largest thermal mass component; use of a special feature on the rework equipment helped keep the topside temperature low.

**Table 8 - Profile Parameters and Measurements**

| Profile Parameters | Target | PBGA420 | PBGA928 | CCGA1657 | CBGA972 | Power Module |
|---|---|---|---|---|---|---|
| Maximum Package Temperature (°C) | <260°C | 259 | 253 | 249 | 252 | 243 |
| Center Solder Joint Temperature (°C) | >235°C | 238 | 237 | 250 | 245 | 242 |
| Corner Solder Joint Temperature (°C) | >235°C | 235 | 236 | 243 | 243 | 243 |
| Adjacent Component Temperature (°C) | <217°C | ***220*** | ***228*** | 203 | 176 | 210 |
| Distance to Adjacent Thermocouple (mm) | | 5 | 5 | 5 | 12 | 5 |
| Soak Time (between 150°C and 217°C) | 60-120s | 84 | 78 | 82 | 71 | 87 |
| Time Above Liquidis (217°C) | 40-90s | 62 | 61 | 87 | 63 | 54 |

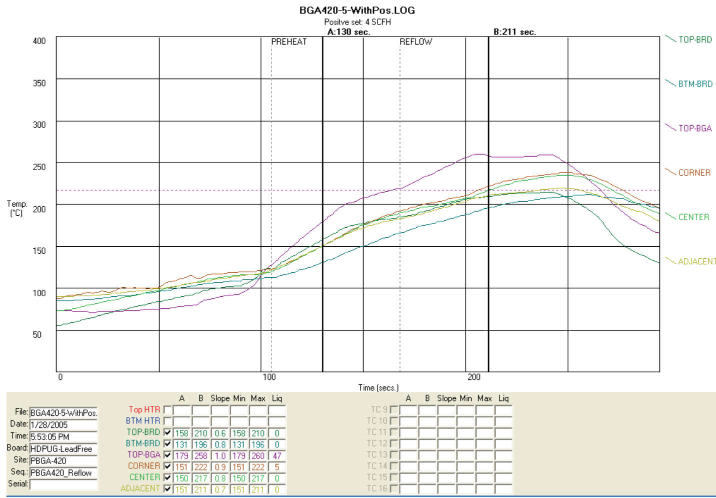
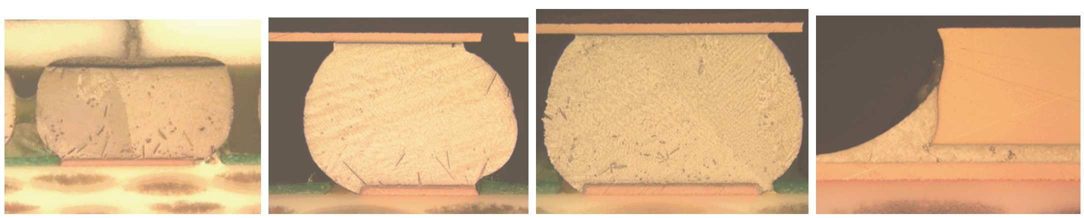



**Figure 24 - Typical Rework Profile**

The rework process was completed and samples were cross sectioned to check for the integrity of the solder joints (see Figure 25). All of the solder balls with the SAC alloy exhibited well-formed solder joints. No indications of adjacent component reflow was observed in the cross sectional analysis. Reliability tests are currently on going.



a) CBGA976 b) PBGA928 c) PBGA420 d) Power Module

**Figure 25 - Cross sections of area array components after rework**

**Conclusions**

During preliminary testing, differences were observed in the microstructure of solder joints created in the range of $224^0$C to $230^0$C versus those above $232^0$C. This variation however did not equate to lower lead pull strength or crack propagation characteristics after limited thermal cycling. As a result, a minimum peak temperature of $224^0$C was targeted for the larger GPLF test vehicle build to allow for direct comparison to the more generally accepted minimum peak temperature of $232^0$C for Sn/Ag/Cu. Numerous assemblies were produced to intentionally create solder joints over the entire range of the Pb-free process window which were then put into ATC testing. The ATC results and $T_0$ metallurgical results for the GPLF test vehicle builds are presented in the companion paper entitled **"Accelerated Reliability Testing and Analysis of Lead-Free Solder Interconnects" Wilcox et.al.**

Although $224^0$C may form adequate intermetallics and have similar strength (from tensile pull tests) to joints produced at $232^0$C and greater, $232^0$C should still be the minimum recommended "target" temperature from a reflow perspective for volume manufacturing, because of the wide variety of components and assemblies encountered and the different loading conditions for the products. The experiments performed at temperatures below $232^0$C highlighted that process margin for unintended inaccuracies or variability resulting from the process, equipment or more challenging products could potentially be tolerated.

The GPLF test vehicle was designed to incorporate design features and components typically found in more complex products. Several profiling trials were performed to minimize the temperature gradient across the assembly. Rework was performed successfully for various area array components, and cross sectional analysis showed satisfactory results.

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**References**

[1] Snugovsky, L., Snugovsky, P., Perovic, D. D., Sack, T., Rutter, J. W., “Some Aspects of Nucleation and Growth in the Pb-free Sn-Ag-Cu Solder”, Materials Science and Technology, 2005, vol 21, No 1, pp. 53-60.

[2] L. Snugovsky, P. Snugovsky, D.D. Perovic and J.W. Rutter, “Effect of Cooling rate on the Microstructure of Ag-Cu-Sn Solder Alloys”, Materials Science and Technology, 2005, vol 21, No 1, pp. 62-68.

[3] L. Snugovsky, D.D. Perovic and J.W. Rutter, “Solidification of Ternary Eutectic and Near Eutectic Alloys in the Ag-Cu-Sn System”, Materials Science and Technology, November 2004, vol.20, pp. 1403-1413.

[4] R.G. Robertson, J. Smetana, “Fundamental Concerns of Pb-free Implementation”, Circuits Assembly, Sept 2000, pg.47

[5] T. Skoczowski, “Simulation von Wärmeprozessen”, International Conference of Mechatronics, Karlsruhe, Sept 2001

[6] Smetana, J., R. Horsley, J. Lau, K. Snowdon, D. Shangguan, J. Gleason, I. Memis, D. Love, W. Dauksher, and B. Sullivan, “Lead-Free Design, Materials, and Process of High Density Packages”, Proceedings of APEX, Anaheim, CA, CD-ROM, March 2003.

[7] Lau, J., W. Dauksher, J. Smetana, R. Horsley, D. Shangguan, T. Castello, I. Menis, D. Love, and B. Sullivan, “Design for Lead-Free Solder Joints reliability of High-Density Packages”, Proceedings of APEX, Anaheim, CA, CD-ROM, March 2003.

[8] Lau, J., N. Hoo, R. Horsley, J. Smetana, D. Shangguan, W. Dauksher, D. Love, I. Menis, and B. Sullivan, “Reliability Test and Data Analysis of High-Density Packages’ Lead-Free Solder Joints”, Proceedings of APEX, Anaheim, CA, CD-ROM, March 2003.