Embedded Passives Go for It!

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Abstract
The trend towards miniaturization has been with us for quite a while, with marketing departments pressuring for ever-smaller dimensions for everything. A question that arises frequently in this context is as follows: Can we accommodate these requirements by offering miniaturization in three dimensions rather than the conventional two in PCB design? A positive answer to this question is now provided through the utilization of embedded passive technology.

In this paper, we present a full flow in comparison between a conventional and 3-D board having the same functionality. The first board is a conventional two dimensional board 780mm x 290mm large, using 1.6mm FR4 in four layers while the second board is three dimensional, 330mm x 366mm large also using 1.6mm FR4 in four layers. The paper includes the details of the decisions taken, the design, layout, simulation, and MRP, as well as considerations of purchasing, materials, assembly, yields, rework, reliability, all summarized in terms of a cost benefit analysis. Additional benefits of this technology are shown to be the possible reduction in size of some of the testing fixtures such as cycling ovens and testbenches.

Introduction
Passive components are known to dominate in all categories. In terms of world market share, passive components has been valued at the order US$700B+* in 2004.

On the circuit boards, they occupy 40%+ of available substrate area, use about 30% of all solder joints and take about 90% of the total assembly cost. A typical design will make use of 15 – 40 passive components on each IC. As a result, passive components, in their present configuration, have an adverse effect on the size, weight, performance and overall cost of PCBs. A much-needed relief is found in the application of embedded passive components methodology for resistors, capacitors inductors and power supplies.

The concept of embedded passives technology (EPT) is to embed passives such as resistors and capacitors into printed circuit boards (PCBs) during the board fabrication process. The embedded passives technology is driven by multiple factors such as the need for better electrical performance, higher packaging density, and potential cost saving. Using this technology, passives may be placed directly below active devices. The shorter distance between the passives and active components reduces the parasitics associated with surface mounted passives, resulting in better signal transmission and less cross talk, lower loss and lower noise, yield in better electrical performance, especially at high frequencies.
Furthermore, passives account for 80 to 95% of the total number of components in a design and consume up to 40 % of the surface area of PCBs. By reducing the number of surface mount passive components, PCB real estate is freed, thereby allowing higher packaging densities to be achieved.
Additionally, Embedded technology has the potential to lower costs by reducing the number of discrete passives used, and by simplifing the assembly process thereby reduce assembly cost .

Principle of Embedded Resistors
With Embedded Resistors technology a concept of sheet resistivity (Figure 1) plays an important role.

The Resistance value Rs for an embedded resistor is defined as:
Resistor value = sheet resistivity x ratio of element length to width

R =Rs x L/W

E.g., a 25 ohm/sq sheet resistivity

Length = 0.030” (30 mils)

Width = 0.015 “ (15mils)

Resistor value = 25 / x (30mils/15mils)

R= 25 / 1 x 2 = 50 ohms/sq

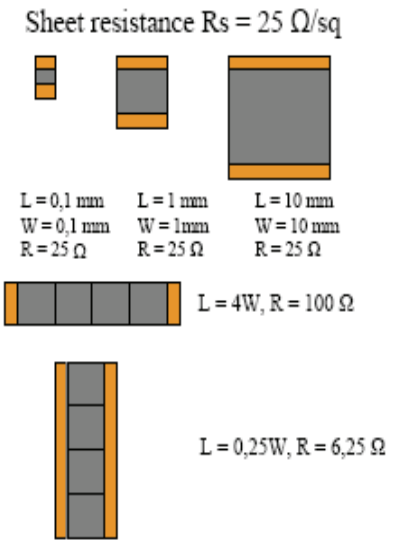


Figure 1 - Resistor Sheet Resistance

As the name indicates, the unit of sheet resistance is ohms per unit area. The sheet resistance comes in different values by different manufacturers. Those are all thin film materials by known manufacturers like Omega Technologies, Gould Electronics and Shipely. It is a very thin layer of resistive material, controled, which is plated on the other side of the copper foil. The limit though is one resistance value per sheet. (Table 1)

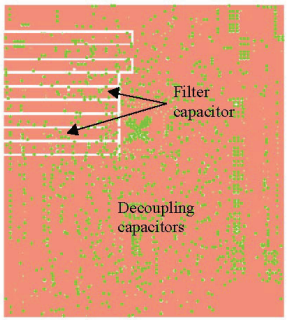
Table 1 - Sheet Resistivity availability in Ohms/square

Sheet Resistivity	Ohmega-Ply® Film Average Thickness	Material Tolerance
10 ?/ ☐	1.00 Micron	3%
25 ?/ ☐	0.40 Micron	5%
50 ?/ ☐	0.20 Micron	5%
100 ?/ ☐	0.10 Micron	5%
250 ?/ ☐	0.05 Micron	10%

Principle of Embedded Capacitors

The principle feature of thin laminated Buried Capacitacne technology are high-frequency by-pass decoupling capacitance, very low by-pass loop inductance, and EMI shielding. These three features of Buried Capacitacne laminates have allowed circuit designers to make significant advances in electronic systems speed and performance.

The ideal electrical characteristics for a power distribution printed circuit board laminate would have capacitive by-pass coupling over a wide frequency range to reject induced IC switching current noise. The laminate should also have a very low and flat impedance response from several hundred Megahertz up to several GHz to minimize power supply voltage noise.



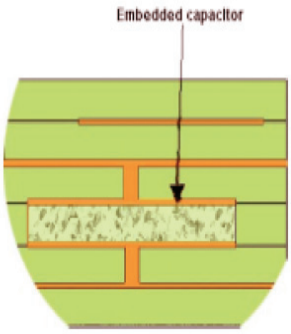


Figure 2 - Embedded Capacitor

The concept of a planar capacitor is to use a thin dielectric having a high capacitance between the power and ground planes. (Figure 2.)

Capacitance and Inductance of a Material will be calculated as

C (in nF) = Dk X A/t

Where Dk is the dielectric constant (or relative permittivity, ε_r)
A is the area in square inches that the power and ground planes have in common
t is the thickness in mils of the dielectric between the planes.

High dielectric constant and thin dielectric give a capacitance density in the range of 2.2 –11 nF/square inch. The total capacitance of a single set of power and ground planes will depend on the total continuous copper area that the planes have in common.

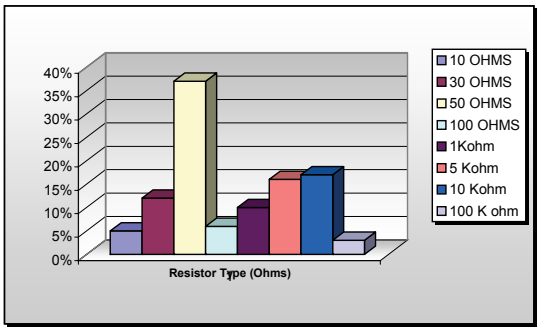
Design Flow

Our application called out for a big board, 780mm x 290mm using 1.6mm FR4 in four layers, with many active and passive components placed on both sides of the PCB, the board needed to be operating in a cycling oven for 24 hours at least. The reason for using over 2000 resistors was due to the nature of the board that is a multi-site burn-in board for IC verification.

When this new embedded resistor application was selected, we needed to determine and analyze several parameters such as: Resistance range availability, thermal cycle parameters, power dissipation, tolerance changes etc.

It was clear that thin film materials do not cover very high resistor values, nevertheless in a digital world with voltages of 1.8V- 3.3V, who needs very high values? Pull-ups pull down and termination resistors can all be in the lower ohm/Kohm range. See comparison table 2.

Table 2 - Common used Resistor values



Heat dissipation ability of a resistor is given as power per unit area, as the thickness of the resistor is constant, it is usually enough to calculate the minimum area for the resistor. All resistor materials can stand high temperature as by definition they are within the PCB structure.

Together with heat dissipation, tolerance of resistor is another key parameter in our design. Most application can operate with 20% to 30 % tolerance; however there might be occasions where tighter tolerances are required. The total resistor tolerance is a combination of the material tolerance and the fabrication tolerances. Trimming and fine-tuning of the resistors value were not considered in this case.

As a result of consulting with several PCB manufacturers who are also implementing Embedded Resistors in their PCB's we decided to go with a 100ohm resistivity sheet. The resistor values in our design ended up being 220ohm, 330 ohm, 1K, and 4.7K.

Once we chose the material resistivity sheet we continued with our electronic design while giving those resistors a different naming convention and value in our CAD schematic system. The resistor prefix changed to BR rather than the traditionally R and it suffix included the material sheet value and power dissipation, like BR_220_0.05w; there exists an IPC naming convention recommendation document regarding embedded resistors. The next step was building the CAD library symbols

for the layout and deciding what shape our resistors will be – Bar, Serpentine, or Round. (Figure 3) It is important to remember that embedded resistors require neither silk nor solder paste patterns.

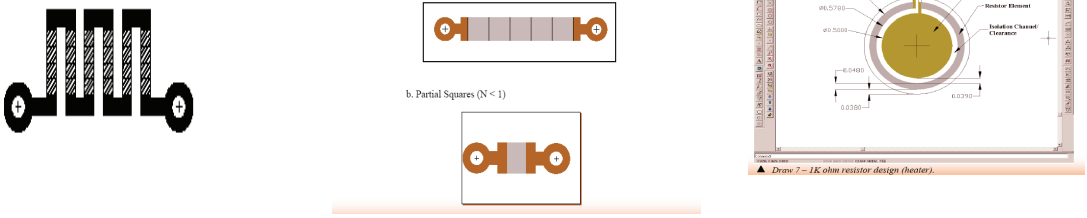


Figure 3 - Resistor types: Serpentine, Bar, Round

We decided on implemetning Bar and Serpentyne resistors in our board and defined as well the internal layers where they are going to be located in. For example in Figure 4 we see an internal power layer, where on one resistor edge we have a direct connection to the plane (no via)and on the other edge of the resistor there is a signal connecting to the to the closest pad/part.

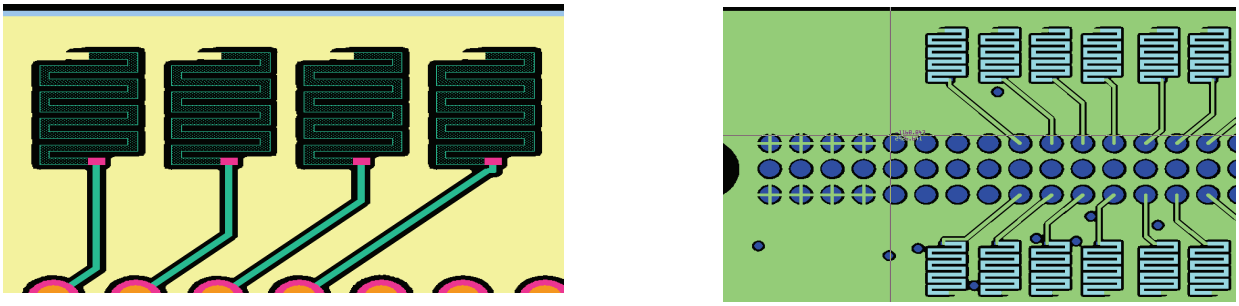


Figure 4 - Embedded resistor in a Plane layer

Once the electronic schemtic was ready we obtained 2 different BOMs. One for the purchase department activity and the second for the PCB manufacturer defining our requirements for the embedded resistors. The layout process continued in its routine path. Most CAD layout systems support today Embedded Passives Technology by offering look up tables to choose materials, resistor shapes and capacitors planes in their latest updated versions. Less can be said on simulation support. We ended up simulating the resistor on its signal line as if it is a regular series or parallel device.

Towards the end of the layout, Gerber files were created, additional resistor layers were defined in our PCB stack-up. By superposition of the resistor layer defined with the plane layer defined, we created a ”full” layer like shown in Figure 4 in the right hand picture, so we were able to check the connection made between the resistor layer and the plane layer, through the connection pad.

A word of caution should be mentioned, in the post processing of the layout the IPC-D356 electrical check for the embedded passives is not completed yet.

We ended up with a board of 330mm x 366mm, 4 layers. (Figure 5) The board was manufactured by the PCB manufacturer we consulted with at first place, the assembly phase was easy, - less 2000 resistors, 4000 solder joints! - the board got tested and integrated into its function. One of the additonal outcomes by the PCB manufacturer were the test results of the embedded resistors values and tolerances.

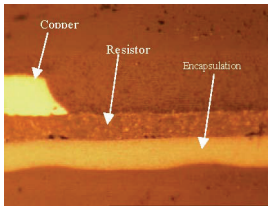
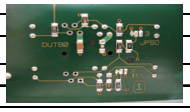
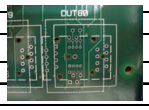


Figure 5 - Embedded resistor in a cross section

The Cost model we chose to in order to "justify" our act was based on 3 elements –
The PCB substrate, the assembly cost, electronic performance. (Table 3)

Table 3 - Comparison table

					Standard Technology		Embedded Technology	
			dimension		30.7″x 11.4″ = 350sq″		12.9″ x 14.4″ = 185sq	
	unit size		layout					
			area		100%		52%	
			substrate		41%		16%	
	unit cost		BOM		17%		22%	
			assembly		42%		10%	
					100%		48%	

End of Story
Embedded passives have been available for a long time. However, due to material limitations (1 nF/in2 and 100 Ohm/sq.), the applications have been limited to a niche market. Significant
progress has been achieved during the past three years. Material manufacturers increased their material's capacitance density from 10 nF/ sq.in to 20 nF/sq.in and their Resistive sheet availability to a much wider range covering from 10 Ohm to 100 K Ohm.

Embedded Passives require similar CAD tools and expertise as regular PCB designs, PCB design tools providers are matching up in their capabilities to support this 3-D trend.
The greatest potential applications for embedded passives technology is in high package density and high frequency products.

Conclusion
Most PCB manufacturers have the capabilities to deal with the process.
Recently, many vendors have been offering new materials for resistor and capacitors sheets for given PCB area. Because change in material is involved and not change in the process, manufacturing shops find it relatively easy to shop between different vendors that offer different materials. For this reason, it is of utmost importance to be aware of the embedded material parameters early in the design phase.

This 3 –D board technique is here to stay. In the short term we can see it applied for embedded passives, however in the long run we will also embed our silicon dies using similar technology.

References

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