An Analytical Analysis of the Discharge of a Buried Sheet Capacitor Using a LCR Analogy

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Abstract
Buried sheet capacitance has been used for sometime in sophisticated PCB designs. The ZBC 2000™ patented by the Sanmina Corporation is a familiar example. Conceptually, this product consists of one or more innerlayers with a two-mil FR4 core. Each such innerlayer forms a sheet capacitor of approximately 500 pico-Farads per square inch. The original purpose of the technology was to replace the surface by-pass capacities with an internal alternative and thereby provide additional outerlayer real estate for routing and active components. Later it was also found that a properly designed buried sheet capacitor is an effective method for containing EMI radiation.

The purpose of this paper is to analytically investigate the dynamic properties of buried capacitors when incorporated into a PCB board. Techniques for improving the performance are also examined.

Introduction
Until now most of the studies focused on the performance of buried capacitance have been empirical relying upon measured responses. This paper will analytically investigate the dynamic properties of a buried sheet capacitor using a LCR lumped system analogy. The discussion considers various interconnect strategies and compares them to the discharge properties of an isolated sheet capacitor. Of special interest is role played by the via interconnecting the sheet capacitor to the board.

The Sheet Capacitor
The typical sheet capacitor is a two mil innerlayer core with copper sheets on each side, see (Figure 1).

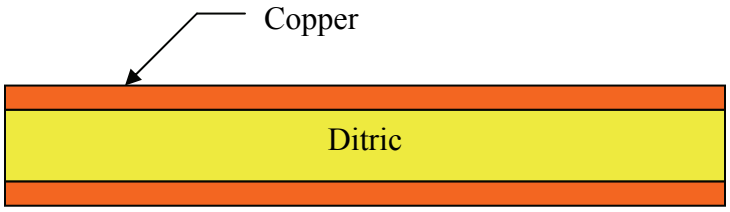


Figure 1
Sheet Capacitor Structure

Inclusion of a sheet capacitor into a MLB structure, unfortunately, complicates the issue. In this case the current flows from the sheet capacitor through a via and to the device as shown in Figure 2.

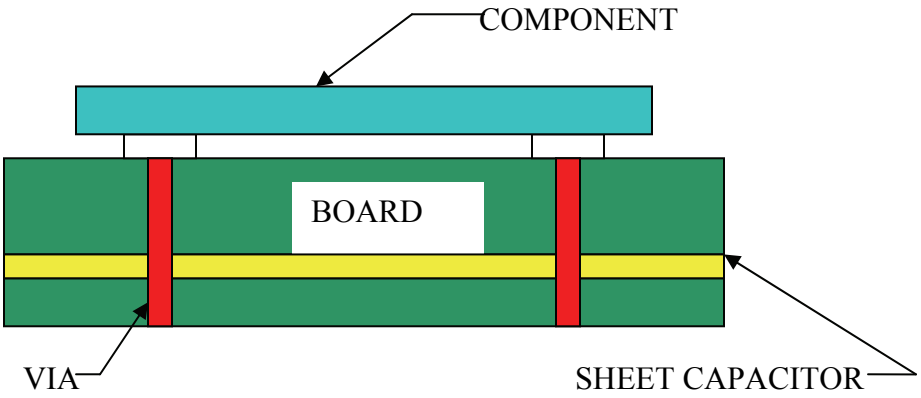


Figure 2
MLB with SHEET CAPACITOR

The result of interconnecting the sheet capacitor by a via to the V_{cc} pin of the device is to increase the time required for the capacitor to fully discharge. The issue is caused by the inductance associated with the via. The analysis presented below analytically quantifies the issue. The lumped system for a sheet capacitor in series with a via is shown in Figure 4.

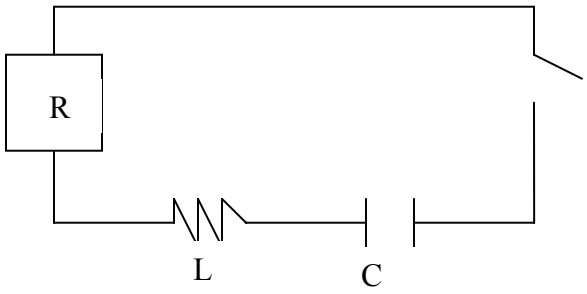


Figure 4

After the switch is closed, the capacitor discharges according to the governing equation:

$$L\frac{d^2Q}{dt^2} + R\frac{dQ}{dt} + \frac{Q}{C} = 0 \qquad (1)$$

for purposes of this analysis it will be assumed that the inductance, resistance and capacitance are constant.

The closed form solution to this differential equation is:

$$Q = Ge^{-pt}\cos(\text{qt-H}) \qquad (2)$$

Where

$p = \frac{R}{2L}$ maybe considered the reciprocal of the time constant and

$q = \frac{R}{2L}\sqrt{\frac{4L}{R^2C} - 1}$ maybe considered the frequency of the current.

H and G are constants of integration.

The boundary conditions are:

When t=0 $Q=CV_e$ and $\frac{dQ}{dt} = 0$

Where V_e is the voltage associated with the sheet capacitor.

It follows:

$H =$ $\tan^{-1}(p/q)$

$G = \frac{CV_e}{\cos H}$

The analysis below will focus upon the behavior of the amplitude envelope in Equation 2. That is: e^{-pt} which governs the flow of the charge Q stemming from the sheet capacitor. It will be noticed that the time constant ($\tau=1/p$) is a function of the inductance and resistance only and independent of the capacitance of the sheet capacitor. Consequently, the discharge rate of the sheet capacitor will be a very weak function of the sheet capacitor material since the resistance and inductance of the sheet capacitor will be shown to be small compared to the same properties of the via.

Typical Values for the Interconnection Structure

For the Via

The resistance of the via with one mil thick copper is 679 micro ohms per square and it follows for a 13 mil via in a 62 mil board the resistance is

$R_v = 1.4 \times 10^{-3}$ ohms

The inductance of a via can be approximated as:

$L_v = 5.08\ h \left[\ln\left(\frac{4h}{d}\right) + 1\right]$ nH (see Ref 2)

Where h is the length of the via and d the diameter in inches. For the case at hand

$L_v = 1.2$ nH

Notice that the inductance is primarily a function of the length of the via and a weak function of the diameter.

The capacitance of the via is:

$C_v = 1.41\varepsilon hd / t_c$ pF (see Ref 2)

Where ε is the dielectric constant

t_c is the thickness of the via copper in inches

$C_v = 4.5$ pF

Which is minor compared to the sheet capacitor.

For the Sheet capacitor

The capacitance of the sheet capacitor is assigned to be 500 pF.

The inductance of the sheet capacitor is

$L_{sc} = 12.56 \times 10^2 (h/w^2)$ nH/m^2 (Ref 3)

Where h is the distance from copper center to copper center (meters)
w is the effective width of the ground plane (meters). The inductance of the sheet capacitor is then

$L_{sc} = 0.107$ nH

Which is small compared to the inductance of the via.

The resistance of the sheet capacitor is 679 micro ohms per square per mil of copper.

$R_{sc} = 0.485 \times 10^{-3}$ ohms.

The lumped resistance, capacitance and inductance for the interconnected sheet capacitor are then

R = 1.88 x 10^{-3} ohms
L = 1.3 n Henrys
C = 500 pF

Analysis
First we will develop the numerical values for the constants in Equation 2.

p = 0.75 x 10^6 / sec
or $\tau = \frac{1}{p}$ is approximately one microsecond.

q = 1.5 x 10^9 radians/ sec or 250 mega Hertz

H = 10^{-3} which is small and the cos H is approximately 1.0. Consequently,

$G = CV_e$

And

$Q = CV_e \exp(-.75 \times 10^6 t) \cos(1.5 \times 10^9 t)$ (3)

Define $Q_0 = CV_e$, the initial charge. Then

$$\frac{Q}{Q_0} = \exp(-.75 \times 10^6 t) \cos(1.5 \times 10^9 t) \quad (4)$$

Our focus will be on the exponential envelop, *i.e.*

$$\frac{Q}{Q_0} = \exp(-.75 \times 10^6 t) \quad (5)$$

The decay in the charge is shown below

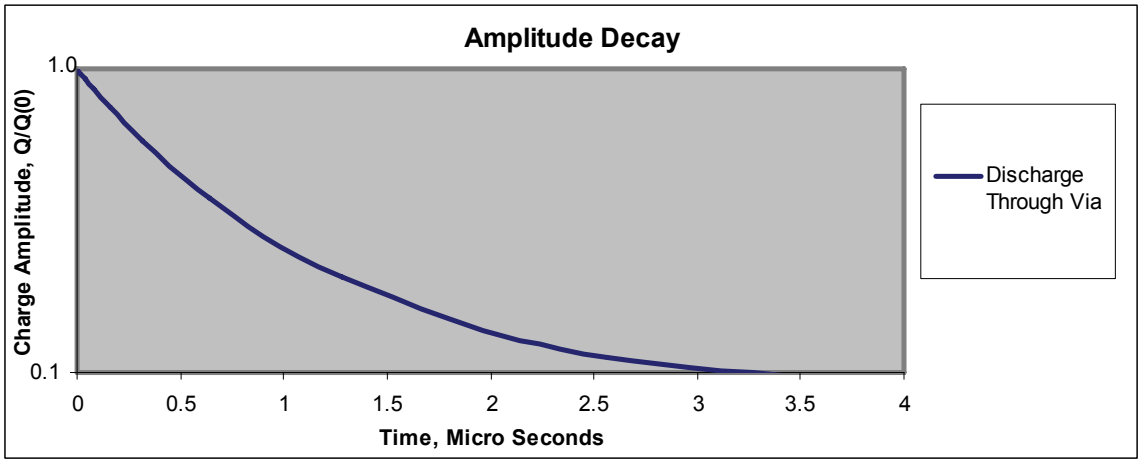


Figure 5

As seen, ninety percent of the original charge has been released after approximately three micro seconds.

Most of the delay is caused by the via. In theory, the absolute minimum time required to discharge the sheet capacitor would be through a via with no impedance. Using this metric, one can then judge the penalty associated with the interconnection system.

The form of the governing equation in this case is still Equation 5. The time constant for the sheet capacitor alone is

$$\tau_{sc} = 1/p = \frac{2L_{sc}}{R_{sc}} = 100 \text{ nano seconds}$$

The dynamics of the discharging sheet capacitor can be examined by focusing upon the exponential envelopes which are shown below.

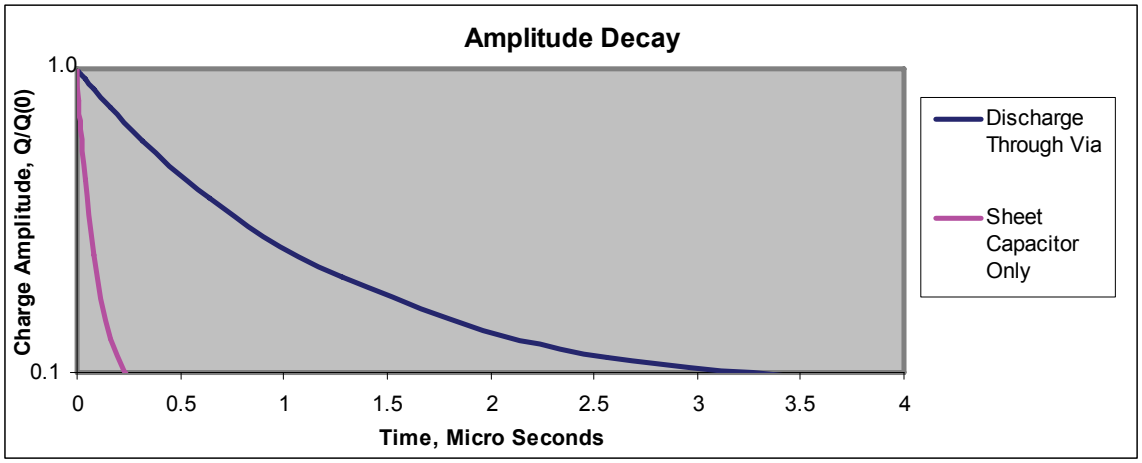


Figure 6

As already noted, about three microseconds are required to discharge the capacitor through a via. On the other hand, with a zero impedance via, the time would be about a quarter of a micro second. Obviously, because of the associated inductance, the via greatly reduces the discharge rate.

We have now bracketed the performance range of the sheet capacitor. Our interest now concerns the influence of other interconnect strategies on this phenomena.

Some improvement can be obtained by using blind microvias. For this analysis assume the via to be four mils long and five mils in diameter. Using the equation above for vias the inductance is

L_{via} = 0.05 nH (as compared to over 1.0 nH for a conventional via)

The resistance is

$R_{via} = 0.34 \times 10^{-3}$ Ohms

The time parameter p in Equation 7 is then

L = 0.16 nH

$R = 0.82 \times 10^{-3}$ Ohms

And

$p = 2.6 \times 10^{6}$ per sec or τ = 380 nano sec

which is about half of the conventional via. The discharge rates are compared in figure 7.

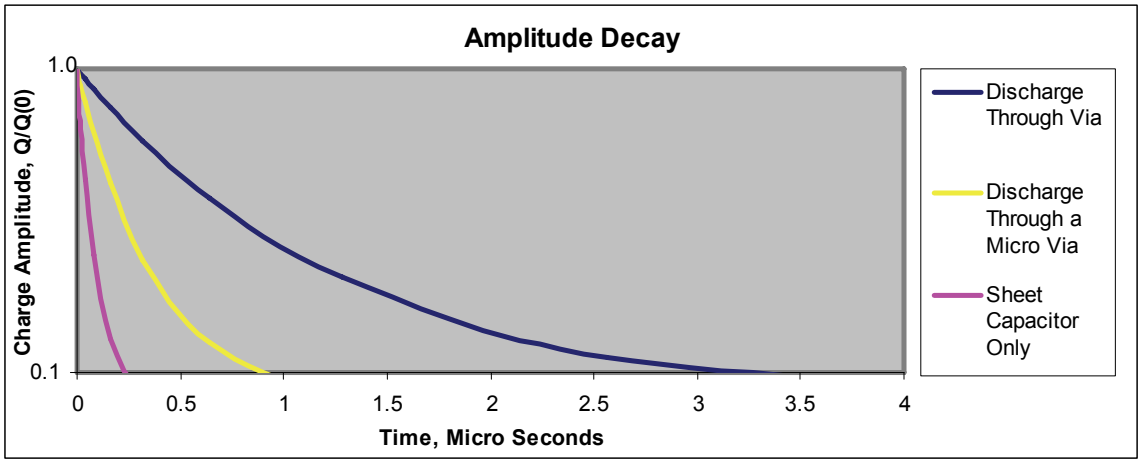
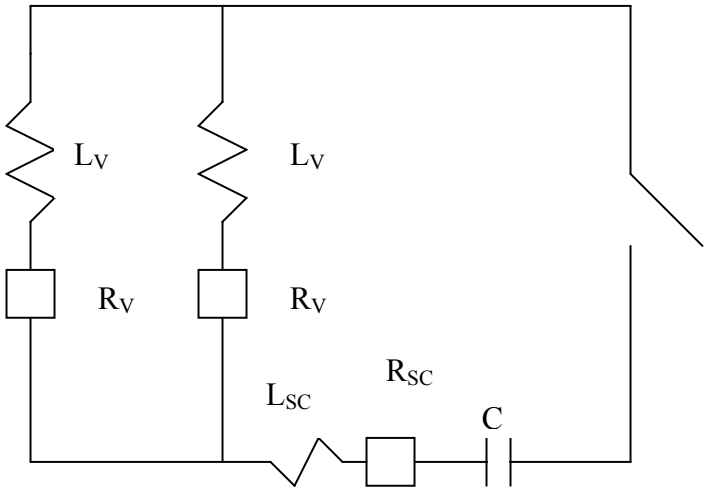


Figure 7

While the discharge time for the micro via is more than the sheet capacity, it is a factor of three less than the conventional via.

It should also be pointed out that by using a blind micro via which as observed reduces the inductance; the noise generated when charge is drawn from the sheet capacitor will in turn be reduced since the noise is proportional to $L\frac{di}{dt}$.

Next, we will consider the case of discharging through two closely spaced identical conventional vias. The lumped system is



shown below:

Figure 8

The governing equation in this case is:

$$L_v \frac{d^2Q}{dt^2} + (R_v + 2R_{sc})\frac{dQ}{dt} + \frac{2Q}{C} = 0 \qquad (10)$$

Using the values already stated above for L_v, R_v and R_{sc}

$$p = \frac{(R_v + 2R_{sc})}{2(L_v + L_{sc})} = 0.92 \text{ x } 10^6 \text{ per second or } \tau = 1.1 \text{ microseconds}$$

The amplitude decay is shown below and compared to the other scenarios discussed above

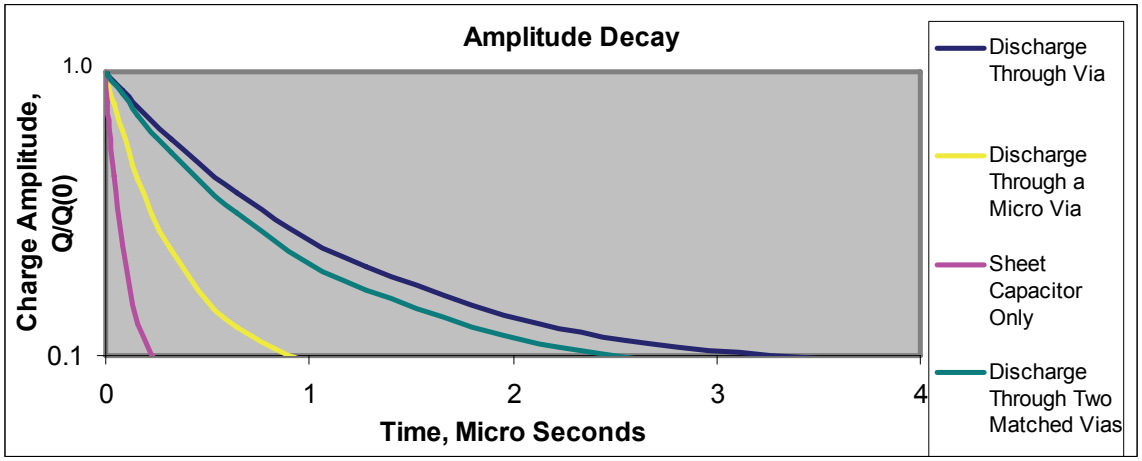


Figure 8

As seen, using multiple vias improves reduces the decay time as compared to a single via, but not to the extent of a micro via.

Summary

The analysis has investigated the discharge of a sheet capacitor when interconnect to a PCB through a via. The analysis found that to first order the decay rate is independent of the initial charge imposed upon the sheet capacitor. It was also shown that the discharge time of the sheet capacitor could be reduced by such techniques as blind micro vias and multiple vias interconnecting the sheet capacitor.

References

1. HADDCO Buried Capacitance Manual
2. Johnson and Graham, High Speed Digital Circuits, Prentice Hall, 1993
3. University of Missouri-Rolla, Electromagnetic Compatibility Laboratory