Substrate with Combined Embedded Capacitance and Resistance for Better Electrical Performance and Higher Integration

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Abstract

Many articles have been published on the benefit of thin substrates for use as embedded capacitor layers as well as thin film resistive material for embedded resistors. Until now the utilization of both technologies within a printed circuit design required the use of separate cores within the PCB. This adds additional thickness to the PCB as well as cost. A new substrate has been developed to address these issues.

Embedded technologies improve the electrical performance of high speed digital circuits as well as enabling the removal of SMT discrete components (the ratio of passives to active components is increasing while the available board surface area is decreasing). By combining capacitance and resistance on the same core, with the resistor foil being supplied on one or both sides of the capacitor dielectric, these benefits can be realized without increasing the overall number of layers or the substrate thickness. Also, some unique R-C circuit designs can be formed by utilizing this substrate.

We will discuss the process and design guidelines for using this substrate as well as some possible applications. Also, results from high frequency testing of PCB test vehicles will be discussed. Future product developments will also be shared.

It will be demonstrated that this new substrate has excellent electrical properties while being able to be readily manufactured using typical inner-layer processing.

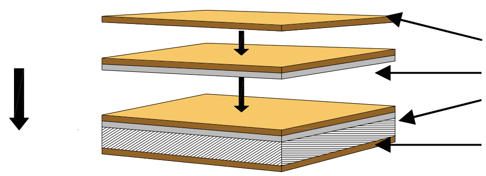
Introduction

The development of Embedded Passive Component technology has been driven by the need to save board area and/or reduce board size, increase functionality, lower costs, improve electrical performance and reliability. Numerous papers describe the current standard 50µm (2mil) dielectric thickness material, mostly utilized for telecom and networking applications[1)] and its electrical performance[2)]. In addition new materials with thinner dielectrics and higher Dk have now begun to be commercialized[3)], further expanding the use of this technology. Embedded resistors have also been utilized for over 30 years in both commercial and military applications. This technology has proven to be reliable and has allowed for designs that could not be achieved otherwise. With both types of technologies available, some designs already incorporate both into the same PCB. The capacitor materials are utilized for the power/ground planes and the resistor materials are incorporated into the signal layers or voltage planes not part of the capacitive cores. This results in multiple special cores being utilized.

A new material has been developed that incorporates both the capacitive material as well as a resistive layer on the same substrate. This substrate can reduce the number of layers required as well as provide opportunities for unique designs.

Embedded Resistor/Capacitor Material Properties

The resistor/capacitor material ("R/C") is constructed of two sheets of copper foil with a thin dielectric between them. On one sheet of the copper foil, a thin film of nickel phosphorous was previously plated. The thin layer provides the resistive properties. This layer is laminated against the dielectric. The dielectric is a blend of epoxy thermoset resin and various thermoplastic resins. The blend provides for compatibility with traditional PCB processing, as well as make the material flexible and strong and have a high dielectric breakdown voltage. Figure 1 shows the construction of the material.



Testing of the R/C material was first performed by doing the standard tests for each material. The capacitor testing showed that the requirements for standard capacitor material were met and is similar to material made without the resistor layer. This is shown in table 1A.

Table 1A - Capacitive Properties of R/C Material

Properties	Ohmega/FaradFlex Core	Remarks and Conditions
Copper Weight, µm	35	Nominal
Sheet Resistivity, ohms / square	25	Nominal
Dielectric Thickness, µm	24	Nominal
Cp@ 1MHz, nF/in2(pF/cm2)	1.0 (155)	IPC-TM 650 2.5.5.3
Dk @1MHz	4.4	IPC-TM 650 2.5.5.3
Loss Tangent @ 1MHz	0.015	IPC-TM 650 2.5.5.3
Peel Strength, lbs/in	5.0	IPC-TM 650 2.4.9
Dielectric Strength, kV/mil	5.3	IPC-TM 650 2.5.6.3
Tensile Strength, Mpa(kpsi)	152(22.0)	ASTM D-882 A
Elongation, %	18.5	ASTM D-882 A

Figure 1 R/C Material Construction

Next the resistive properties were measured. Again the resistive properties were as good as or better than resistive material on standard FR4 epoxy. In particular the thermal properties of the material, on the capacitor substrate, were much better. This includes less change in resistive values after thermal cycling and solder shock. This is important as the resistor values will be less likely to change during assembly and in use. Another important difference is that the power density is 3 times higher. This is probably due to the fact that the thin laminate can transfer heat to the copper on the opposite side so it can be dissipated. Higher power density is valuable as this can allow smaller resistors to be utilized and will be discussed further. The resistive properties of the R/C material are shown in Table 1B and compared against FR4.

Table 1B - Resistive Properties of R/C Material

Properties	Ohmega/FaradFlex Core	Ohmega Core FR-4 (control)	Remarks and Conditions
Sheet Resistivities (ohm/square)	25	25	Nominal
Material Tolerance	+/-5%	+/-5 %	
Load Life Cycling Test Resistor Size: 0.500" X 0.050" Loaded: (Δ R%) @ 150mW Unloaded: (Δ R%)	<0.9 after 3200 hrs.) <0.74 after 3200 hrs.)	<5	MIL-STD-202-108I Ambient Temp: 70C On Cycle: 1.5 hrs Off Cycle: 1.5 hrs Length Of Test: 10000 hrs
Current Noise Index in dB	<-23	<-15	MIL-STD-202-308 Voltage Applied: 5.6 Volts
Humidity Test (Δ R%)	0.5	0.5	MIL-STD-202-103A Temp: 40 °C Relative Humidity: 95% Time: 240 hrs
Characteristic (RTC) PPM/°C	-6.0	50	MIL-STD-202-304 Hot Cycle: 25°, 50°,75° 125°C Cold Cycle: 25°, 0°,-25°, -55°C
Thermal Shock (Δ R%)	0.2	-0.5	MIL-STD-202-107B No of Cycles: 25 Hot Cycle Temp: 125 °C Cold Cycle Temp: -65 °C
Solder Float (Δ R%) After 1 Cycle After 5 cycles	-0.4 -0.6	0.5	MIL-STD-202-210D Temp: 260°C Immersion: 20 Second
Power Density (mW/mil ^{2}) derated at 50%	0.45	0.15	Step-up Power Test Resistor size 0.020" x 0.030"

Processing of R/C Material

Figure 2 shows the process flow for forming the resistors and capacitors on the R/C material. The capacitive electrodes are formed by removing the unwanted copper and resistive material during the first and second etching steps. In order to form the resistors it is necessary to perform a 3rd etching step that selectively removes the copper but leaves the resistor material (this is usually an alkaline etching solution).

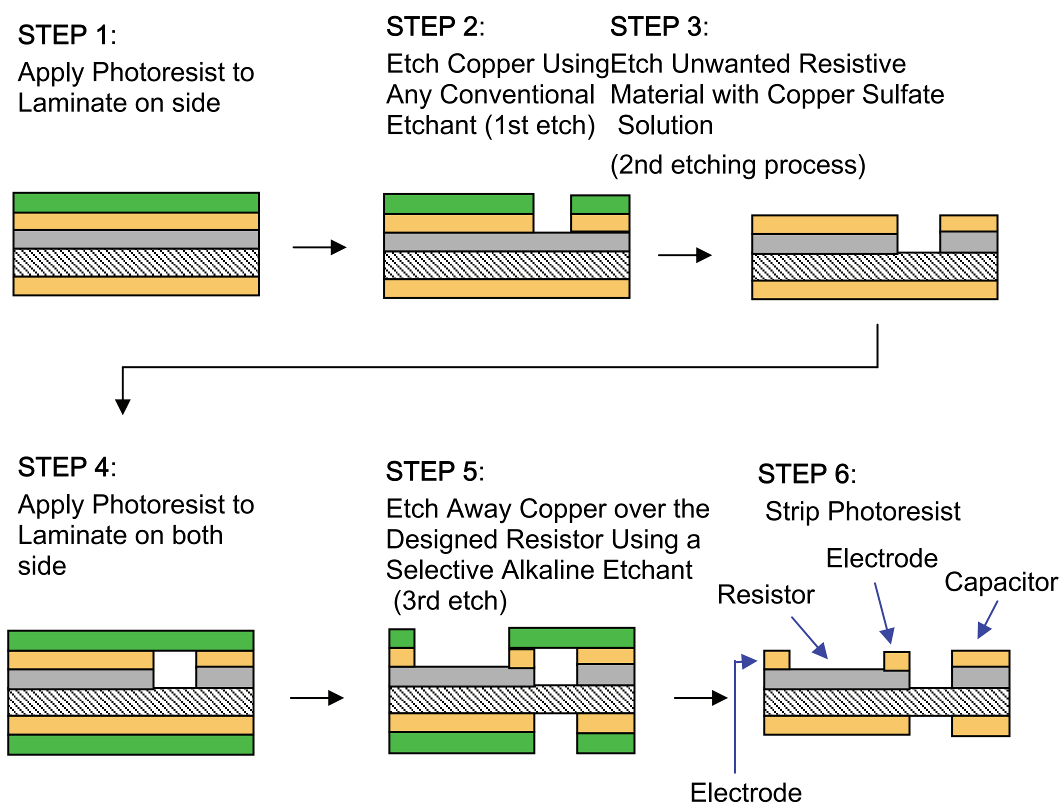


Figure 2 - Process Flow for forming Capacitor Planes and Resistors

For the unfilled or partially filled materials the dielectric is strong enough to allow etching of both sides of the laminate at the same time. For highly filled material, sequential processing is required. This involves etching the copper on only one side to form the bottom capacitor plane and then laminating this side to dielectric material. The dielectric supports the thin capacitor material during the etching of the top copper and resistive layers.

Electrical performance of PCB using R/C Material

Numerous articles have been published on the benefits of embedded capacitors [3,4] and resistors [5]. Two of the principle performance benefits of the thin power/ground planes are the reduction of the power distribution system impedance as well as reduction in resonances at higher frequencies. This is shown in Figure 3. The Figure demonstrates that the thinner the dielectric the better the performance at both low and high frequency. Raising the dielectric constant provides additional performance at the lower frequencies, but has no impact at higher frequencies on improving resonances. This effect was described by Grebenkemper[6], but he also demonstrated that other factors effect the resonances at higher frequencies. Unlike signal propagation, in which we want low loss, a good power distribution, as pointed out by this article, could benefit by higher loss. Loss can be introduced through a dielectric with a higher loss tangent, but can also be provided by a more resistive conductor layer. Modeling he conducted indicated that by putting a resistive layer between the copper and dielectric the noise level can be reduced by an additional 7 db. We are in the process of verifying this on actual test vehicles.

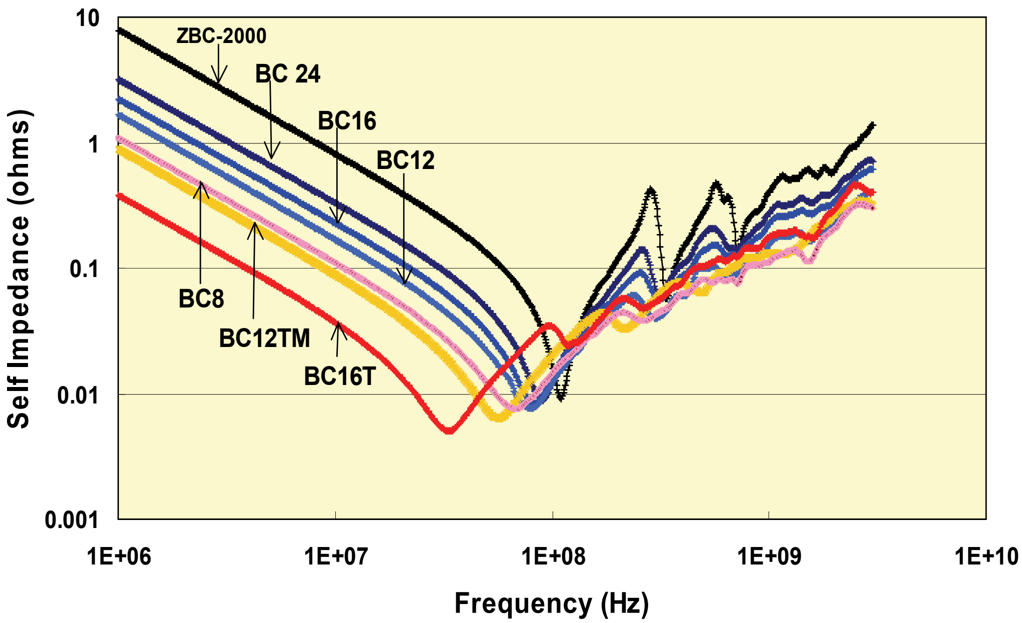
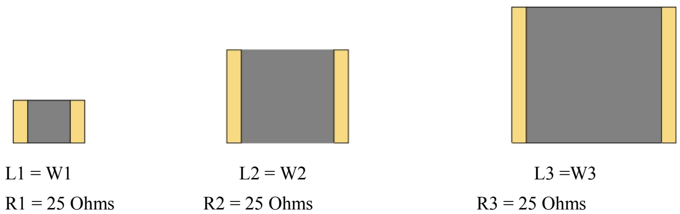


Figure 3 - Impedance versus Frequency for various thickness and Dk substrates

The capacitive performance is expected to be better with the resistive material added to the substrate, but it has also been discovered that the resistive performance is enhanced by being on the capacitive material. As mentioned earlier, the power density is significantly higher when the resistor is on the capacitor material versus standard FR4. Resistive material is specified in ohms/square. The resistor value is a function of the width to length ratio, with long thin resistors having higher values than short wide ones. Resistors with the same form factor will have the same resistor value. The size of the resistor that is ultimately specified is based on the power that it is expected to carry. The higher the power requirement, the larger the resistor that is needed. This is so that the heat can be dissipated. With the higher power density of the R/C material, smaller resistors can be used and allow further optimization of area on the PCB. Figure 4 demonstrates this fact.



Resistor 3 has the same resistance as resistor 1 but can handle 3 times the power if on the same FR4 substrate. Resistor 1 on capacitive substrate could handle the same power as resistor 3 on FR4.

Figure 4 - Sizing of Resistors

Applications

As was mentioned earlier, the largest use of embedded capacitors is to lower the impedance of the power distribution system and reduce the resonances (and thus also reduce EMI) at high frequency. For resistors the main applications have been where the need was to reduce the surface area required for passive devices as well as improve reliability. Improved electrical performance was an additional benefit. A number of designs need to utilize both materials, but have had to use individual layers to get the functionality. With the combined R/C material these can now be incorporated into the same substrate.
Each material can be utilized individually or can be combined in the same circuit as required. Some possible R/C combinations are shown in Figure 5, R8 – R12.

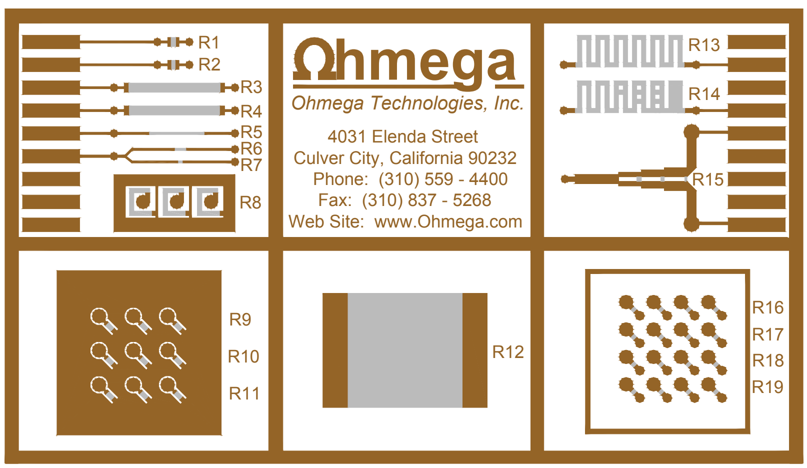


Figure 5 - R/C Networks on a PCB Demo board. Gray area is resistive material

For these same high speed applications another way of utilizing the material is to tailor the equivalent series resistance (ESR) of the large surface discrete capacitors that are needed for energy storage. As described in the previously cited paper by Grebenkemper[6)] it is desirable to spread high ESR capacitors across the PCB to help dampen resonances and use low ESR capacitors as close as possible to devices that have significant change in their current requirements. By introducing a resistive element between the power plane and the capacitor, one can adjust the ESR to the exact amount needed to optimize the dampening performance. Where low ESR is needed the capacitors can be directly attached to the copper on the power plane. This can result in a reduction in the number of different discrete capacitors as the low ESR capacitors can now be used in both applications. Grebenkemper also indicates that the number of capacitors can also be reduced, as higher ESR capacitors are much more effective at dampening noise.

Having both resistive and capacitive material available allows the formation of passive devices. One example is a band pass filter. These are devices that either block or allow certain frequencies to be utilized by an analog circuit. These devices have become extremely important, as the world continues to go wireless. If inductors are also needed, they can be formed by making spirals on one or both of the copper layers. Thus an LRC circuit can be realized on one substrate. One special type of LRC circuit that is utilized is the one for radio frequency identification tags (RFID). RFID tags store data in chips that are accessed wirelessly. Active tags have there own energy source (such as a battery) and have the ability to both receive and send data. Passives tags do not have their own energy source and utilize radio frequency energy so the data can be read.

They are usually read only. The R/C material can be used in conjunction with the copper planes forming the inductors (antenna) to provide all the necessary passives devices for the tags. To complete a passive tag only the chip would need to be mounted. For an active tag the battery would also need to be provided.

Conclusion

Embedded Passive technology has been utilized for several years and in millions of PCBs. With the increase in processor and data rate transfer speeds, as well as the ever present pressure to reduce size and lower overall cost, the impetus is for expanding use of this technology. Discrete passive component manufactures are addressing the space issue by further shrinking the size of the components. This opens up new issues as it is extremely difficult to place these SMT components which can result in missing, misplaced components and "tombstoning" or other solder joint failures. Also, no matter how small the components, vias will still be needed to connect to them, and there are limitations to how small they can become. In addition, the move to lead-free solders has many manufacturers concerned about the reliability of surface mount components. Embedding as many components as possible with reduce the risk of joint failure (since the solder joints are now replaced with highly reliable PCB interconnects).

It has been demonstrated that by combining the resistive and capacitive functions on one substrate, the performance of both materials are enhanced and can lead to better material utilization. Having a material solution that combines both resistive and capacitive capability will further advance the use of Embedded Passive technology and allow for unique and clever solutions in PCB design and organic chip packaging.

Acknowledgement

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