A Comparison of Small Discretes and Polymer Thick Film Embedded Resistors for Mobile Phone Applications

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Abstract
As an increasing amount of functionality is crammed into today's mobile phones, designers must find ways to save board area. Two common solutions are the use of embedded passives and the use of smaller (0201) discretes. In this paper, we examine the cost and area tradeoffs between small discretes and embedded polymer thick resistors. Three typical mobile phone designs are analyzed using high volume assembly and state of the art board fabrication techniques for scenarios with either small discretes or polymer thick film (PTF) resistors. The size and cost impacts of each option are presented.

Introduction
One major challenge of the mobile phone industry is to put more functionality into the same area. While cell phones are not necessarily becoming smaller, what was once a cell phone is now a cell phone plus PDA, camera, video monitor, GPS, and so on. This results in a large increase in the "functionality density" of the phone. Creating a larger phone is not an option, so this additional functionality must be realized using the same board area. Because these boards are already dense, techniques to release the board surface area must be utilized.

The other main driver in the mobile phone industry is cost. The competitive nature of this market means profit margins are small, and a few cents may be the difference between a successful product and a failure. Higher density designs may or may not increase the total product cost. The additional cost of placing small devices and/or embedding resistors in the board may be offset by a reduction in the board size and cost. Alternatively, the additional board area could be utilized to add more functionality, enabling a higher price for the phone. It is critical that each situation be analyzed thoroughly for the optimal size and cost decision.

Polymer Thick Film (PTF) Option for Size and Cost Reduction
One way to release board area is to embed the passives in the board instead of placing them on the board. Although each device is small by itself, there are many embeddable resistors in a cell phone. The board area available for other functionality includes the area of each embedded device plus the assembly spacing around each device.

The graph in Figure 1 shows a typical process flow for embedded PTF resistors. These steps are done on one or more inner layer pairs and are in addition to the normal inner layer processing. Following are the key cost drivers for this process.

- *Paste and paste printing cost* – A high precision screen printer must be used for the PTF fabrication process. The cost of the paste used (and wasted) in this process must also be considered.

- *Laser trimming cost* – The tolerance of untrimmed resistors will only be +/- 20%. Therefore, to achieve e.g. +/- 5% accuracy, each resistor must be measured and laser trimmed to fall within spec. Because each device must be measured, either a fixed probe card approach or a flying probe approach will be used to measure the device during laser trimming. Fixed probe cards increase the throughput of the process, but the probe cards themselves add expense, and therefore fixed probe cards should not be used in prototyping. However, in high volume production, the cost per board of the probe cards is relatively small and it is more cost effective to use fixed probe cards.

- *Yield hit cost* – Yield is often the dominant cost driver for the PTF fabrication process. Unlike discrete passives that can be reworked, one bad embedded passive on a board results in the scrapping of the entire

board. Since the board cannot be scrapped until after the majority of the fabrication process has occurred, the scrap cost can be quite high.

- *Resistance testing cost* – Each device must be tested after the board is completed. This is typically done with a flying probe test system for low volume, but as with laser trimming, a fixed probe card or bed-of-nails test approach should be used for volume production. This will significantly increase the throughput of resistance testing.
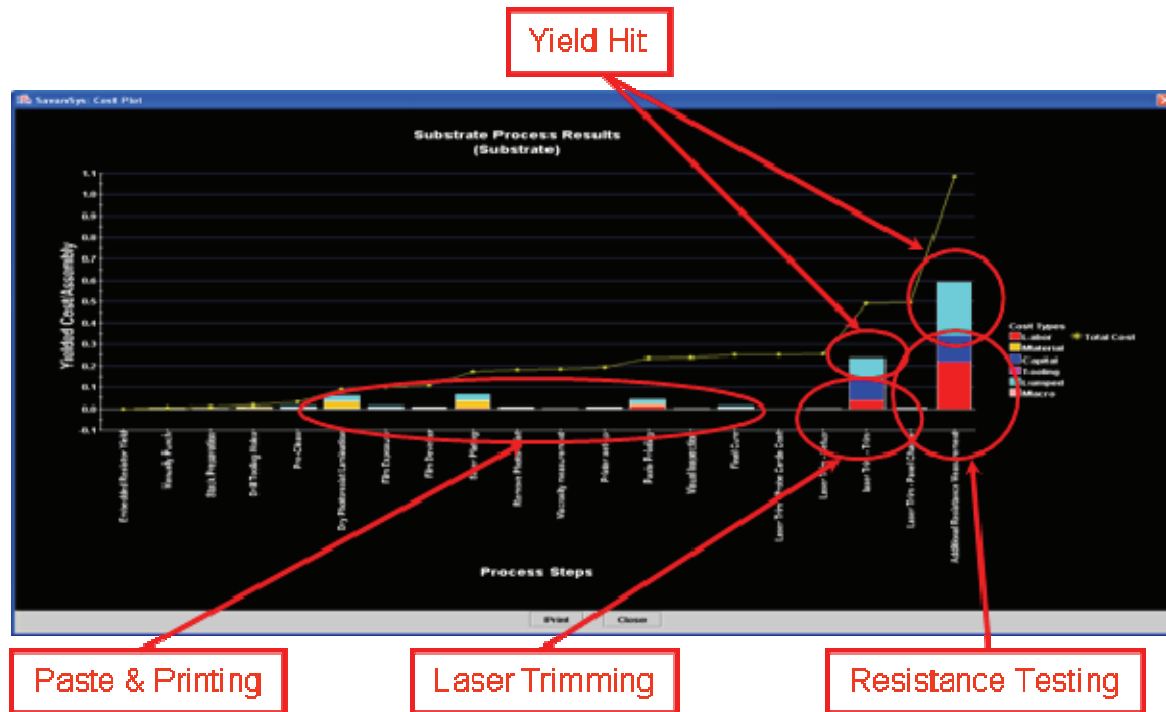

Figure 1 – Typical PTF Process Flow

The use of PTF devices provides the following two opportunities for cost savings.

- *Smaller board size* – A smaller board size may be less expensive if the size reduction is sufficient to increase the number of boards on a fabrication panel. Most of the board fabrication cost is spent to fabricate a complete panel. This panel cost is then divided by the number of boards per panel. If the number of boards per panel increases, the cost per board will be reduced.

- *Reduced assembly and component cost* – Embedding passives means there will be fewer components to assemble. The reason behind this cost savings results from a reduction in solder joints and component costs. However, because the cost of small discrete resistors is minor, the majority of the cost savings results from the reduction of assembly labor and time.

0201 Discrete Option for Size and Cost Reduction
The use of small discretes affects the cost of the board assembly process. Unlike the PTF option that affects both the fabrication and assembly processes, the use of 0201 discretes impacts only the assembly process. The graph in Figure 2 shows a high volume assembly flow and the specific activities that are affected the most. The key cost differences between assembly with 0402 devices and 0201 devices are:

- *Equipment cost* – Modern assembly equipment is required to handle 0201 device placement. This often requires a significant capital investment.

- *Lower yield* – The assembly yield is directly related to the precision of the placement process. In many cases, the tolerance of the placement process approaches the size of 0201 devices, and this will result in lower assembly yield and more rework.

- *Higher rework cost* - The cost to rework small devices is higher because of the increased difficulty.

- *Inspection cost* – Visual inspection and AOI will be more challenging due to the small size of 0201 devices, and therefore the cost will be somewhat higher. This additional cost is relatively minor.
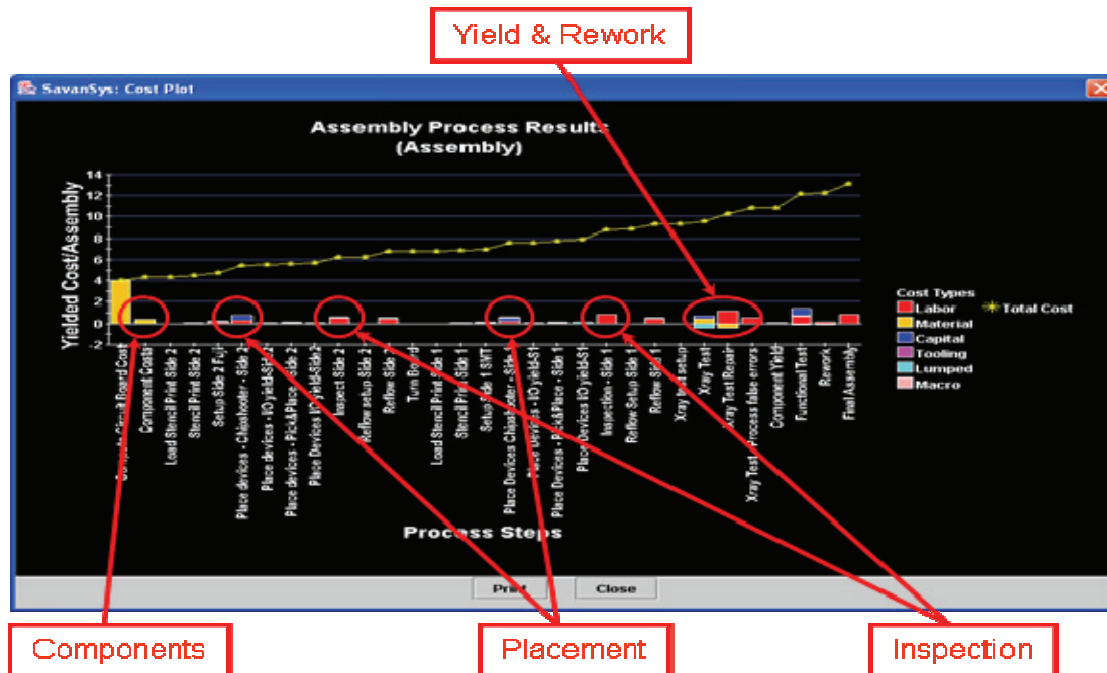

Figure 2 – Typical SMT Assembly Flow

The area savings resulting from the use of 0201 devices instead of 0402 devices is the difference in total board area consumed by each. The total board area consumed is the total of the device area, the pad area, and the assembly spacing around the device. Even though an 0201 device is only 25% of the size of an 0402 device, it is a mistake to assume that an area savings of 75% can be achieved through the use of 0201 devices. Figure 3 compares a typical device, pad, and assembly spacing of an 0201 with an 0402 device. The 0201 savings in this example is only 36%. Figure 4 shows two adjacent 0201 devices with 0.2mm minimum component spacing.
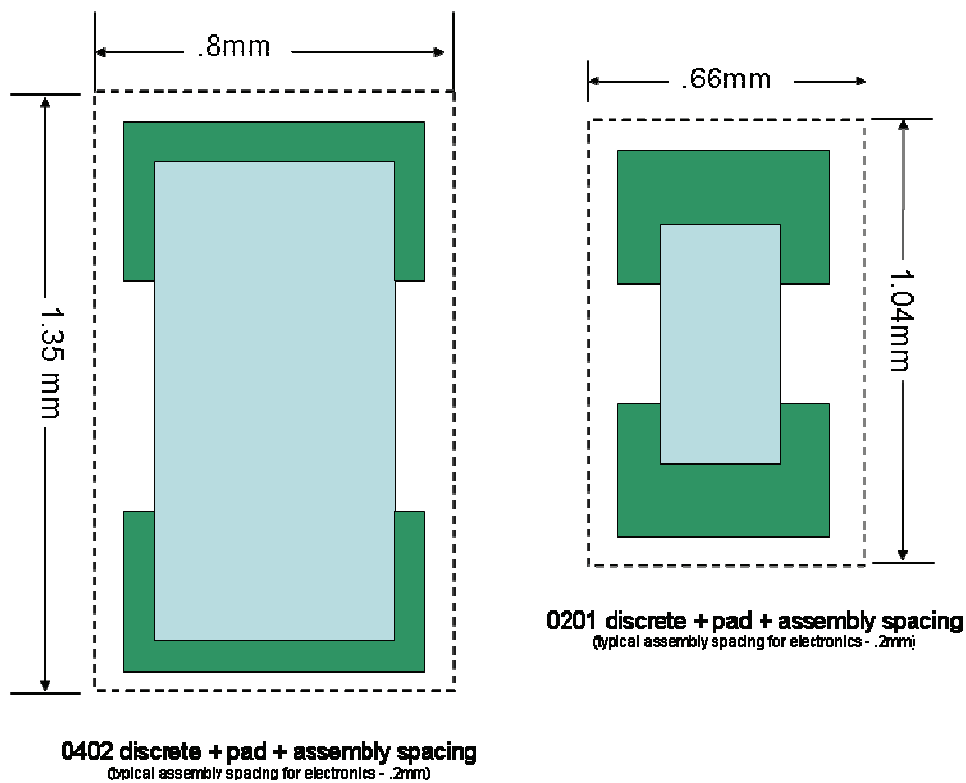
.8mm

1.35 mm

0402 discrete + pad + assembly spacing
(typical assembly spacing for electronics - .2mm)

.66mm

1.04mm

0201 discrete + pad + assembly spacing
(typical assembly spacing for electronics - .2mm)

Figure 3 – Area Savings 0402 devices vs. 0201 Devices
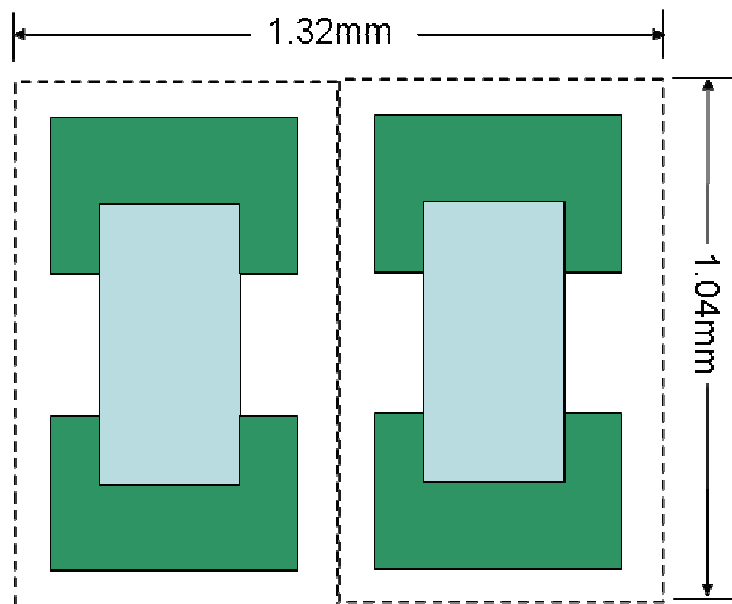

1.32mm

1.04mm

Figure 4 – Two 0201 Devices with Typical .2mm Assembly Spacing for Electronics

Cost Comparisons of Three Typical Phone Designs

In this section, we analyze three typical phone designs for cost and area savings with a variety of small device and embedded PTF scenarios. The *SavanSys* technology and manufacturing models representing typical industry costs and capabilities are used. The costs given do not represent specific costs for Nokia or any other manufacturer.

The following assumptions were used in the manufacturing cost models:

Discrete costs are all .001 Euro. No difference was assumed between the cost of 0201 devices and 0402 devices. Although there is a difference in those component costs today, over time, the cost of 0201s will drop.

- Annual volume is two million boards, and lifetime volume is ten million boards,

- Both assembly and fabrication are done in either Europe or North America. Manufacturing in Asia would change the labor costs; however, this change would not have a large overall effect, since both fabrication and the assembly processes are highly automated and only have a small labor component.

- A fabrication panel size of 61cm by 55cm is used, and individual boards are delivered to the assembly factory. This is somewhat different from the typical process of delivering multiple boards per assembly panel, but moving to single board delivery (or the ability of assembly factories to handle bad boards in a panel) is critical for the use of embedded passives.

Overview

The software used to analyze these is described below. The software is an activity based cost and yield modeling technology. For additional information on the capabilities and availability of this technology, please contact the authors.

The software is a size, cost, yield, and technology tradeoff tool. Data is extracted from the design tool environment, or through spreadsheets containing the bill of materials (BOM), to create a physical representation of the design. Activity based models of both board fabrication and assembly are created to model the manufacturing process. This combination of design and manufacturing information is used to generate a "virtual prototype" of the board to accurately determine size, cost, and yield throughout the complete (fabrication and assembly) manufacturing process. The results of this simulation are extremely accurate because it considers the details of the target board built in a specific manufacturing environment with precise costs and yields.

The data considered in this analysis is listed below.

The Design Model

Because of the large number of packaging technologies, processes, and materials that are available, making optimum choices is not a trivial task.

The software accepts physical information that describes multiple chips (or bare die) and their interconnection. All of the information collected by the software is physical as opposed to logical, behavioral, or functional. The software does not import VHDL or similar behavioral information because such descriptions do not contain a significant amount of useful, physical information. The software inputs and considers the following physical data.

- Chips (bare die and packaged die):
- Dimensions (length, width, thickness)
- I/O type and count
- Cost and yield
- Bonding and package type

Process flow information (chip preparation, testing, and burn-in)

Boards/Modules:
- Substrate (technology, materials, and design rules)
- Connectorization (technology, materials, and design rules)
- Process flow information (substrate fabrication and assembly process)

- Module size prediction is accomplished by computing the following set of footprints for each component (active and passive) in the board.

- The interconnect-capacity footprint is the size limitation based on the amount of wiring required to connect a component within the module. It depends on the wiring capacity of the substrate and the quality of the routing.

- The via-density footprint accounts for the number of vias available to connect component I/O to wiring layers.

- The bond-pad-density footprint accounts for the distribution of bond pads on the surface of the interconnecting substrate.

- The escape-routing footprint analyzes the minimum required layers to route BGA connections away from the package area.
- The placement or die footprint represents the physical size of the bare die or packaged chip and its surrounding bonds, as well as minimum spacing to adjacent components.

In order to obtain the module area, the footprints representing each component are accumulated.
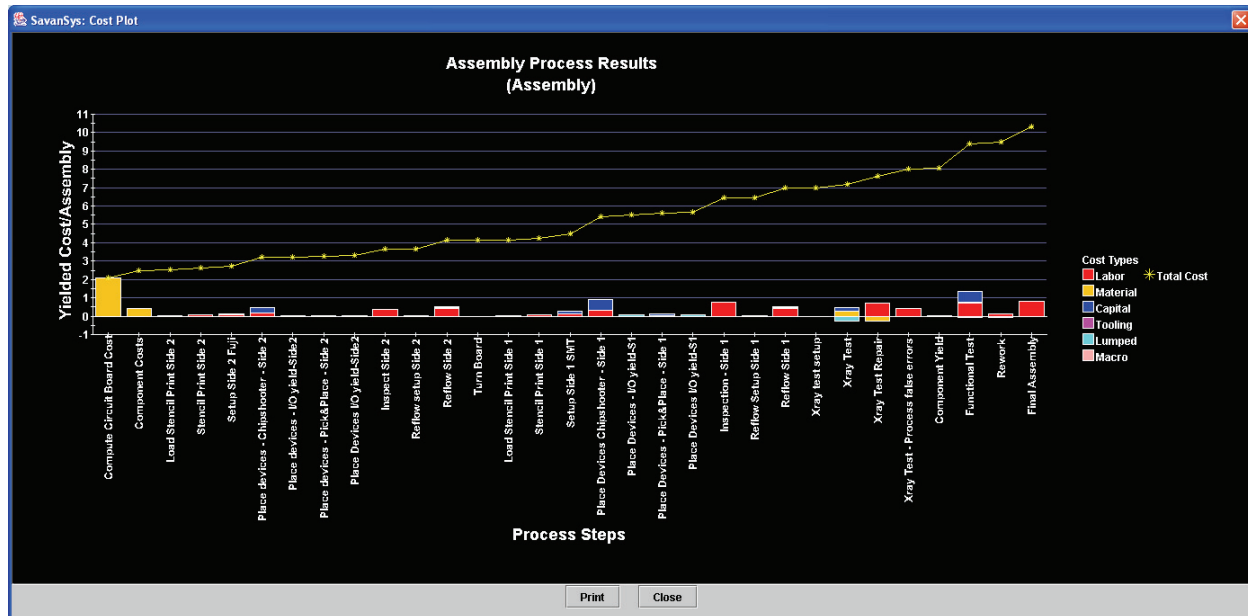

Figure 4 - Cost Plot

The Manufacturing Model

The plot in Figure 4 shows the results of a cost analysis. Cost models may include the following costs and yield. Given that the costs listed below are optional, models can be used to analyze total system costs or specific components of the system cost. Many of these costs can either be directly entered by the user, computed using a calculation, or simulated using a full process flow.

- Component cost and yield (entered or computed)
- Component preparation (entered or process flow)
- Single chip package cost and yield (entered or computed)
- Substrate fabrication cost and yield (entered, computed, or process flow)
- Surface mount and through-hole assembly cost and yield (entered or process flow)
- Bare die attach cost and yield (entered or process flow)
- Tooling costs associated with assembly processes
- Test, repair, and rework costs, coverages, success rates, and yields (entered or process flow)

The methodology for defining cost models in *SavanSys* is based on dividing the process into a series of activities and then defining the costs, times, and yields associated with each activity. Step types are one of the following:

- Substrate – This type of step calculates the cost and yield of the substrate by either using a user defined calculation or running a substrate fabrication process flow.

- Component – This type of step adds the cost and yield of new components to a system.

- Assembly – This type of step defines the cost and yield of board assembly activities.

- Processing – This type of step defines the cost and yield of board fabrication activities.
- Test - This type of step defines testing activities. Defects introduced into the system by previous steps are detected by this type of step, and the board/panel is either fixed through rework or scrapped.

- Rework – This type of step defines the repair/rework activities.

Figure 5 – Develop Step Details

The details of step definitions vary based on step type, but all types include the following basic information:

- Time – Used to calculate labor and equipment costs
- Operator utilization and rate – Combined with time to obtain cost
- Equipment utilization and cost – Combined with time and depreciation schedule to determine allocated cost
- Defects in parts per million/defects per square cm – Used to calculate and accumulate the system yield
- Tooling costs – Divided over the lifetime quantity of boards
- Material and amount used – References the material database to calculate material costs

The screen shot in Figure 5 shows an example step definition for a develop step.

Design Results

For each design, the following six size comparison scenarios were run:

- *Baseline - .2mm assembly spacing* – This scenario gives the size, surface density, and routing utilization of the existing mobile phone design.

- *0201 Rs - .3 mm assembly spacing* – For this scenario, the embeddable resistors in the design are converted from 0402 devices to 0201 devices using a .3mm assembly spacing.

- *0201 Rs - .2mm assembly spacing* – For this scenario, the embeddable resistors in the design are converted from 0402 devices to 0201 devices using a .2mm assembly spacing.
- *0201 Rs - .15mm assembly spacing* – For this scenario, the embeddable resistors in the design are converted from 0402 devices to 0201 devices using a .15mm assembly spacing.

- *0201 All* – For this scenario, all 0402 devices in the design are converted to 0201 devices.

- *Embedded R* – For this scenario, all embeddable resistors in the design are embedded.

- For each design, the following six cost comparisons were run:

- *Baseline* – This is the baseline board, assembly, and partial component cost. No attempt is made in any of these analyses to calculate component costs of the active devices.

- *0201 Rs - .2 mm spacing* – This is the total cost of a design with a combination of 0402 devices and 0201 devices. The devices converted to 0201 are all of the resistors that are able to be embedded. The size of the board is not changed from the baseline.

- *0201 All - .2mm spacing* – This is the total cost of a design with all 0402 devices converted to 0201s. The size of the board is not changed from the baseline.

- *0201 All with size reduction* – This is the total cost of a design with all 0402 devices converted to 0201s. The size of the board is reduced by the amount of area savings resulting from the use of the smaller devices.

- *Embedded R* – This is the total cost of a design with embedded resistors. The size of the board is not changed from the baseline.

- *Embedded R with size reduction* – This is the total cost of a design with embedded resistors. The size of the board is reduced by the amount of area savings resulting from the use of the smaller devices.

Design1 Results

Tables 1 and 2 display the results of these six size and cost scenarios run on the first mobile phone design. This design has the following characteristics:

- 41 actives
- 389 passives
- 90 embeddable resistors
- 289 small passives (0402)

Table 1 – Size Results for Design1

	Surface Density	Routing Utilization	Board Area
Baseline - .2mm spacing	83.32%	12.35%	47.87 sq.cm.
0201 Rs - .3mm spacing	82.93%	12.35%	47.87 sq.cm.
0201 Rs - .2mm spacing	82.47%	12.35%	47.87 sq.cm.
0201 Rs - .15mm spacing	82.23%	12.35%	47.87 sq.cm.
0201 All - .2mm spacing	80.42%	12.35%	47.87 sq.cm.
Embedded R	80.64%	13.87%	47.87 sq.cm.

Table 2 – Cost Results for Design1

	Total	Partial Component Cost (Discretes Only)	Assembly Cost	Board Cost	First Pass Assembly Yield	Board Area	Surface Density
Baseline	**13.98 €**	0.50 €	9.40 €	4.08 €	94.03%	47.87 sq.cm.	83.32%
0201 Rs - .2mm spacing	**15.09 €**	0.50 €	10.51 €	4.08 €	92.89%	47.87 sq.cm.	82.47%
0201 All - .2mm spacing	**15.58 €**	0.50 €	11.00 €	4.08 €	91.15%	47.87 sq.cm.	80.42%
0201 All with size reduction	**15.50 €**	0.50 €	11.00 €	4.00 €	91.15%	47.17 sq.cm.	83.32%
Embedded R	**14.07 €**	0.37 €	8.51 €	5.19 €	94.66%	47.87 sq.cm.	80.64%
Embedded R with size reduction	**13.98 €**	0.37 €	8.51 €	5.10 €	95.00%	47.22 sq.cm.	83.32%

For this design, the area savings of embedding 90 resistors are approximately the same as the area savings resulting from converting 289 0402 devices to 0201 devices. However, the cost of the 0201 option exceeds the embedded option by 1€.

Design2 Results

Tables 3 and 4 illustrate the results of these six size and cost scenarios run on the second mobile phone design. This design has the following characteristics:

- 69 actives
- 353 passives
- 47 embeddable resistors
- 248 small passives (0402)
-

Table 3 – Size Results for Design2

	Surface Density	Routing Utilization	Board Area
Baseline - .2mm spacing	84.51%	6.13%	47.78 sq.cm.
0201 Rs - .3mm spacing	84.35%	6.13%	47.78 sq.cm.
0201 Rs - .2mm spacing	84.18%	6.13%	47.78 sq.cm.
0201 Rs - .15mm spacing	84.10%	6.13%	47.78 sq.cm.
0201 All - .2mm spacing	82.43%	6.13%	47.78 sq.cm.
Embedded R	83.51%	6.39%	47.78 sq.cm.

Table 4 – Cost Results for *Design2*

	Total	Partial Component Cost (Discretes Only)	Assembly Cost	Board Cost	First Pass Assembly Yield	Board Area	Surface Density
Baseline	12.69 €	0.35 €	8.34 €	4.00 €	94.70%	47.78 sq.cm.	84.51%
0201 Rs - .2mm spacing	13.22 €	0.35 €	8.87 €	4.00 €	94.29%	47.78 sq.cm.	84.18%
0201 All - .2mm spacing	13.65 €	0.35 €	9.30 €	4.00 €	92.53%	47.78 sq.cm.	82.43%
0201 All with size reduction	13.65 €	0.35 €	9.30 €	4.00 €	92.53%	47.28 sq.cm.	84.51%
Embedded R	12.85 €	0.30 €	7.99 €	4.56 €	94.94%	47.78 sq.cm.	83.51%
Embedded R with size reduction	12.85 €	0.30 €	7.99 €	4.56 €	94.94%	47.54 sq.cm	84.51%

For this design, only 47 resistors can be embedded. Therefore, the cost effect and area savings gained from embedding are less than those seen with the first design. Greater area savings can be achieved with 0201 devices, but,, there is a cost penalty associated with this approach. There is no difference in the total cost for either the small discretes or the embedded resistors approach because neither option resulted in more boards pre panel.

Design3 Results

Tables 5 and 6 show the results of these six size and cost scenarios run on the third mobile phone design. This design has the following characteristics:

- 41 actives
- 389 passives
- 90 embeddable resistors
- 289 small passives (0402)

Table 5 – Size Results for Design3

	Surface Density	Routing Utilization	Board Area
Baseline -.2mm spacing	109.10%	8.88%	25.66 sq.cm.
0201 Rs - .3mm spacing	108.60%	8.88%	25.66 sq.cm.
0201 Rs - .2mm spacing	108.00%	8.88%	25.66 sq.cm.
0201 Rs - .15mm spacing	107.70%	8.88%	25.66 sq.cm.
0201 All - .2mm spacing	104.60%	8.88%	25.66 sq.cm.
Embedded R	105.60%	10.39%	25.66 sq.cm.

Table 6 – Cost Results for Design3

	Total	Partial Component Cost (Discretes Only)	Assembly Cost	Board Cost	First Pass Assembly Yield	Board Area	Surface Density
Baseline	9.78 €	0.38 €	7.30 €	2.10 €	95.81%	25.66 sq.cm.	109.10%
0201 Rs - .2mm spacing	10.40 €	0.38 €	7.92 €	2.10 €	95.19%	25.66 sq.cm.	108.00%
0201 All - .2mm spacing	10.63 €	0.38 €	8.15 €	2.10 €	94.01%	25.66 sq.cm.	104.60%
0201 All with size reduction	10.54 €	0.38 €	8.14 €	2.02 €	94.01%	25.08 sq.cm.	109.10%
Embedded R	9.74 €	0.30 €	6.70 €	2.74 €	96.26%	25.66 sq.cm.	105.60%
Embedded R with size reduction	9.65 €	0.30 €	6.70 €	2.65 €	96.26%	25.21 sq.cm.	109.10%

For this design, 90 resistors are embeddable and the original board is significantly smaller than the first two designs. Because of this relatively high resistor density, there is a slight cost advantage to using embedded passives even without size reduction.

Conclusions and Key Findings

Below is a list of key findings and conclusions drawn from this exercise.

The cost drivers, not the actual cost numbers, are the most important result of this analysis.
Because the numbers used in this exercise do not represent the actual costs for a particular manufacturer, the conclusions regarding whether or not PTF or small discretes will be cost effective will differ across the industry. For your applications, it is important to use the correct numbers for your own cost structure and supply chain to generate your own, accurate numbers. On the other hand, the cost drivers do not depend on specific manufacturers, but are, instead, unique to the technology used for assembly or fabrication. Therefore, these cost drivers apply equally well to similar designs across the industry.

The major cost drivers for 0201 assembly are lower assembly yield, higher equipment costs, and more difficult rework.

Other factors in the assembly process, such as device cost and increased inspection, can also be different, but the dominant differences are assembly yield, equipment costs, and rework time. If, through the use of 0201 devices, the design can be reduced enough to include more boards per fabrication panel, size will also become a cost driver.

The major cost drivers for embedded PTF are yield per embedded device and laser trimming cost.

The point of interest regarding this result is not, in fact, what the major cost drivers *are*, but what they are not. Historically, designers used embedded resistor density as a measure of suitability for embedding. While this is still useful for larger boards, for mobile phone style boards, resistor density is no longer a dominant cost driver. This is due to the fact that the density of resistors is already high enough that the variable costs per resistor (yield per device and laser trimming cost and time) are dominant. Embedded resistor density is still a factor, but as can be seen from these three designs which exhibit a large range in resistor density, the cost effects are similar. The fixed costs of extra processing steps, silver plating, paste printing, etc. are relatively small contributions to the total fabrication cost of these designs. If the design can be reduced enough to include more boards per fabrication panel through the use of PTF embedded passives, size will also become a cost driver.

Embedding one resistor reduces the board area approximately the same amount as converting three 0402 devices to 0201 devices.

Embedding a resistor releases the board area by 100% of the area used by that resistor. Since the conversion of a 0402 device to an 0201 device releases the surface area consumed by that device by 36%, it will take approximately three converted devices to achieve the same savings as with one embedded resistor.

Risk should be considered.

Given that this analysis and series of results are largely based on a set of assumptions, it is important to understand and take into account the risk associated with any "bad assumptions" when considering 0201 devices or PTF resistors. The lowest risk implementation is undoubtedly the use of 0402 devices. While neither 0201 devices nor PTF fabrication have a great deal of technological risk, both contain some cost risks. For example, the yield per embedded resistor is assumed to be 99.95%; many suppliers can and have achieved these levels. However, if a supplier can only achieve 99.5% per device, the cost will change dramatically. Similarly, the assembly defect rate of 0201 devices is assumed to be 40 defects per million opportunities (DPMO) per solder joint. If this cannot be achieved, there will be significant amounts of rework and potentially scrap of full assembly boards involved in the cost. If less than 40 DPMO per solder joint can be achieved, the cost penalty of using 0201 devices will be less.

Summary

The analysis of three typical mobile phone boards has illustrated that both 0201 discretes and embedded PTF resistors can contribute to reducing the size of next generation mobile phone designs. For each case considered, the cost of the 0201 option is greater than that of the equivalent design using 0402 devices. However, the embedded PTF option reduces more board area and, in some cases (Design1 and Design3), also reduces the total product cost.