

MANDALAY BAY RESORT AND CONVENTION CENTER LAS VEGAS, NEVADA

## Reliability of Embedded Planar Capacitors: A Review

NEW IDEAS ... FOR NEW HORIZONS

## Michael H. Azarian, Ph. D.





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## Outline

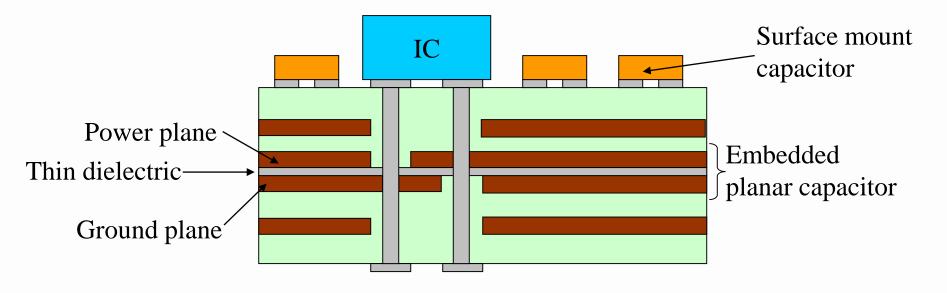
### Introduction

- Overview of Reliability Studies
- Conduction Mechanism
- Conclusions



## NEW IDEAS ... FOR NEW HORIZONS LASV Embedded Planar Capacitors

- Embedded planar capacitors are thin laminates embedded inside a PWB that serve both as a power/ground plane and as a parallel plate capacitor.
- These laminates extend throughout the board and consist of a thin dielectric (8-50 µm), sandwiched between two copper layers.
- Their low parasitic inductance makes them effective replacements for discrete local decoupling capacitors that function at high frequency.

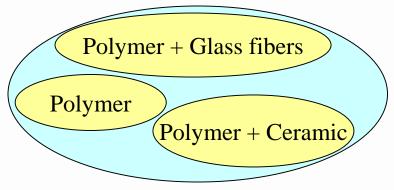






### NEW IDEAS ... FOR NEW HORIZONS Dielectric Materials

- The dielectric material in a planar embedded capacitor can be:
  - Polymer (such as epoxy or polyimide)
  - Polymer reinforced with glass fibers (to provide mechanical strength).
  - Polymer filled with high dielectric constant ceramic



- The dielectric constant of pure polymer or polymer reinforced with glass fibers is low (typically <5).
- Polymer ceramic composite (polymer filled with ceramic powder) is one of the most promising materials for embedded capacitors due to its higher dielectric constant.



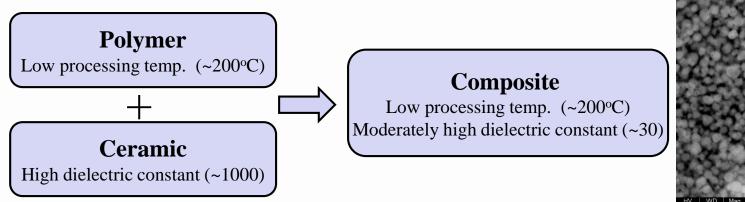
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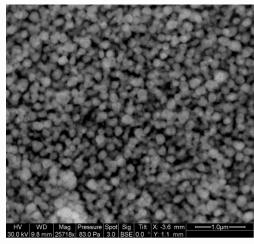
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## Why Polymer-Ceramic Nanocomposites?

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 Pure ceramic dielectrics are brittle and require processing temperatures (~1100°C) that are much higher than the processing temperature of typical PWB manufacturing process (~300°C).





- The polymer typically used is epoxy.
- The ceramic widely used is Barium Titanate (BaTiO<sub>3</sub>) whose dielectric constant ( $\varepsilon$ ) can be as high as 15,000 in the crystalline phase.

The effective dielectric constant ( $\varepsilon_c$ ) of the composite can be increased by increasing the ceramic loading (up to 50-60% by Vol.)





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## **Reliability of Embedded Planar Capacitors**

- Failure of an embedded capacitor can lead to board failure since these capacitors are not reworkable.
- Change in electrical parameters of an embedded capacitor, such as:

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- capacitance (C),
- dissipation factor (DF), and
- insulation resistance (IR),

can affect a circuit connected to these capacitors.





## Motivation for CALCE Research on Embedded Planar Capacitors

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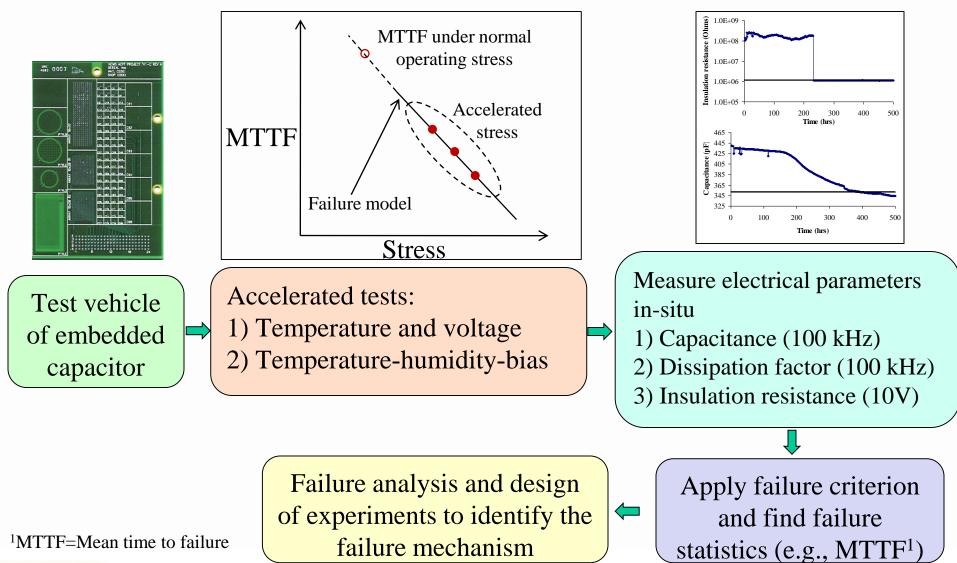
- Adoption of embedded planar capacitors would be encouraged by availability of
  - failure models;
  - long term reliability data; and
  - insights into failure mechanisms
    (e.g., the mechanism of leakage current).



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## **CALCE's Reliability Testing of Embedded Capacitors**

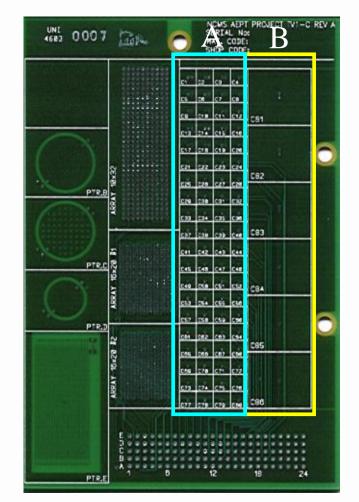




## **Test Vehicle**

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- The *test vehicle* was a 4-layered PWB in which a commercially available planar capacitor laminate formed layer 2 and layer 3.
- The *power plane was etched* at various locations to form individual capacitors and the ground plane was continuous.
- *Two sizes* of capacitor were investigated:
  - Group A (small): 0.026 in<sup>2</sup>, 400 pF; 80 capacitors/test vehicle
  - Group B (large): 0.19 in<sup>2</sup>, 5 nF;
    6 capacitors/test vehicle.
- The *failure criteria* used were:
  - 20% decrease in capacitance (C)
  - increase in dissipation factor (DF) by a factor of 2
  - drop in insulation resistance (IR) to approximately 1.1 MOhms.

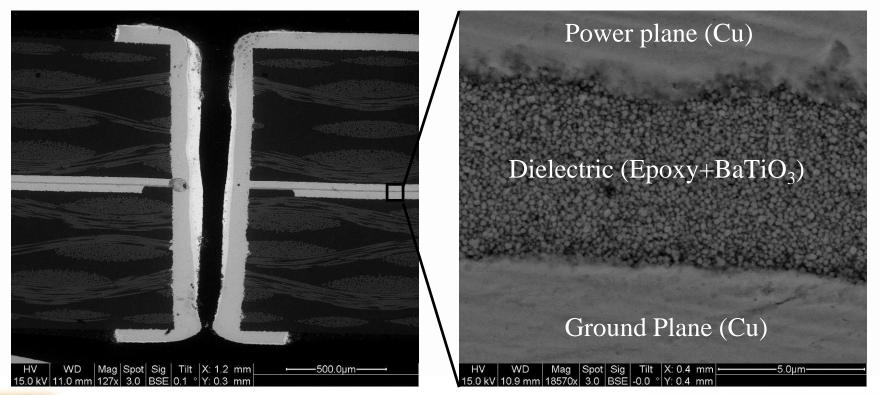




## Sectional View of an Embedded Capacitor

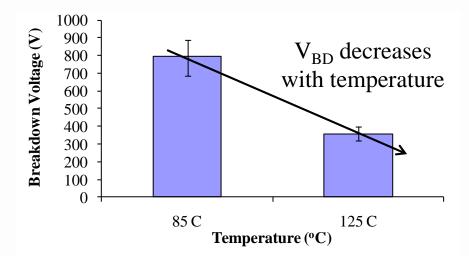
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- Each capacitor had its power plane connected to a PTH and the ground plane was common for all capacitors.
- The dielectric (8  $\mu$ m thick) was a composite of BaTiO<sub>3</sub> of 250 nm mean diameter loaded to 45% by volume in epoxy.





- Maximum temperature  $(T_{max})$  and voltage  $(V_{max})$  were selected such that:
  - $T_{max} < 130^{\circ}C$  (maximum operating temperature of the PWB).
  - V<sub>max</sub> < V<sub>BD</sub> (breakdown voltage at that temperature).



Measurement of breakdown voltage ( $V_{BD}$ ) on 10 small capacitors

• The reduction in the breakdown voltage with temperature can be explained by an increase in free volume of the polymer matrix.



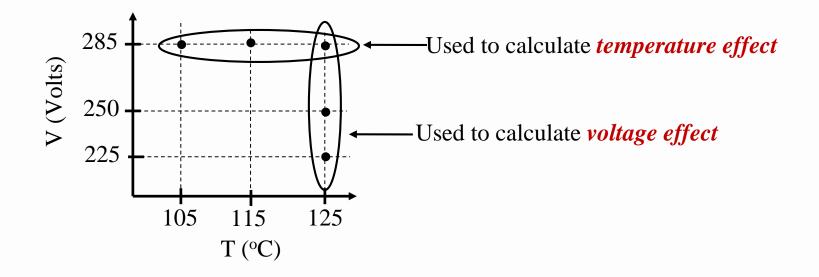
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## **Design of Experiments for Lifetime Modeling**

• Failure terminated highly accelerated life tests (HALT) were conducted at multiple stress levels.





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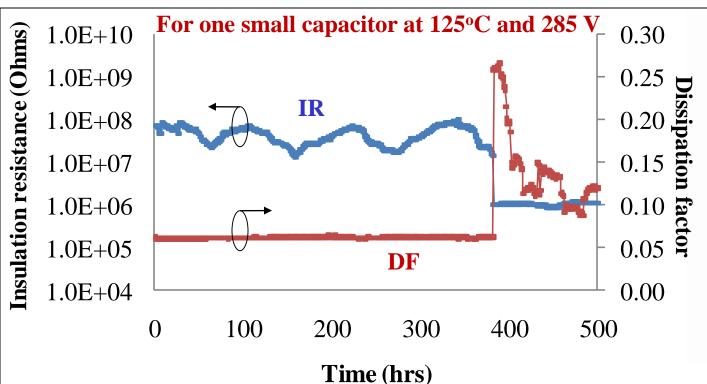
Avalanche breakdown of

the dielectric

## **Failure Modes Observed During Lifetime Testing**

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- The failure modes observed were:
  - Sudden decrease in insulation resistance
  - Sudden increase in dissipation factor
  - Gradual drop in capacitance
- There was no trend in the values of IR or DF before failure.







#### NEW IDEAS ... FOR NEW HORIZONS LAS VEGA Effect of Temperature and Voltage on IR

Prokopowicz<sup>1</sup> proposed a model that is used in accelerated life testing of multilayer ceramic capacitors (MLCCs) to describe IR failures.

The values of n and  $E_a$  for BaTiO<sub>3</sub> in MLCCs can be found in the literature

The values of n and  $E_a$  for epoxy-BaTiO<sub>3</sub> composite had not been documented

where t is the time-to-failure, V is the voltage, n is the voltage exponent,  $E_a$  is the activation energy, k is the Boltzmann constant, T is the temperature, and the subscripts 1 and 2 refer to the two aging conditions.

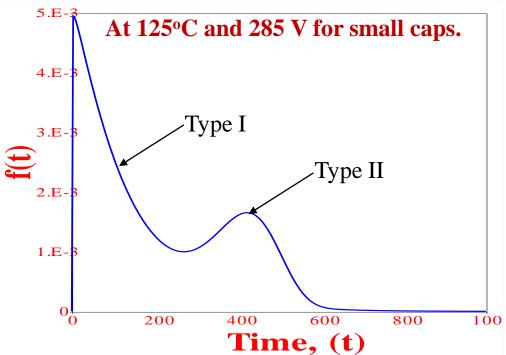
The applicability of this model for an epoxy- $BaTiO_3$  composite dielectric had not previously been established.

<sup>1</sup>T. Prokopowicz and A. Vaskas, Final Report, ECOM-90705-F, pp. 175, NTIS AD-864068, 1969.

 $\frac{\mathbf{t}_1}{\mathbf{t}_2} = \left(\frac{\mathbf{V}_2}{\mathbf{V}_1}\right)^n \exp\left(\frac{\mathbf{E}_a}{\mathbf{k}}\left(\frac{1}{\mathbf{T}_1} - \frac{1}{\mathbf{T}_2}\right)\right)$ 

#### APEX EXPO NEW IDEAS ... FOR NEW HORIZONS Lifetime Modeling of Avalanche Breakdown Failures

- At all stress levels, the time-to-failure was observed to follow a **bimodal distribution**:
  - A mixed Weibull with 2 subpopulation was used to calculate the mean time to failure (MTTF).



- A shorter time-to-failure (all Type I) of large capacitors implies that their failures were defect driven, whose probability increases with capacitor area.
- Statistical analysis was not performed on large capacitors due to small sample size (4).

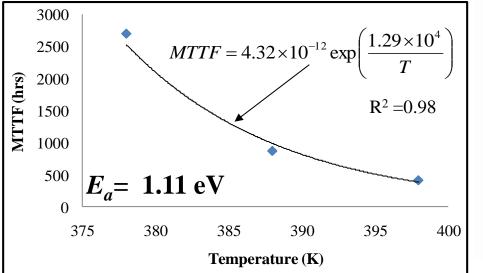


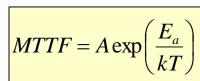
## Activation Energy $(E_a)$ of the Prokopowicz Model

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Type I failures seem to be **random** ( $\beta \sim 1$ ) and Type II represent a **wear-out** mechanism ( $\beta > 1$ ) so only Type II failures were modeled.

	Type I (Random failures)			Type II (Wear-out failures)		
	β	η	MTTF (hrs)	β	η	MTTF (hrs)
125°C and 285V	1.0	130	130	6.0	444	413
115°C and 285V	1.1	65	63	1.8	979	871
105°C and 285V	1.6	267	238	4.9	2937	2702





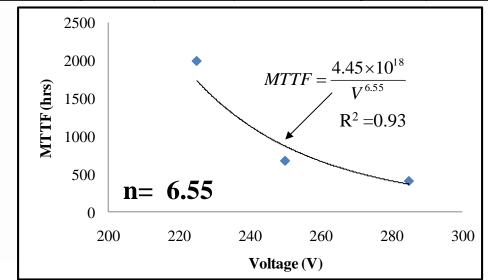


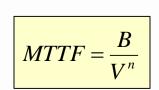
## Voltage Exponent (n) of the Prokopowicz Model

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	Mode I (Random failures)			Mode II (Wear-out failures)		
	β	η	MTTF (hrs)	β	η	MTTF (hrs)
125°C and 285V	1.0	130	130	6.0	444	413
125°C and 250V	1.4	188	171	5.5	739	680
125°C and 225V	1.0	935	935	22.3	2058	1996







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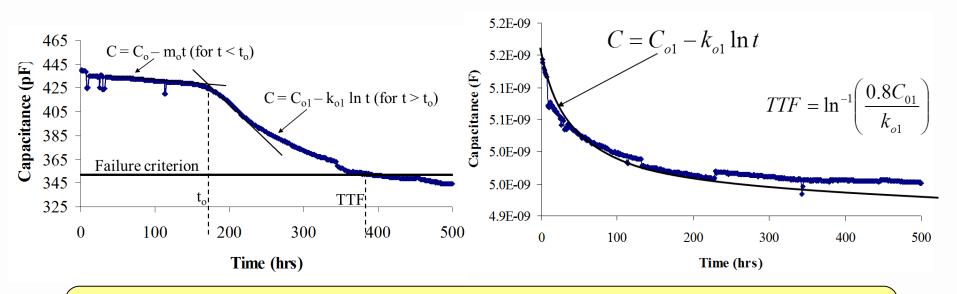
#### NEW IDEAS ... FOR NEW HORIZONS LAS Gradual Decrease in Capacitance

(Plot of Capacitance at 125°C and 285 V for Group B Capacitor)

- In small capacitors (group A) the onset of logarithmic degradation was delayed by a time which is referred to as  $t_o$ .
- The linear degradation region was absent in group B (large) capacitors.

Group A (small)

Group B (large)



Failures were not observed in group B (large) capacitors due to a large value of initial capacitance  $(C_{ol})$  as compared to group A.



#### **NEW IDEAS ... FOR NEW HORIZONS** LAS VED **Effects of Temperature on Capacitance**

An increase in plate spacing as a result of thermo-mechanical stress generated due to CTE mismatch Decrease in the dielectric constant: •Aging in BaTiO<sub>3</sub> •Residual stress relaxation in polymer

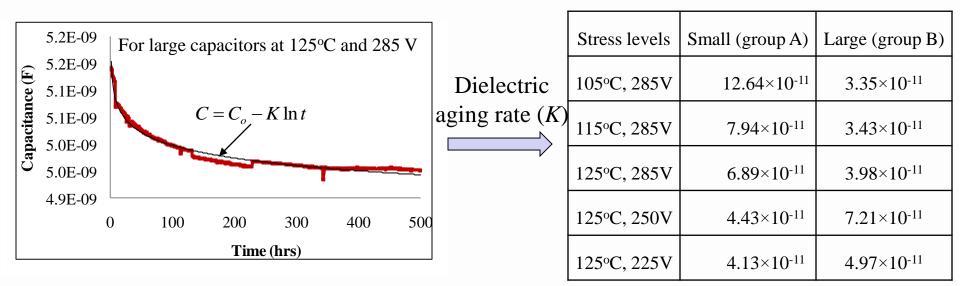
 $C = C_o - k \ln t$   $\Rightarrow$  Aging model

where C is the capacitance at time t,  $C_o$  is the initial capacitance, k is the capacitance degradation rate, and t is time.

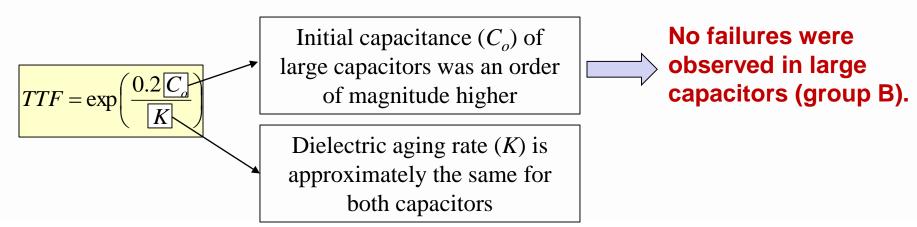


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## **Modeling the Decrease in Capacitance During HALT**



- Time-to-failure as a result of 20% decrease:

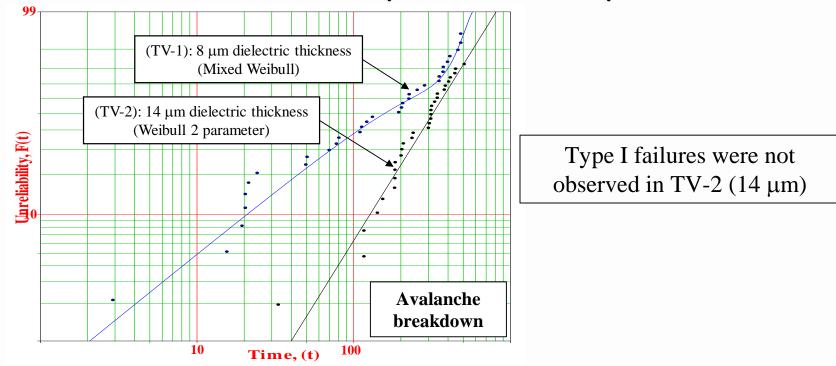




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#### Thickness Effect: 8 μm versus 14 μm



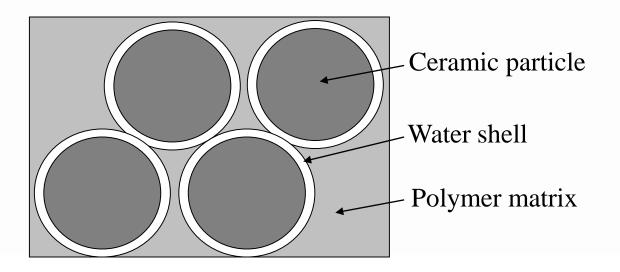
	Avalanche breakdown at 125°C and 285 V						Decrease in
	Туре І				Туј	capacitance	
	β	η	MTTF (hrs)	β	$\eta$	MTTF (hrs)	K
<b>TV-1 (8 μm)</b>	1.0	130	130	6.0	444	413	6.89×10 <sup>-11</sup>
<b>TV-2</b> (14 μm)				2.0	383	341	4.52×10 <sup>-11</sup>



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## **Effect of Humidity**

- Under humid conditions, the *capacitance and DF were found to increase* due to moisture absorption in the dielectric (since  $\varepsilon_{water} > \varepsilon_{air}$ , where  $\varepsilon$  is the dielectric constant).
- The primary site of absorbed moisture in these composites is the *interface* between the ceramic and the polymer matrix.
- The level of moisture absorbed in these composites increases with a decrease in the ceramic particle size or an increase in the ceramic loading, both of which increase the interfacial area.



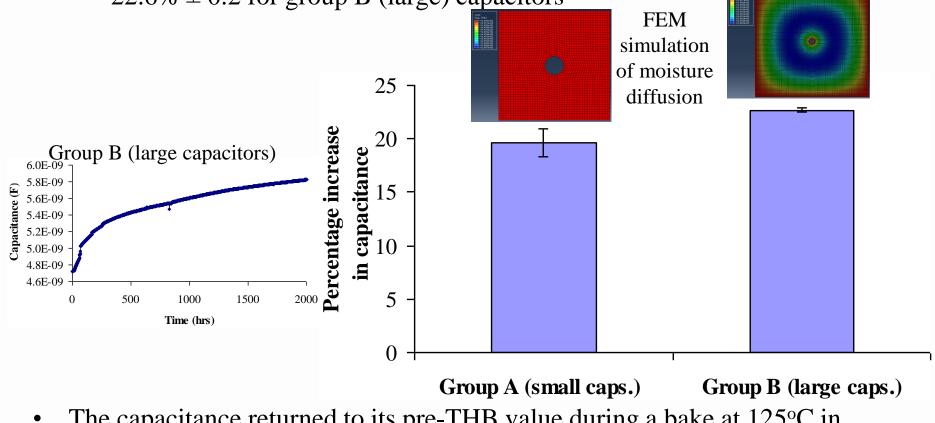


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#### NEW IDEAS ... FOR NEW HORIZONS LAS V Percentage Increase in Capacitance

- The increase in capacitance at 85°C, 85% RH and 0 V after 2000 hrs was
  - $-19.6\% \pm 1.3$  for group A (small) capacitors
  - $-22.6\% \pm 0.2$  for group B (large) capacitors



• The capacitance returned to its pre-THB value during a bake at 125°C in about 20 hrs.

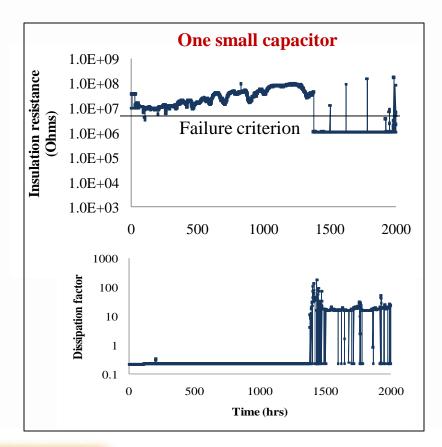


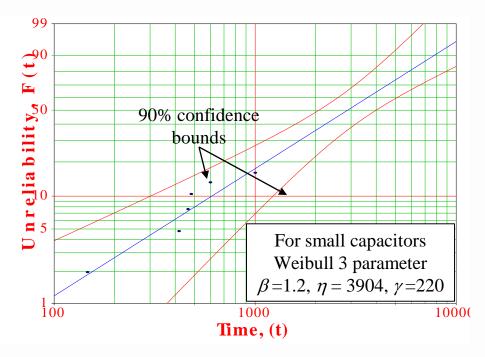
# **Results of Temperature-Humidity-Bias (THB) Tests** (85°C, 85% RH, and 5 V)

IR failures as a result of formation of a conduction path were observed :

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- 6/36 small capacitors and 2/4 large capacitors failed by this mode.





All failures as a result of formation of a conduction path disappeared after baking at 125°C for several days.





## NEW IDEAS ... FOR NEW HORIZONS Outline

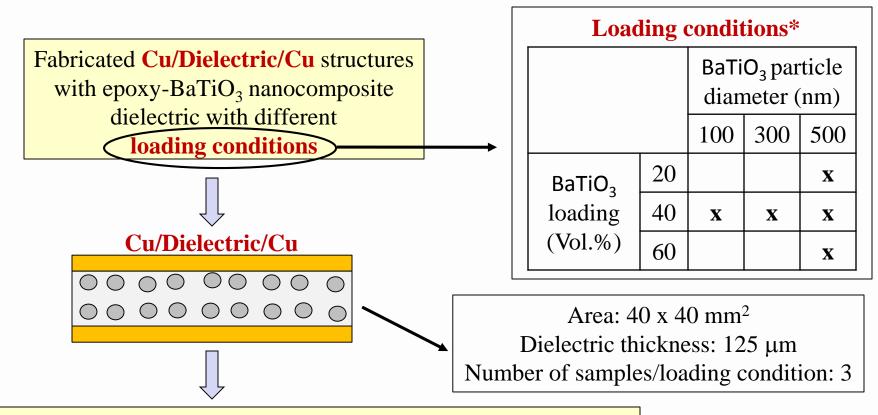
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## Approach



Measured the following parameters:

- 1. Capacitance and dissipation factor (as a function of Temperature)
- 2. Leakage current (as a function of Temperature and Voltage)

\*Three control samples were also fabricated with 0% loading



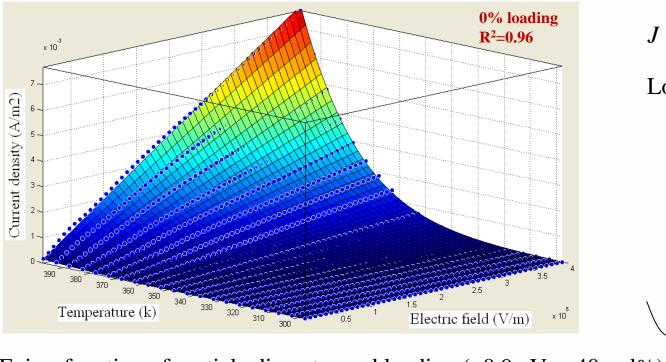
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## **3D Regression of the Leakage Current Data**

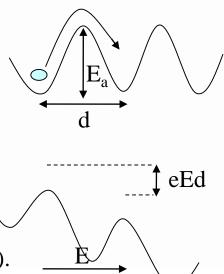
#### (To Calculate the Activation Energy of Ionic Hopping)

- 3D regression was performed on the leakage current data.
- The goodness of fit (*R*<sup>2</sup>) for ionic hopping conduction was greater than 0.90 for all loading conditions, which indicated that hopping was the dominant conduction mechanism (as opposed to Schottky or Poole-Frenkel).



$$J \approx A \left(\frac{E}{T}\right) \exp\left(-\frac{E_a}{kT}\right)$$

Low field approximation



 $E_{\rm a}$  is a function of particle diameter and loading (~0.9 eV, < 40 vol%).



## **Effects of Particle Loading and Diameter**

• The effective dielectric constant was found to increase with the ceramic loading:

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- The maximum dielectric constant was close to 25 at 60% loading (for 500nm particles).
- The effective dielectric constant was found to decrease when the particle diameter was reduced to 100 nm:
  - this may be due to an increase in the agglomeration of ceramic particles.
- Leakage current was found to increase
  - with an increase in the ceramic loading;
  - with an increase in the particle diameter.
- Leakage current was found to increase with temperature at all voltages (between 1 and 50 V) and loading conditions.





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## **Conclusions: Temperature and Voltage Aging**

- Two failure modes observed:
  - 1. Sharp drop in insulation resistance (*IR*): bimodal

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- Mechanism: avalanche breakdown
- Type I (infant mortality): **TTF decreased with capacitor area** (defect driven)
- Type I (infant mortality): risk of failures increased for thinner capacitor
- Type II (wear-out): determined failure statistics (Weibull parameters, MTTF)
- Type II (wear-out): Prokopowicz model is applicable

- Values of constants n = 6.5,  $E_a = 1.1$  eV; material, not size, dependent

- 2. Gradual decrease in capacitance (C)
  - Mechanism: dielectric aging, plus stress relaxation and electrode separation
  - **TTF increased with capacitor area** (governed by relative changes)
  - Logarithmic aging model is applicable for large area capacitors
  - Smaller capacitors have an initial linear aging trend
    - Aging constant  $K = 5 \times 10^{-11}$ ; material, not size, dependent



## **Conclusions: Temperature-Humidity (and Bias)**

- Temperature-Humidity (no bias):
  - Capacitance and DF both increased with time
  - Mechanism: moisture diffusion/adsorption, leading to increase in dielectric constant

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- Diffusion constant was calculated for moisture in epoxy-BaTiO<sub>3</sub> nano-composite film:  $D \approx 1 \times 10^{-11} \text{ m}^2/\text{s}$
- Reversible after bake-out
- Temperature-Humidity-Bias:
  - The failure mode observed was a sharp drop in *IR*
  - DF also increased suddenly at the same time
  - **Mechanism:** moisture diffusion/adsorption followed by conductive path formation (defect-mediated)
  - Reversible after bake-out



## **Conclusions: Leakage Current Mechanism**

• The leakage current was found to be governed by the **ionic hopping mechanism** 

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- The activation energy for ionic hopping was determined
  - E<sub>a</sub> is a function of particle diameter and loading
  - E<sub>a</sub>  $\approx 0.9$  eV, for loadings less than or equal to about 40 vol%
- The leakage current in the dielectric was found to increase
  - with an increase in the ceramic loading
  - with an increase in the particle diameter

### **Recommended Future Work:**

- Further investigate effects of area, thickness, particle loading, and particle diameter
- Assess alternative film constructions and materials
- Investigate the path of leakage current and identify the charge carriers



#### NEW IDEAS ... FOR NEW HORIZONS

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## Questions?

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## Thank You

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