



0.3mm W.L CSP Assembly

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DG1 Debbie Gomez, 7/18/2005



Abstract

 Due to the ever-aggressive miniaturization program that is rolling through the electronics industry, the next component that is fast approaching this horizon is the 0.3mm CSP





Abstract

- This paper will research the key elements that influence the 0.3mm CSP deposition process.
- Process design factors such as solder paste stencil design and substrate will be fully investigated.
- The impact of typical fabrication defects associated to the fabrication of stencils will be observed to ensure that an authentic picture is created and not one that belongs in a laboratory.







Experimental conditions





Experimental conditions

Parameter	Value & Unit
Print Speed with standard blades	50mm/s
Print Pressure with standard blades	4Kg
Separation Speed	2mm
Separation Distance	5mm/s
Squeegee Angle	60 Deg
Tooling	81mm pins
Temp & Humidity	21 Deg C & 40% R.H



Line configuration

- A Dek Galaxy carried out the Solder paste printing
- A Universal GSM carried out the placement of the devices
- A Soltec XPM2 employed to carry out the duties of reflow. The reflow atmosphere was air.



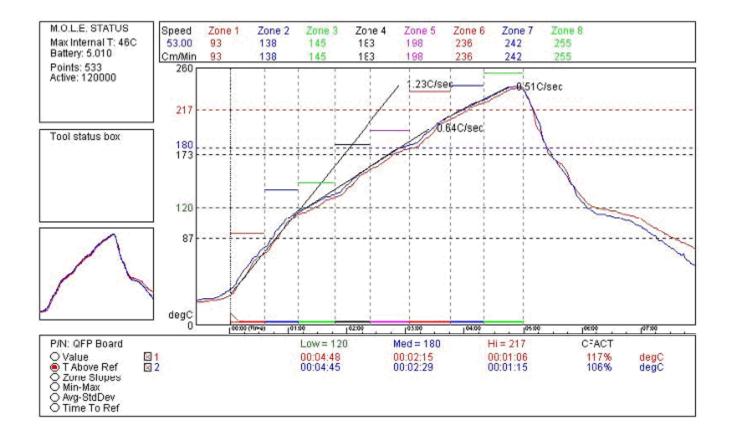
Experimental conditions

- 3 boards were printed on a set-up substrate before each production board was assembled this ensured an optimised condition for the paste as well as lubrication for the stencil apertures
- To further help reduce any statistical noise the print direction for all production boards was set to a forward print stroke.





Reflow - Profile



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Materials - Solder pastes

Paste label	Alloy type	Metal content (% weight)	Particle size
Х	Sn96.5Ag3.0Cu0.5	89	Type 3
Y	Sn96.5Ag3.0Cu0.5	88.75	Type 4

All samples were suspended in a Lead Free no clean flux medium, single supplier and are commercially available.







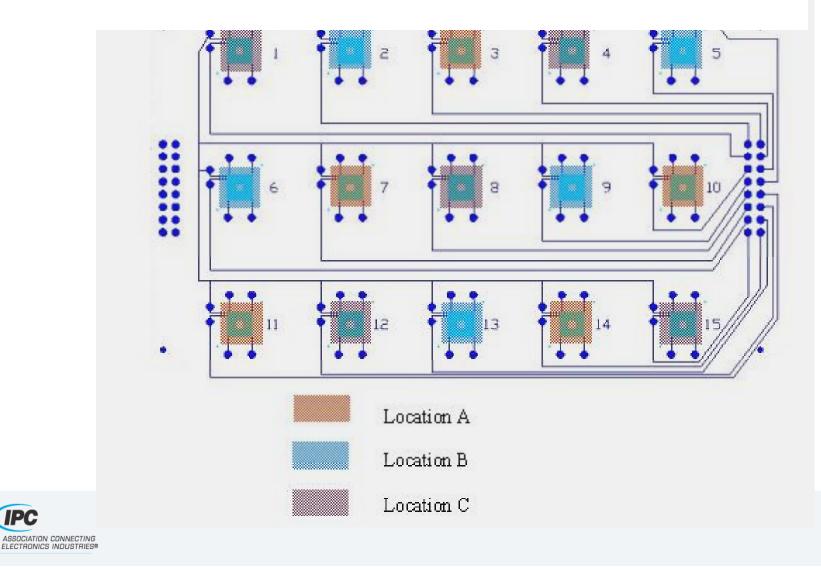
Stencil – Fabrication type

Stencil label	Fabrication method	Metal Thickness	Metal type	Quality
Stencil A	Laser YAG	50 micron	SS 304	High- quality
Stencil B	Laser YAG	75 micron	SS 304	High- quality
Stencil C	Laser YAG	75 micron	SS 304	Inferior
Stencil D	E-Form	66 micron	Ni	High- quality





Stencil- Design Locations







Stencil – Aperture Size

Stencil label	Location A	Location B	Location C	Thickness
Stencil A	125	140	155	50 microns
Stencil B	170	180	190	75 microns
Stencil C	190	200	210	75 microns
Stencil D	170	180	190	66 microns







Stencil – Area Ratio's

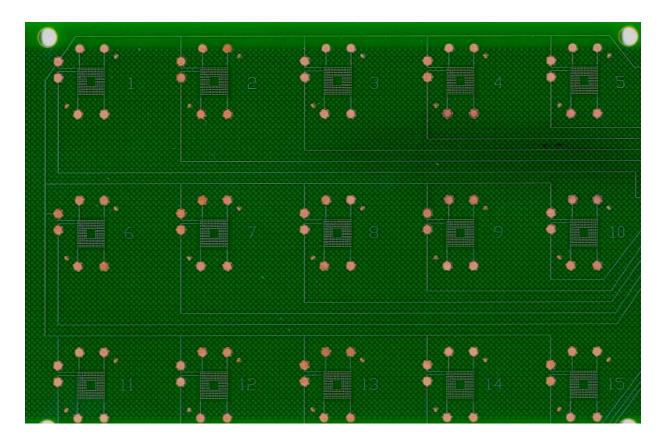
Stencil label	Location A	Location B	Location C	Thickness
Stencil A	0.63	0.70	0.78	50 microns
Stencil B	0.57	0.60	0.63	75 microns
Stencil C	0.63	0.67	0.70	75 microns
Stencil D	0.64	0.68	0.72	66 microns



Ref - IPC 7525



Circuit Board



Board construction = FR4,0.9mm thick & Multi-layer



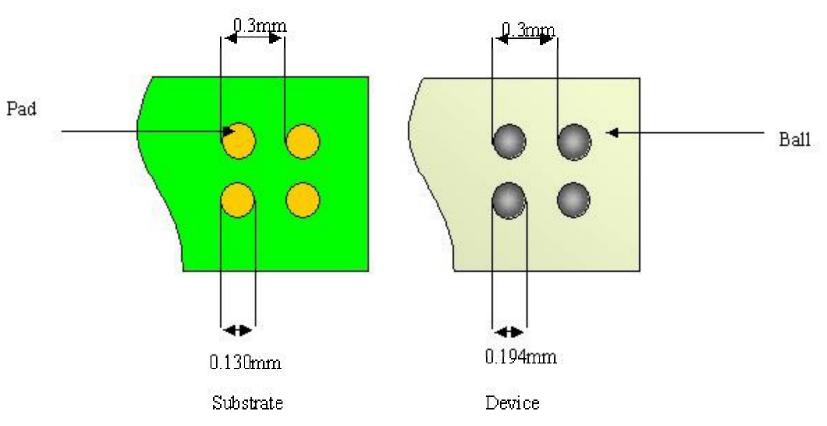


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Board & Component Dim's

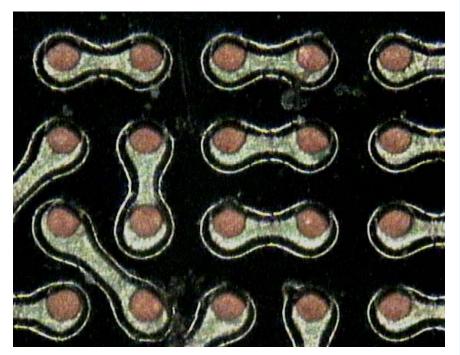


The board design incorporated a daisy chain function for all 15 locations therefore electrical integrity could be carried out during the analyses. The 0.3mm CSP has 264 IO



Issues with substrate fabrication

- Random solder resist mis-registration
- Will this cause assembly issues ?









Analysis





Continuity testing results

Paste Type	Stencil	% of Location A fails	% of Location B fails	% of Location C fails
3	А	100.00%	0.00%	0.00%
	В	60.00%	20.00%	0.00%
	С	75.00%	20.00%	40.00%
	D	20.00%	0.00%	0.00%

64

Paste Type	Stencil	% of Location A fails	% of Location B fails	% of Location C fails
4	А	40.00%	0.00%	0.00%
	В	0.00%	0.00%	0.00%
	С	0.00%	20.00%	0.00%
	D	20.00%	0.00%	0.00%

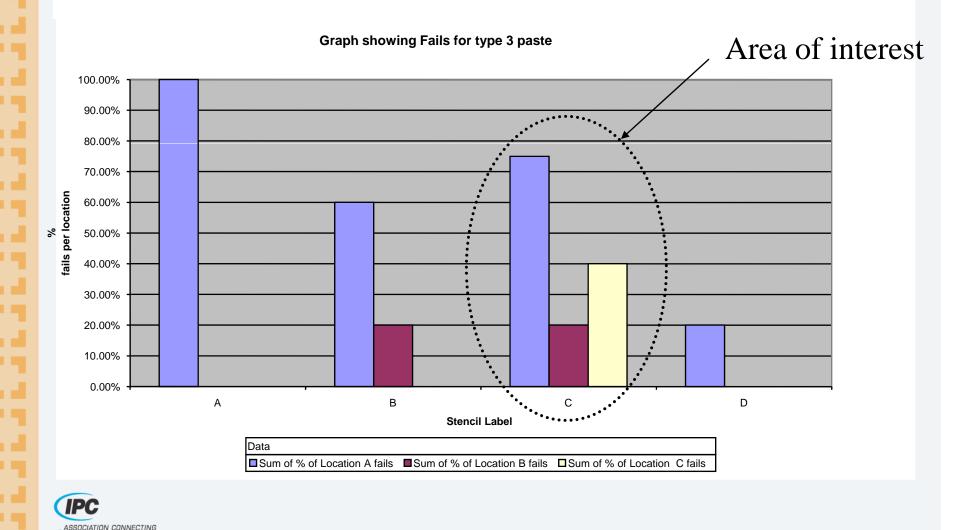
100% = All 5 locations failed





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Continuity testing - Type 3



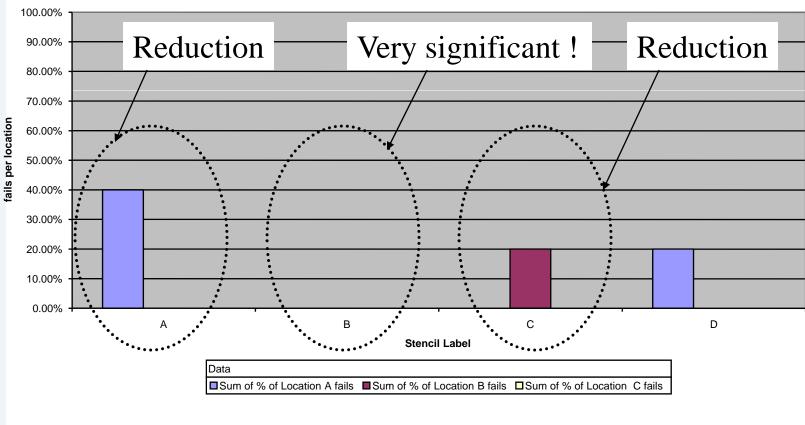


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Continuity testing - Type 4

Graph showing Fails for type 4 paste



Type 4 = reduced number of failed interconnects





Die penetration – IPC 7095A



Example of a dye penetration (Board 1site 10)



Die penetration results

	Sum of Failed Interconnects	Sum of Failed Interconnects
Stencil	Туре 3	Type 4
Α	33	19
В	26	0
С	64	3
D	3	1





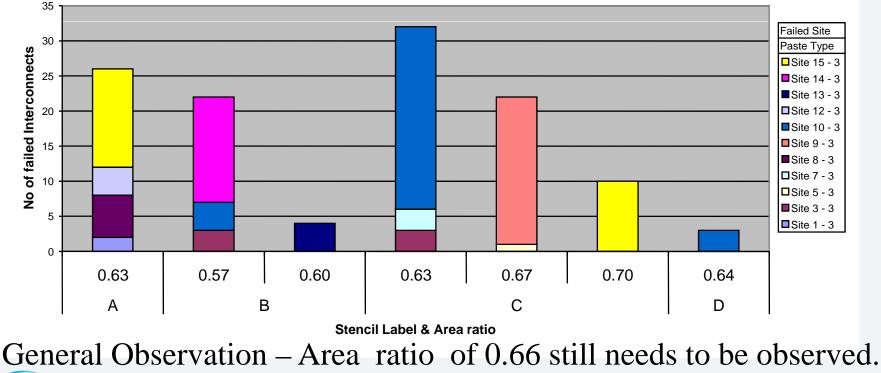
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No. of failed interconnects Versus Area Ratio – Type 3

Graph showing the number of failed interconnects versus Stencil and area ratio Type 3 Solder paste



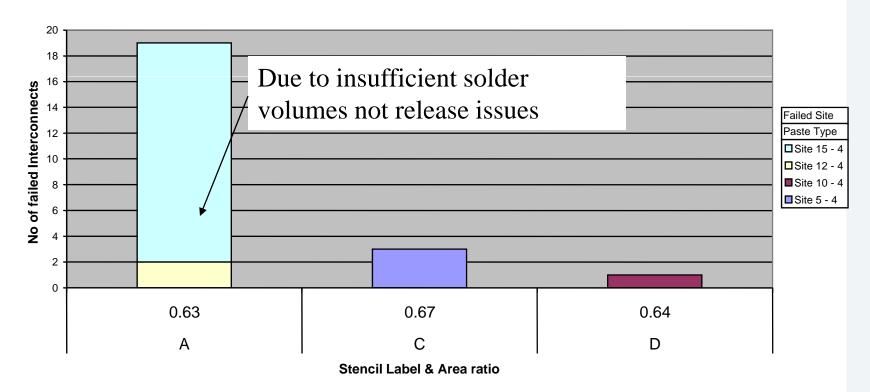
Stencil C shows poor quality = poor results



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No. of failed interconnects Versus Area ratio – Type 4

Graph showing the number of failed interconnects versus Stencil and area ratio Type 4 Solder paste

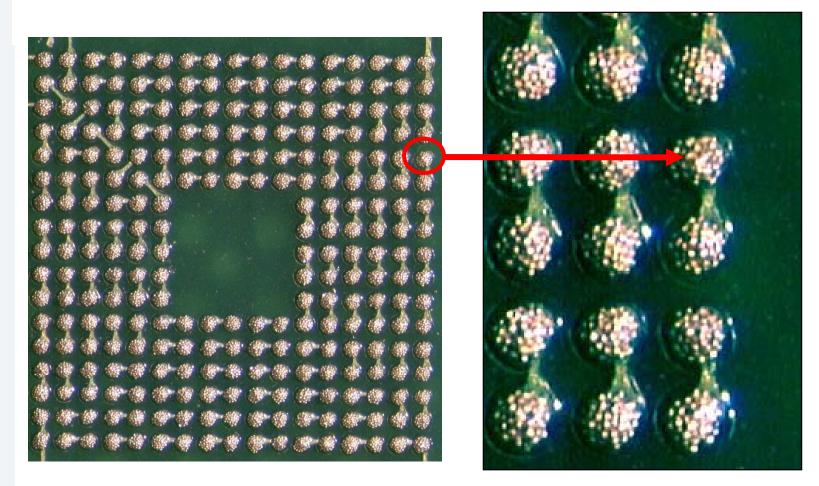


General Observation –Stencil B shows no Fails Type 4 shows that stencil quality is not as significant





FMEA

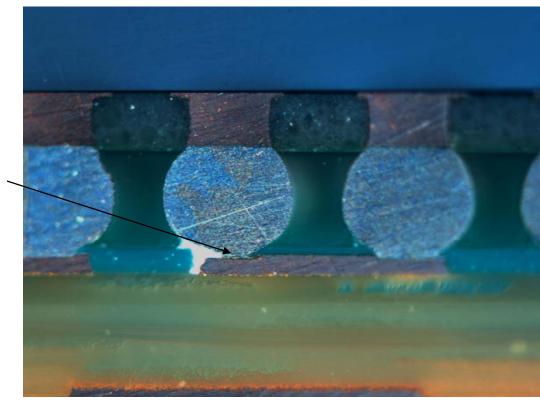


Photograph of a failed interconnect, Stencil C Type 3 site 14 (AR 0.63)





FMEA



Photograph of a failed interconnect, Stencil C Type 3 site 14 (AR 0.63)

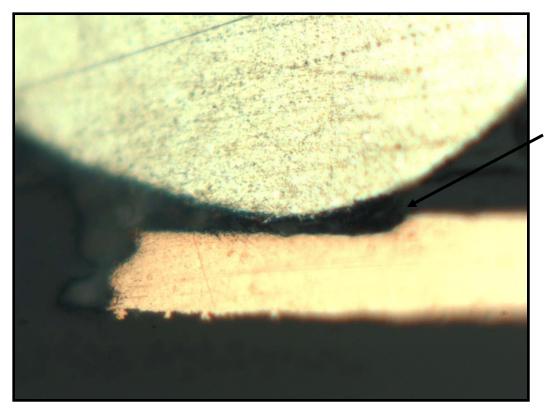
Insufficient

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Remember the mis - registration?

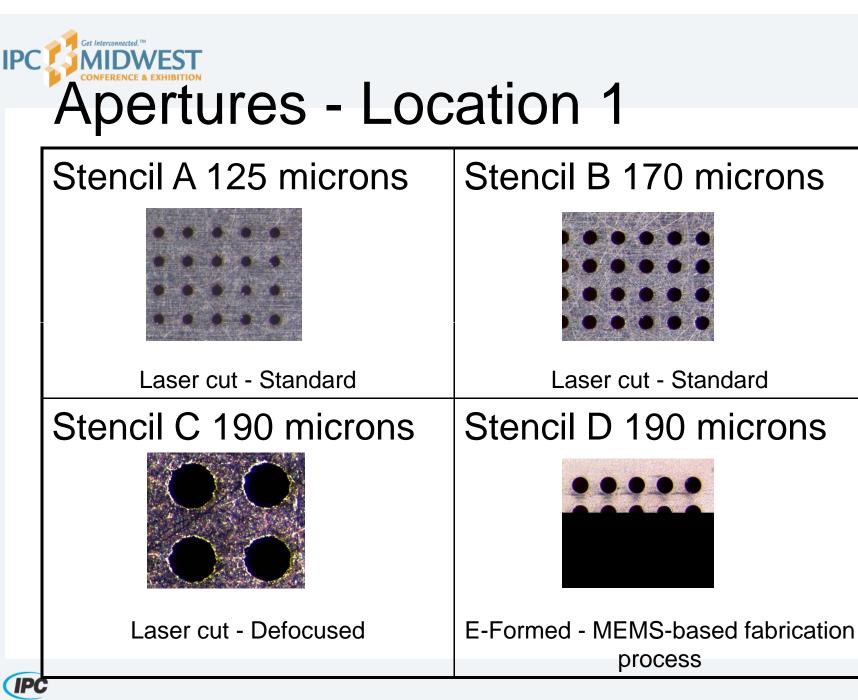


Mis-registered Solder Mask

Combination of solder mask mis registration and low solder volume, causing failed interconnect







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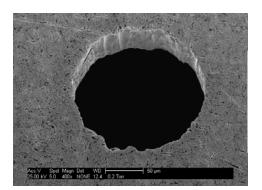
FMEA – Stencil C & D

Irregular edge-



REAL Sum Magn (M) 02 02 000 02 000

Stencil C

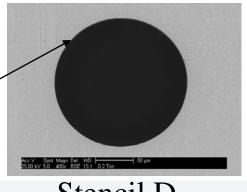


Stencil C

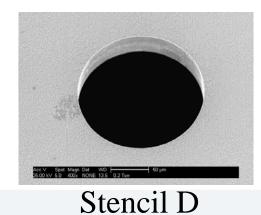
Smooth side wall

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Stencil D





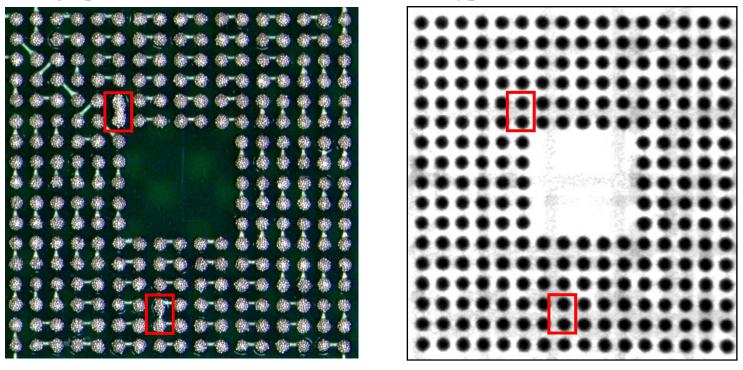
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X-Ray

Photograph of a failed interconnect, Stencil C Type 3 site 3 (210 micron)



The solder paste bridge did not manifest itself into a post reflow solder bridge





Summary



a)

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If you really want to use Type 3

50-micron mask thickness and aperture diameters in the ballpark of 180 microns (this figure has been concluded from the results gained from Stencil B).

However the 50 micron mask thickness this would undoubtedly cause insufficient volumes issues with other technology types, thus not complying with heterogeneous assembly requirements.

b) A thicker material (75 microns) would be required but the aperture diameters would need to be greater than 200 microns. These aperture sizes could possible lead to solder paste bridging and coining in the Laser stencil fabrication process.

Both these options are not lending themselves to a high volume assembly.





Sensible set-up

- Type 4 solder paste
- 75 micron thick stencil
- High quality Laser cut stencil or Electro Formed
- Aperture diameters ranging from 170-190 microns







Thank you for your attention

Questions?

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