

Cleaning a No-Clean Flux on Contaminated Hardware as a Recovery Plan

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Abstract

There is a growing problem in the industry with no-clean flux technology and the after effects it can have on reliability. If the fluxes are not fully complexed (not fully heat activated) there can be a number of failure mechanisms attributed directly to the flux. There is a tendency for the flux to become entrapped under low standoff parts and parts with very tight spacing if you have dirty incoming bare boards or components. The problem then becomes how to clean and recover the product to acceptable functioning hardware after time has passed. The flux becomes harder and harder to remove but the partially heat activated flux residue does not become less moisture absorbing over time.

In this presentation we will show the effectiveness and timing issues on cleaning hardware that has been assembled with a no-clean flux that has a corrosive contamination problem. Potential issues include: high chloride residues from bare boards (HASL), partially activated flux residues, and localized cleaning that has created a trapped surface residue causing corrosive or leakage problems. This recovery plan outlines the material and hardware assessment for water intolerant or material compatibility issues. Mission critical hardware contaminated by process and assembly chemicals can be cleaned effectively when using a combination of cleaning energies, such as, low pressure, high volume, saponified chemical wash followed by a steam cleaning and DI water rinsing. We will show that a no-clean flux can be cleaned and the product brought back to levels of acceptable functioning hardware.

Introduction

No-clean fluxes are formulated with very low solid contents, normally 1%-5%, intended to not be cleaned after a soldering process since any residues are supposed to be inert. Eliminating the post soldering wash process can be a real time saver, not to mention the money saved on equipment, manpower and consumables used in the process. One small, or not so small, problem with the term no-clean flux is you may still have to clean it. Many assembly houses have learned this the hard way with failures at bench level testing, field returns or even cosmetically the way the customer needs. After the problem of uncomplexed no-clean residues has been identified the question is how to remove the corrosive/conductive residues.

The visual element of a corrosive no-clean residue effect is pictured in Figure 1. This particular result was caused by hand solder of a thru-hole component that did not fully complex. When the assembly was powered up in a humid environment the residue caused dendrites in a short period of time with failure soon to follow.

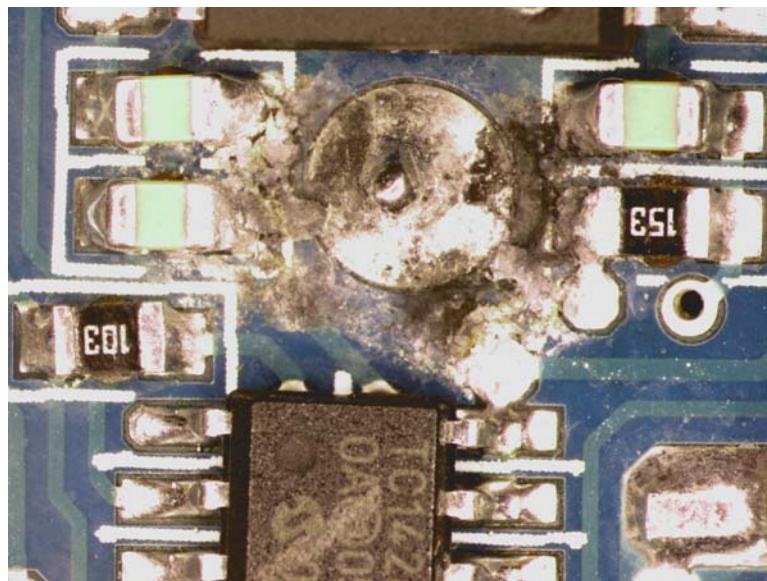


Figure 1

This presentation will outline several different cleaning processes on PCB's exposed to a no-clean flux that is not fully complexed. The first examples are from field return and warehoused power supplies that were found to have non-complexed no-clean flux. Some of the questionable units were failures that could be recovered after a specific cleaning process and some were found to be beyond recoverable due to the residues and hard failures they caused. The second set of PCB's were built and treated with no-clean flux and then cleaned in one of three processes. The first was DI water only, in the second process heated saponifier was added and finally a steaming step for the third process.

Discussion of Methodology (Ion Chromatography and Surface Insulation Resistance)

Ion Chromatography

This evaluation used Ion Chromatography per IPC-TM-650, method 2.3.28 to characterize process residues. The test samples were extracted with a localized extraction system to isolate a 0.1 in² area. All testing was performed on a Dionex ICS 2000 ion chromatography system using Chromeleon software Controls and blanks were performed on the Dionex ICS 2000 ion chromatography system before the test began. *NOTE: Foresite used NIST-traceable standards for all system calibrations.*

A 1.5mL sample of each test samples' extracted solution was analyzed using a 1.7mM sodium bicarbonate/1.8mM sodium carbonate eluent using the AS4A-SC column and all results were reported in µg/in² to allow for the extraction volume and surface area.

SIR Testing of the Umpire Test Assemblies

All of the Umpire boards were handled using ionically clean gloves. And, all boards were handled only by the edges. The SIR data acquisition system had a nominal 1 megohm resistor (1.0 E 6) in each circuit pathway. The one megohm value is relatively common in the SIR test field. These current-limiting resistors serve two primary purposes: To preserve dendritic formations that grow during the test, and to protect the data acquisition system from large current spikes. The test boards were placed – in randomized order – onto a circuit board rack and fixed in place with Teflon coated wire. The loaded racks were placed into separate SIR Chambers sequentially. The racks and the test boards occupied approximately 35 - 40% of the chamber workspace and did not block the flow of air over the control sensors. This was an important element allowing the chamber to keep tighter control over the test environment, avoiding condensation from inadequate air flow. A bias connection of 50v DC was applied to each test specimen.

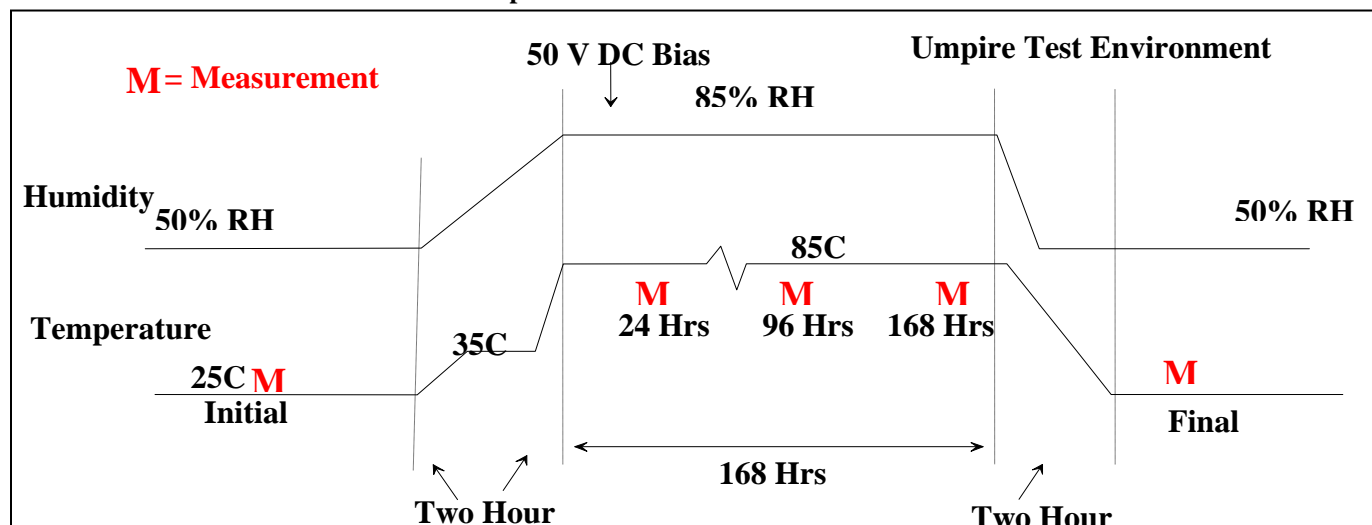
Measurements

Measurements were made with test specimens in the chamber under the test conditions of temperature and humidity at 24, 96 and 168 hours. When taking these measurements, the 45 - 50v DC bias voltage source was removed from the test specimen and a test voltage of -100v. DC was applied.

Evaluation

1. Each comb pattern on each test specimen was evaluated by the insulation resistance values obtained at 96 and 168 hours. If the control coupon readings were less than 1000 megohms, a new set of test coupons were obtained and the entire test repeated. The reading at 24 hours could fall below the required value provided that it recovers by 96 hours. Graph 1 illustrates the cycle for temperature, relative humidity, and measurements. At the 96 and 168 hour measurement points we are looking for values greater than 1.0e8 ohms or resistance.

Graph 1 - SIR Environment 168 hours



Study 1: Warehoused and Field Returns

Fifty industrial power units were supplied for the study and were a mix of field returns (14 units-intermittent failures) and units warehoused for more than 6 months (36 suspect units). These boards were processed with no-clean bottom side SMT and hand soldered thru-hole. The hand solder areas were cleaned with a brush and a chlorinated solvent. These particular PCB's have a large heat sink that easily became faded with exposure to any sort of saponifier and was unacceptable to the end customer. This meant that conventional methods of cleaning were immediately eliminated. The cleaning plan became to take the boards and, instead of sending them through the in-line wash section, soaking them to just below the level of the heat sink in a small heated stainless steel tank that contained 10% saponifier for two minutes. Then we used steam energy to push the saponifier under the components and in between the leads to remove the no-clean residues. Since the problems resulting from the residues were contained to the bottom side of the board, we were able to concentrate the cleaning to one side and not expose the heat sink to any saponifier. After steaming, the unit went through the normal DI rinse and air knife procedure. An oven bake for one hour at 85°C was added to ensure complete drying. Figure 2 shows the two main areas of concern affected by the residues before cleaning and Figure 3 shows the same two areas after cleaning. Ion chromatography testing was performed before and after cleaning on problem areas of each board using a spot extraction method. Tables 1 and 2 show IC results from some of the worst case areas and Sample # 27 shows both areas of concern before and after wash.

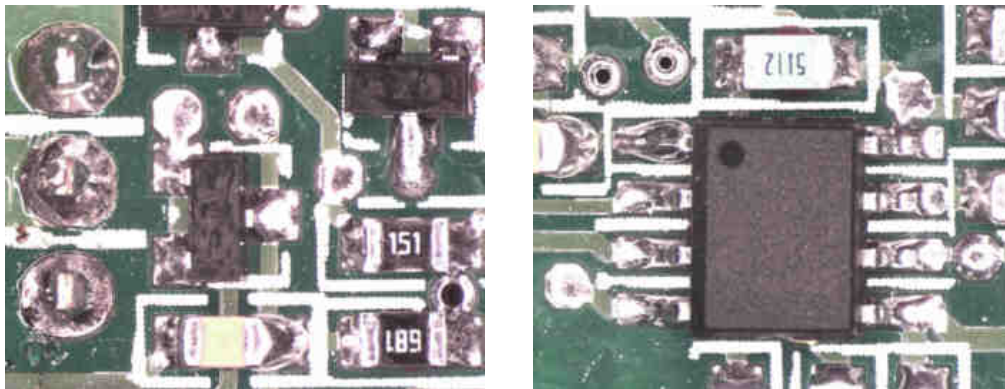


Figure 2 – Sample # 27 Areas of concern 1 and 2 before washing

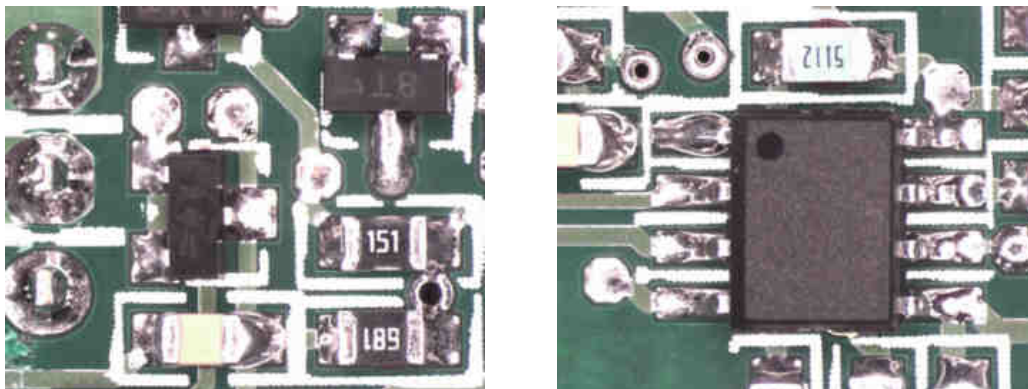


Figure 3 – Sample # 27 Areas of concern 1 and 2 after washing

Table 1 - Ion Chromatography Before Cleaning Results

Condition	Sample Description	Cl ⁻	NO ₂ ⁻	Br ⁻	NO ₃ ⁻	WOA
Before Clean	Sample # 2 area 1	5.07	0	18.32	0.64	83.94
Before Clean	Sample # 6 area 1	5.45	0	2.97	0.64	29.41
Before Clean	Sample # 11 area 1	5.37	0	1.17	0.3	20.74
Before Clean	Sample # 15 area 1	6.11	0	13.08	1.64	114.58
Before Clean	Sample # 27 area 1	13.5	0	15.42	0.3	97.29
Before Clean	Sample # 29 area 1	5.1	0	4.35	0.84	34.23
Before Clean	Sample # 34 area 1	5.1	0	12.96	1.02	75.88
Before Clean	Sample # 39 area 1	7.98	0	10.63	1.24	63.61
Before Clean	Sample # 41 area 1	14.66	0	10.95	1.25	61.21
Before Clean	Sample # 48 area 1	8.62	0	8.44	2.86	135.97
Before Clean	MEAN	7.16	0.00	9.64	1.20	67.89
Before Clean	Standard Deviation	2.98	0.00	5.40	0.72	36.68

Table 2 - Ion Chromatography After Cleaning Results

Condition	Sample Description	Cl ⁻	NO ₂ ⁻	Br ⁻	NO ₃ ⁻	WOA
After Clean	Sample # 2 area 2	2.25	0.05	1.43	0.21	10.98
After Clean	Sample # 6 area 2	0.88	0.00	1.02	0.27	16.66
After Clean	Sample # 11 area 2	0.47	0.00	0.61	0.15	12.65
After Clean	Sample # 15 area 2	0.41	0.00	0.78	0.13	10.65
After Clean	Sample # 27 area 2	1.08	0.00	1.16	0.07	10.45
After Clean	Sample # 29 area 2	1.32	0.00	0.69	0.28	11.08
After Clean	Sample # 34 area 2	1.00	0.00	1.85	0.14	14.43
After Clean	Sample # 39 area 2	2.44	0.11	1.57	0.28	10.83
After Clean	Sample # 41 area 2	1.44	0.05	1.41	0.18	10.23
After Clean	Sample # 48 area 2	1.35	0.08	1.81	0.23	12.47
After Clean	Mean	1.29	0.03	1.20	0.20	12.21
After Clean	Standard Deviation	0.66	0.04	0.47	0.07	2.00

Data Analysis

The IC results show that the units have been recovered to a level of acceptable hardware and pose a minimal risk of electrochemical migration. The boards also improved visually with shiny solder joints, less process residues, etc. These units were then placed back into environmental chamber testing and 49 of the 50 units were totally functional, the one exception was a unit that had a burnt SOT and not even the best cleaning process can fix that.

Study 2: Laboratory Controlled Assemblies

The second part of this study used Umpire boards built by Foresite using both thru-hole and surface mount parts. They were standard FR-4, immersion silver boards using an industry available water soluble paste for SMT components. The boards were then cleaned at Foresite so they all had the same starting baseline cleanliness. Next, the boards were processed with liquid no-clean flux. Then the boards were divided into three different cleaning process groups. The first was DI wash only. Boards were ran through an in-line cleaner at 2 FPM, 40 PSI (top and bottom) and DI wash at 85°F. The second process was the same as the first; however a saponified wash step was added. An industry available saponifier was used at 10% and 150°F. The third process was the same as the first two, with steam between the wash and rinse steps added. The steam is a constant 190 PSI and each component was exposed to steam by an experienced operator. The steam was “pushed” under each component from an angle, close to the board surface ensuring that the saponifier was working under the part. Figure 4 shows the Umpire board used in this experiment, the right portion of the Umpire shows the break off coupon that includes the 68 pin

LCC for IC testing. Figures 5, 6, and 7 shows the Umpire boards TQFP area under magnification with the different processes after the cleaning. The IC and SIR data in table 3 shows the results after the various cleaning processes.

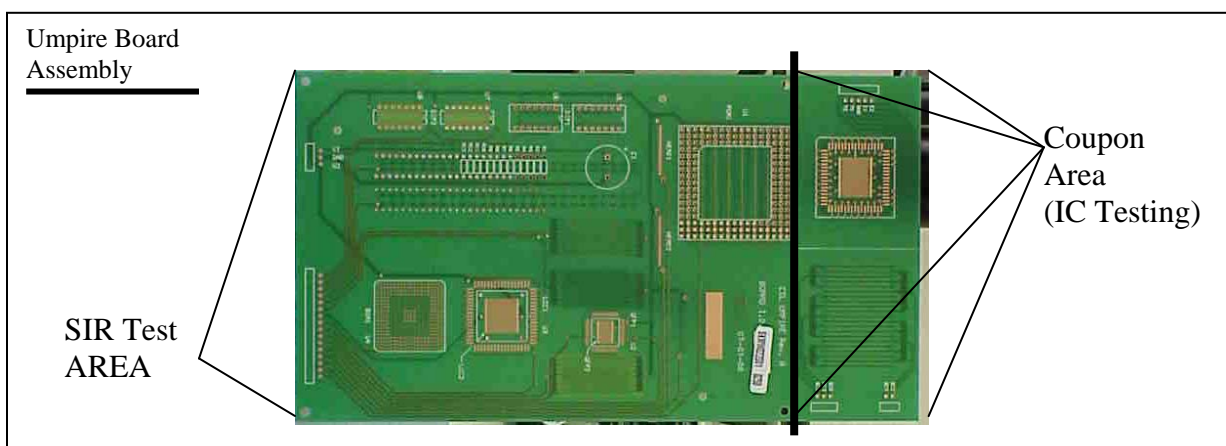


Figure 4 - Umpire Board with Break Off IC Coupon

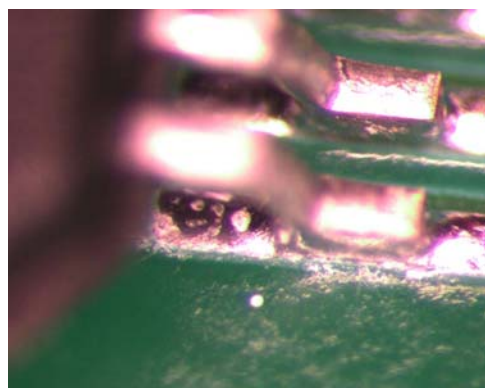


Figure 5 - DI Only

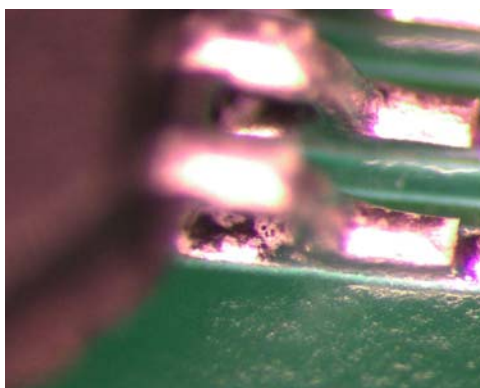


Figure - 6 DI and Saponifier

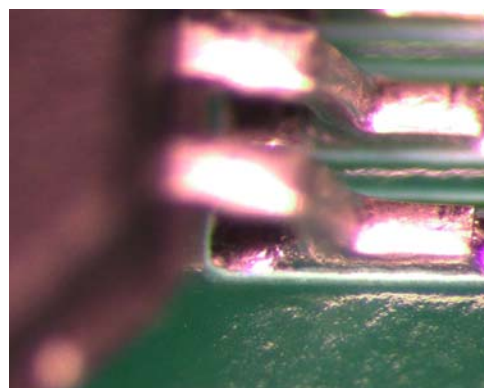


Figure - 7 DI-SAP-Steam

Table 3 - Ion Chromatography and SIR After Cleaning Results

	Ion Chromatography				SIR Testing of the 68pin LCC at 85C/85%RH					
Sample Description	Cl ⁻	Br ⁻	WOA	NH4 ⁺	Initial	24 hrs	96 hrs	168 hrs	Final	Results
5 Sample Set										
Bare Panel - Mean	0.85	0.33	1.57	0.98	1.51 e12	5.21E+10	4.14E+09	3.12E+10	1.36E+12	Pass
Bare Panel - Std Dev	0.1	0.06	0.28	0.35						
15 Sample Set										
DI Wash Only - Mean	0.4	0.28	175.41	2.03	2.64E+12	3.98E+07	1.22E+06	1.00E+06	1.00E+06	Failed
DI Wash Only - Std Dev	0.07	0.05	2.82	0.32						
15 Sample Set										
DI -SAP Wash - Mean	0.44	0.35	49.07	5.36	1.04E+11	4.14E+07	3.24E+07	1.00E+06	1.00E+06	Failed
DI -SAP Wash - Std Dev	0.06	0.03	2.37	0.46						
15 Sample Set										
DI-SAP-Steam - Mean	0.32	0.18	38.59	1.08	4.27E+12	3.25E+09	5.22E+09	2.94E+10	4.85E+12	Pass
DI-SAP-Steam - Std Dev	0.31	0.15	69.65	2.14						

Data Analysis

The IC testing was performed on a built in break off coupon, shown in figure 4, designed just for the purpose of qualifying a build process. J-STD-001C Appendix B, B-3 calls for qualification testing to be performed on circuitry similar to the IPC-B-36, in this case we used a 68 pin LCC. The pass/fail criteria for SIR results are any readings that are less than 1000 megohms at 96 and 168 hours, per IPC-TM-650 2.6.3.3a, 5.5.1. The IC and SIR results logically show that the more cleaning energy applied to the boards the better the results. The group of DI water wash only shows that the opportunity for dendritic growth or leakage path was very high and the SIR 96 hour numbers for the same group showed hard failures. The same can be said for the group with DI and saponified wash, with some improvement but failures just the same. The third group shows passing levels on both IC and SIR results. Groups 1 and 2 did not have sufficient energy to penetrate the tight spacing between leads or package body and board surface. The no-clean flux creates a dam of sorts between leads and even with heated saponified wash there isn't enough contact time to break down the flux and flow under the parts where the most detrimental of the residues can be hidden and given the proper environment cause problems such as no trouble found failures and intermittent shorts. Unless you physically remove the parts to get a better look at the residues under the package body, you may not really know what is going on since to the naked eye and even under a microscope the boards may look clean between the leads.

Conclusions

Looking at both of these studies the end result is that for no-clean flux that is left on an assembly and not fully complexed, it is just a matter of time and opportunity before an issue occurs. It may be an issue of a large scale recall or a handful of no trouble found returns, there are a lot of variables at play like with most aspects of the PCB build process. The short resolution to this issue is to make sure that the flux is fully complexed whether you are looking at an issue due to the entire build process or if it is isolated to just hand solder or rework. Production houses have to do the due diligence of reflow and wave solder profiling, cleanliness monitoring and overall education of workers who have even the smallest responsibility of producing a quality product. When cleaning a no clean flux it is important to remove the flux from wave solder, surface mount soldering, localized cleaning residues and bare board / component fabrication residues. These residues, depending on their location, need different energy forms to remove the residues when rescue cleaning. Wash water needs to be heated to 150°F for good ionization of the flux residues and requires a saponifier to lower the surface tension and solubilize residues trapped below the SMT components. Low pressure, high flood sprays in the wash section allow a lot of chemistry to get to the entire surface and below component areas. The amount of energy required for removing a no clean flux has included the use of DI water steam for SMT flux removal in and around the pad surface. This followed by a DI water medium pressure rinse has proven to be the most effect process and can clean thousands of assemblies or become a standard process. Removal of flux residues that were not designed to be cleaned is not easily done with water only and requires tools like Ion Chromatography with localized extractions and SIR on test coupons that show the electrical effect on the residues in high humidity.



FORESITE

Cleaning a No-Clean Flux on Contaminated Hardware as a Recovery Plan

Presented by Eric Camden
Foresite



No-Clean Flux Issues

Topics

- Uncomplexed no-clean flux and the various root causes
- Detrimental effects on finished assemblies
- Field returns vs. warehoused assemblies with partially active no-clean flux residues
- Lab created contaminated samples
- Ion chromatography and SIR data on contaminated boards
- Cleaning methods
- Results and overview



Reasons for choosing a no-clean

- Eliminating the cost of cleaning machinery and the staff that goes along with cleaning. As well as the cost of saponifiers and manufacturing DI water.
- Improving through put numbers.
- A fully activated no-clean flux will leave a benign and insulative layer of protection against various levels of moisture and humidity.
- Customer imposed

Reasons to not choose a no-clean flux

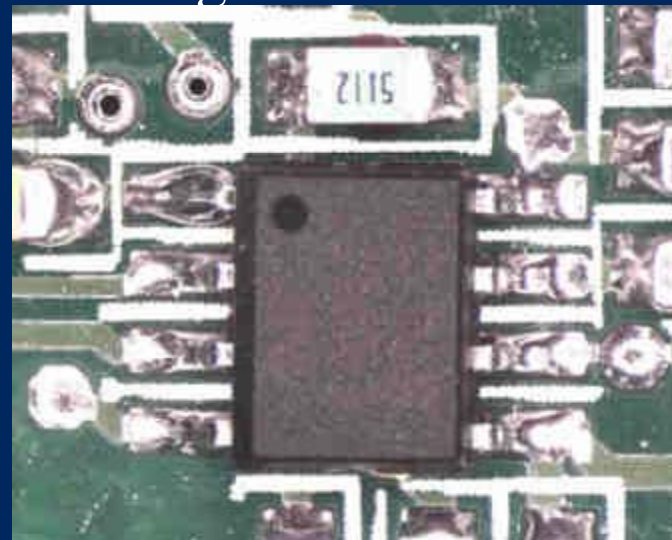
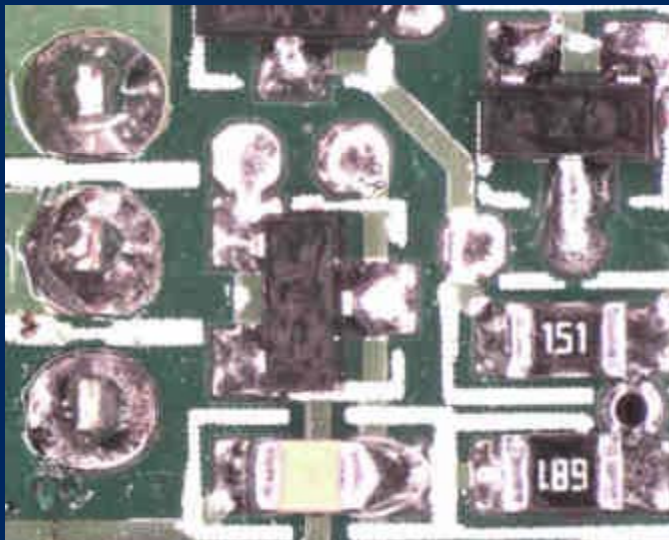




Field Returns and Warehoused Units

50 industrial power units were the subject of the first part of the study with 14 units exhibiting some level of intermittent failures and the remaining 36 suspect units being warehoused for over 6 months. IC testing was performed before and after cleaning.

Before Cleaning





Ion Chromatography Before Cleaning

Condition	Sample Description	Cl ⁻	NO ₂ ⁻	Br ⁻	NO ₃ ⁻	WOA
Before Clean	Sample # 2 area 1	5.07	0	18.32	0.64	83.94
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Before Clean	Sample # 11 area 1	5.37	0	1.17	0.3	20.74
Before Clean	Sample # 15 area 1	6.11	0	13.08	1.64	114.58
Before Clean	Sample # 27 area 1	13.5	0	15.42	0.3	97.29
Before Clean	Sample # 29 area 1	5.1	0	4.35	0.84	34.23
Before Clean	Sample # 34 area 1	5.1	0	12.96	1.02	75.88
Before Clean	Sample # 39 area 1	7.98	0	10.63	1.24	63.61
Before Clean	Sample # 41 area 1	14.66	0	10.95	1.25	61.21
Before Clean	Sample # 48 area 1	8.62	0	8.44	2.86	135.97
Before Clean	MEAN	7.16	0	9.64	1.2	67.89
Before Clean	Standard Deviation	2.98	0	5.4	0.72	36.68



Cleaning Procedure

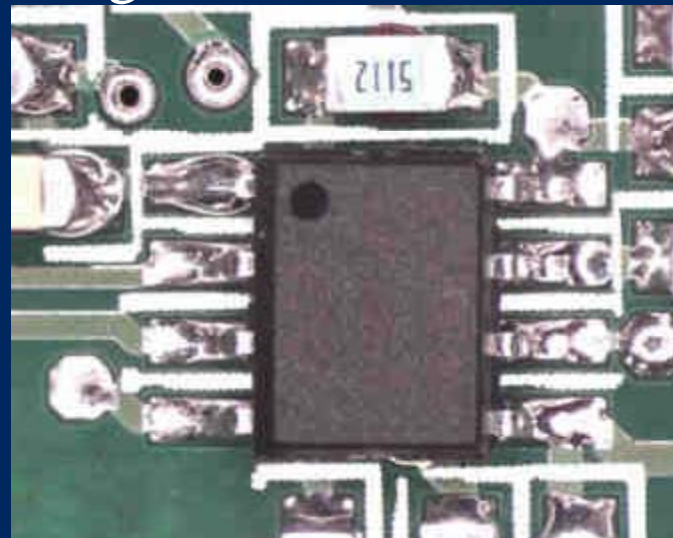
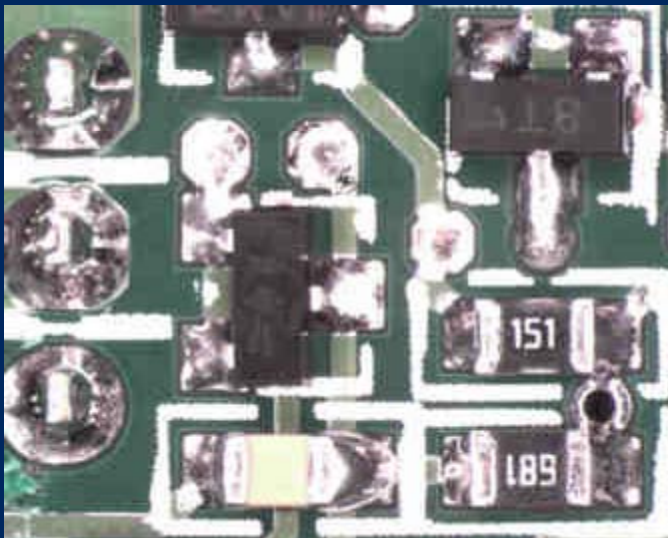
- These boards have a saponifier intolerant part on them so that ruled out conventional cleaning methods
- Boards were soaked just over the topside in 10% saponifier for two minutes at 150°F
- The boards were then cleaned with a COTS steaming unit that provided a constant 190 psi of pressure



Cleaning Procedure

- Boards were then put through an in-line cleaner DI rinse water sections and through the air knives
- The boards were then placed into a cross flow oven at 100°F for 1 hour to ensure they were dry.

After Cleaning





Ion Chromatography After Cleaning

Condition	Sample Description	Cl ⁻	NO ₂ ⁻	Br ⁻	NO ₃ ⁻	WOA
After Clean	Sample # 2 area 2	2.25	0.05	1.43	0.21	10.98
After Clean	Sample # 6 area 2	0.88	0	1.02	0.27	16.66
After Clean	Sample # 11 area 2	0.47	0	0.61	0.15	12.65
After Clean	Sample # 15 area 2	0.41	0	0.78	0.13	10.65
After Clean	Sample # 27 area 2	1.08	0	1.16	0.07	10.45
After Clean	Sample # 29 area 2	1.32	0	0.69	0.28	11.08
After Clean	Sample # 34 area 2	1	0	1.85	0.14	14.43
After Clean	Sample # 39 area 2	2.44	0.11	1.57	0.28	10.83
After Clean	Sample # 41 area 2	1.44	0.05	1.41	0.18	10.23
After Clean	Sample # 48 area 2	1.35	0.08	1.81	0.23	12.47
After Clean	Mean	1.29	0.03	1.2	0.2	12.21
After Clean	Standard Deviation	0.66	0.04	0.47	0.07	2



Data Analysis

The IC results show that the units have been recovered to a level of acceptable hardware and pose a minimal risk of electrochemical migration. The boards also improved visually with shiny solder joints, less process residues, etc. These units were then placed back into environmental chamber testing and 49 of the 50 units were totally functional, the one exception was a unit that had a damaged SOT and not even the best cleaning process can fix that.



Laboratory Controlled Assemblies

The second part of this study looks at test coupons processed in a lab environment.

- The boards are standard FR-4, immersion silver boards using an industry available water soluble paste for SMT components.
- The boards were then cleaned at Foresite so they all had the same starting baseline cleanliness.
- Next, the boards were processed with liquid no-clean flux.
- Then the boards were divided into three different cleaning process groups.
- The first was DI wash only. Boards were ran through an in-line cleaner at 2 FPM, 40 PSI (top and bottom) and DI wash at 85°F.

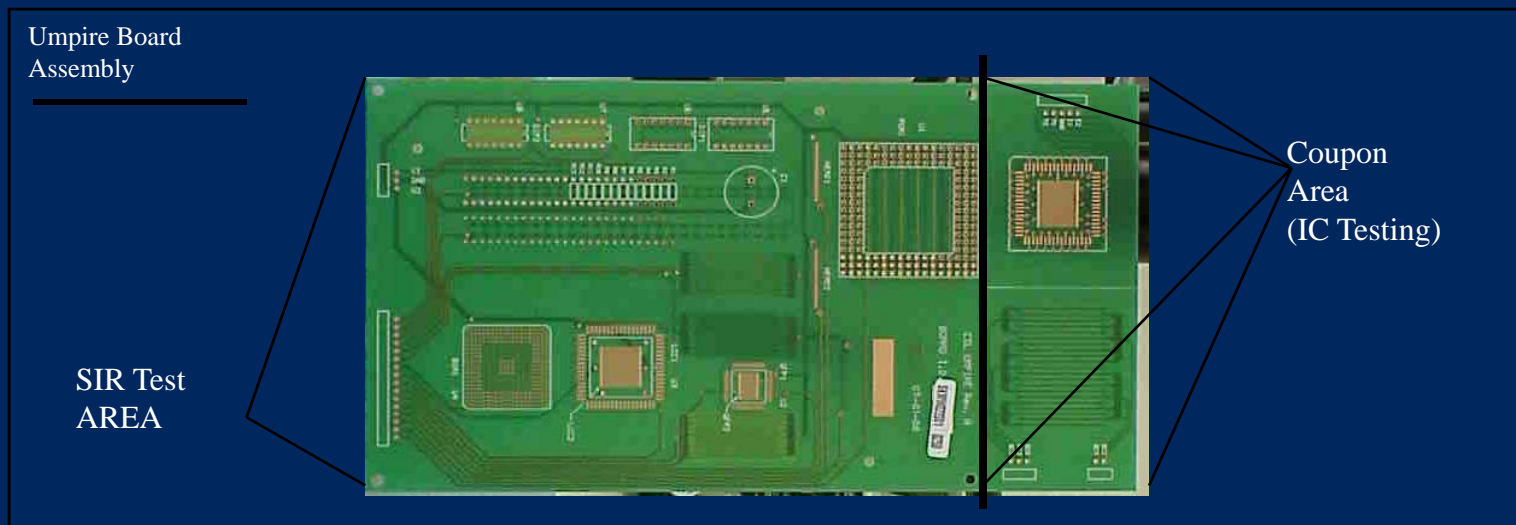


Laboratory Controlled Assemblies

- The second process was the same as the first; however a saponified wash step was added. An industry available saponifier was used at 10% and 150°F.
- The third process was the same as the first two, with steam between the wash and rinse steps added. The steam is a constant 190 PSI and each component was exposed to steam by an experienced operator.



Laboratory Controlled Assemblies



Parts Placed: LCC(2),BGA,TQFP,DIP(4)



Testing

After cleaning of the test coupons all boards went through both IC and SIR testing.

	Ion Chromatography			
Sample Description	Cl ⁻	Br ⁻	WOA	NH4 ⁺
5 Sample Set				
Bare Panel - Mean	0.85	0.33	1.57	0.98
Bare Panel - Std Dev	0.1	0.06	0.28	0.35
15 Sample Set				
DI Wash Only - Mean	0.4	0.28	175.41	2.03
DI Wash Only - Std Dev	0.07	0.05	2.82	0.32
15 Sample Set				
DI -SAP Wash - Mean	0.44	0.35	49.07	5.36
DI -SAP Wash - Std Dev	0.06	0.03	2.37	0.46
15 Sample Set				
DI-SAP-Steam - Mean	0.32	0.18	38.59	1.08
DI-SAP-Steam - Std Dev	0.31	0.15	69.65	2.14



Testing

SIR Results

SIR Testing of the 68pin LCC at 85C/85%RH

Intial	24 hrs	96 hrs	168 hrs	Final	Results
1.51 e12	5.21E+10	4.14E+09	3.12E+10	1.36E+12	Pass
2.64E+12	3.98E+07	1.22E+06	1.00E+06	1.00E+06	Failed
1.04E+11	4.14E+07	3.24E+07	1.00E+06	1.00E+06	Failed
4.27E+12	3.25E+09	5.22E+09	2.94E+10	4.85E+12	Pass



Data Analysis

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Data Analysis (cont)

Groups 1 and 2 did not have sufficient energy to penetrate the tight spacing between leads or package body and board surface. The no-clean flux creates a dam of sorts between leads and even with heated saponified wash there isn't enough contact time to break down the flux and flow under the parts where the most detrimental of the residues can be hidden and given the proper environment cause problems such as no trouble found failures and intermittent shorts. Unless you physically remove the parts to get a better look at the residues under the package body, you may not really know what is going on since to the naked eye and even under a microscope the boards may look clean between the leads.



Conclusions

Looking at both of these studies the end result is that for no-clean flux that is left on an assembly and not fully complexed, it is just a matter of time and opportunity before an issue occurs. It may be an issue of a large scale recall or a handful of no trouble found returns, there are a lot of variables at play like with most aspects of the PCB build process. The short resolution to this issue is to make sure that the flux is fully complexed whether you are looking at an issue due to the entire build process or if it is isolated to just hand solder or rework. Production houses have to do the due diligence of reflow and wave solder profiling, cleanliness monitoring and overall education of workers who have even the smallest responsibility of producing a quality product. When cleaning a no clean flux it is important to remove the flux from wave solder, surface mount soldering, localized cleaning residues and bare board / component fabrication residues. These residues, depending on their location, need different energy forms to remove the residues when rescue cleaning.



Conclusions (cont)

Wash water needs to be heated to 150°F for good ionization of the flux residues and requires a saponifier to lower the surface tension and solubilize residues trapped below the SMT components. Low pressure, high flood sprays in the wash section allow a lot of chemistry to get to the entire surface and below component areas. The amount of energy required for removing a no clean flux has included the use of DI water steam for SMT flux removal in and around the pad surface. This followed by a DI water medium pressure rinse has proven to be the most effect process and can clean thousands of assemblies or become a standard process. Removal of flux residues that were not designed to be cleaned is not easily done with water only and requires tools like Ion Chromatography with localized extractions and SIR on test coupons that show the electrical effect on the residues in high humidity.