Advances in Plating Technology: Reliable High Aspect Ratio's

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EXECUTIVE SUMMARY

The Semiconductor industry is demanding more and more from today's PWB manufacturers. This paper offers some insights to the needs, requirements, solutions and process verifications that R&D Circuits has spent years analyzing and perfecting for its customers in the industry.

The industry in question is known as the A.T.E. or Semiconductor test industry. The need is to electrically test or characterize a packaged device, prior to it being shipped to OEM's for use in their electronic devices. The package size continues to decrease, while the test regimen gets tougher and tougher. The fine pitch of devices is pushing PWB manufacturing to the far limits of capability. Six mil diameter holes drilled and plated in 0.187 thick panels (30+:1 aspect ratios) is truly on the edge of that manufacturing capability.

New techniques in drilling holes, prepping them for the subsequent plating processes, of which DRPP has proven to be a crucial step for us, and finally solid verification of those steps is a fundamental requirement for any PWB manufacturer, looking to build PWB's for this demanding industry.

Data is provided to validate the process techniques, utilizing the IST test methods, simply show that while the attributes are not those you would see in traditional PWB's, reliable and repeatable A.T.E. boards can be produced.

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Disclaimer

While the details of drilling and plating these PWB's with these attributes are not unique to R&D Circuits, there are certain Trade Secrets we cannot reveal in this presentation. These attributes ARE unique to this industry and type of board produced and we are not advocating their use in traditional PWB's.

Outline

- The Semiconductor Test Industry
- The Attributes
- The Processes
- The Verification Method
- The Results
- The Summary and Recommendations

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Semiconductor Test

- Fine Pitch Devices / Package Test
  - 0.5mm BGA
  - 0.4mm BGA
- Elevated Temperature Testing
  - 4 to 8 hours

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Semiconductor Test

Temperature Cycling for Characterization

- -40°C to +125°C

- Package Verification

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The ATE Industry

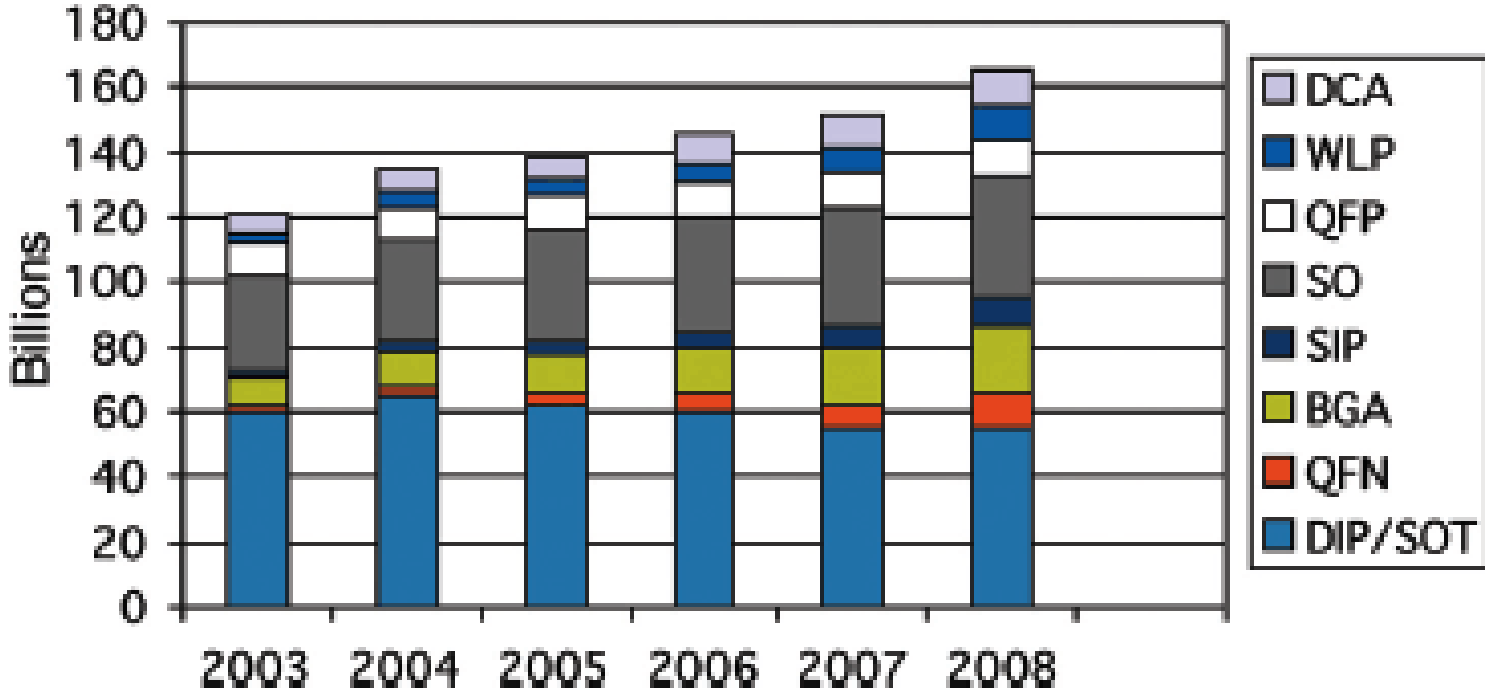

Table 1. Worldwide Semiconductor Package Volume

iNEMI Roadmap

The ATE Industry

- Packaged Device Testing
- 1.0mm – early 1990's
- 0.8mm – 0.65mm – late 1990's
- 0.5mm – 2000's
- 0.4mm – 2007
- 0.3mm – 2009
- 0.2mm – 2011

Int'l Tech Roadmap
for Semiconductors

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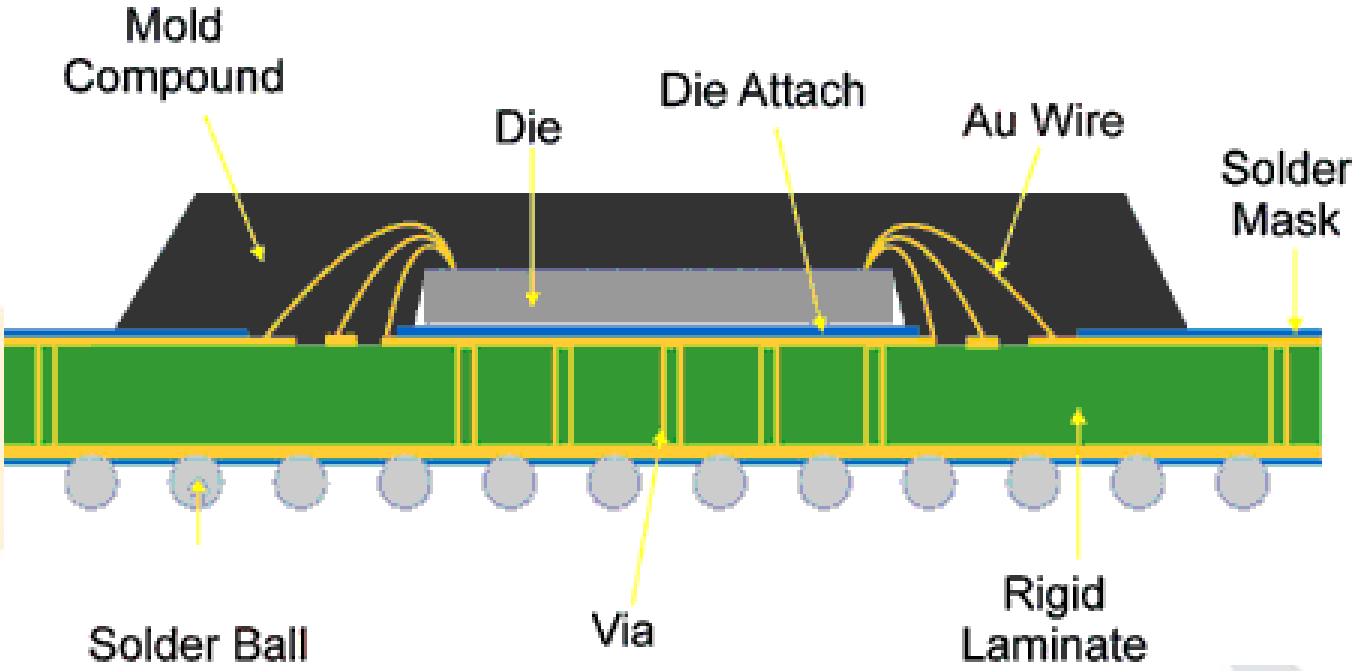
The Package



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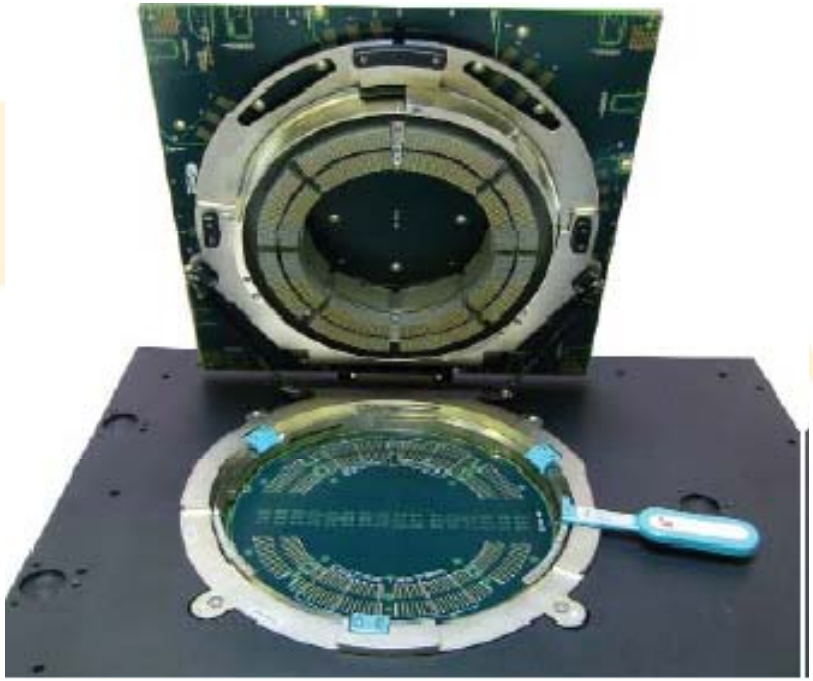
The Interface



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Engineering Evaluation

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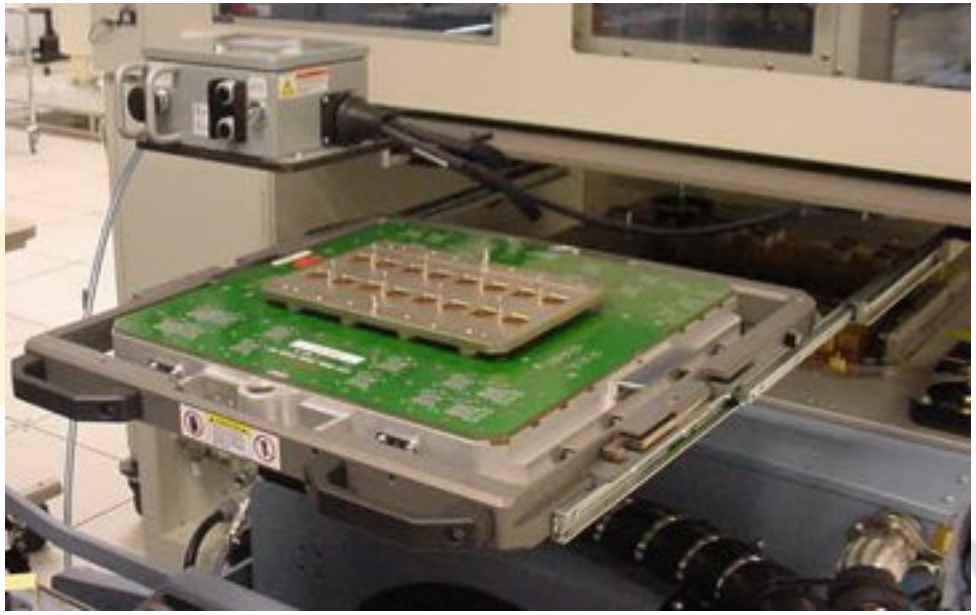
Multi-site Test



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The Test Floor

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High Aspect Ratio's

- Unique Board Geometries
  - Over-sized, not your usual 18 x 24 panel
  - Thick
    - 3.2mm minimum to > 6.4mm
  - Small holes
    - Mechanically drilled
    - 150 micron and less (100 micron currently)
  - High Aspect Ratio
    - 31:1 to 45:1

Why These are Unique

- Attributes
- One of a Kind (ok, maybe two or three)
- Thermal Extremes
- Continuous Use Environment

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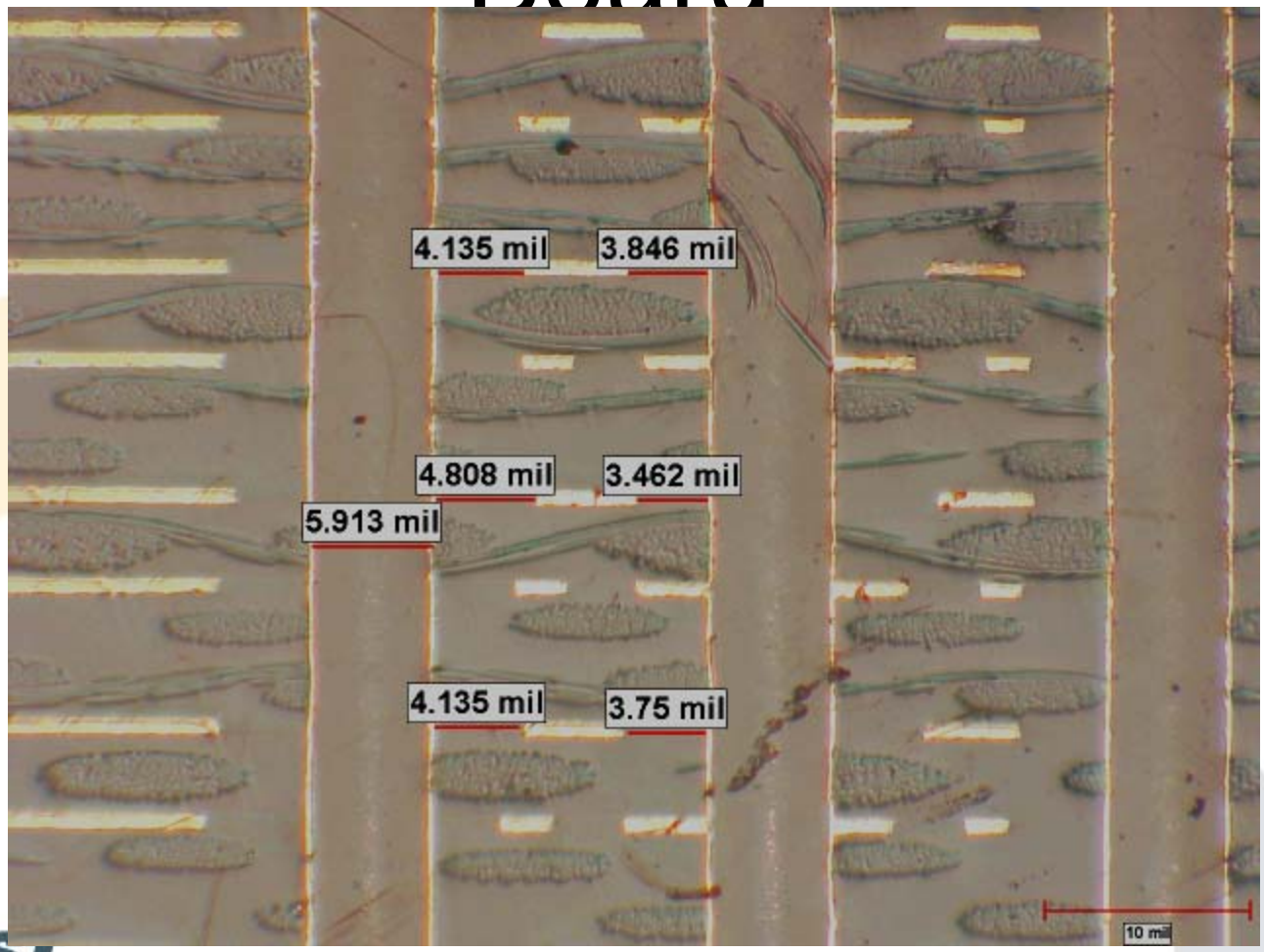
The Requirements

- The Tolerance Budget – 0.5mm
  - 0.5mm [0.0197] pitch
  - 150 micron [0.006] drill diameter (31:1)
  - 350 micron [0.0137] hole wall to hole wall
  - 100 micron [0.004] line width
  - 250 micron [0.0098] remaining / 2 =
  - 125 micron [0.00485] hole to circuit!

The Requirements

- The Tolerance Budget – 0.4mm
  - 0.4mm [0.0157] pitch
  - 100 micron [0.004] drill diameter (47:1)
  - 300 micron [0.0117] hole wall to hole wall
  - 75 micron [0.003] line width
  - 220 micron [0.0087] remaining / 2 =
  - 110 micron [0.00435] hole to circuit!

Registration on a 0.5mm Board



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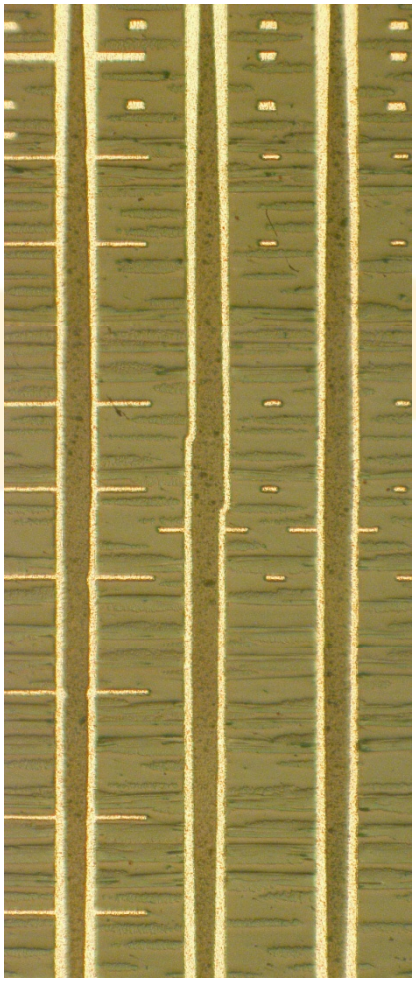
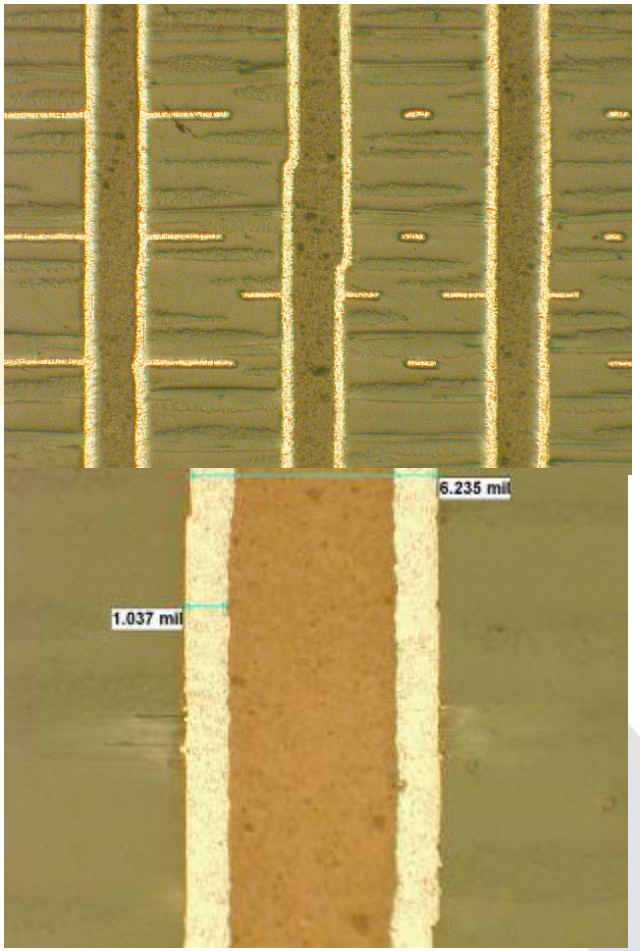
Drilling / Plating Holes





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Plating Techniques

- High Aspect Ratio
- Cleaning (debris)
- Desmear / Hole Wall Prep
- Deposition
- Develop Resist
- Pattern Plate
- Nickel / Gold!

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DRPP

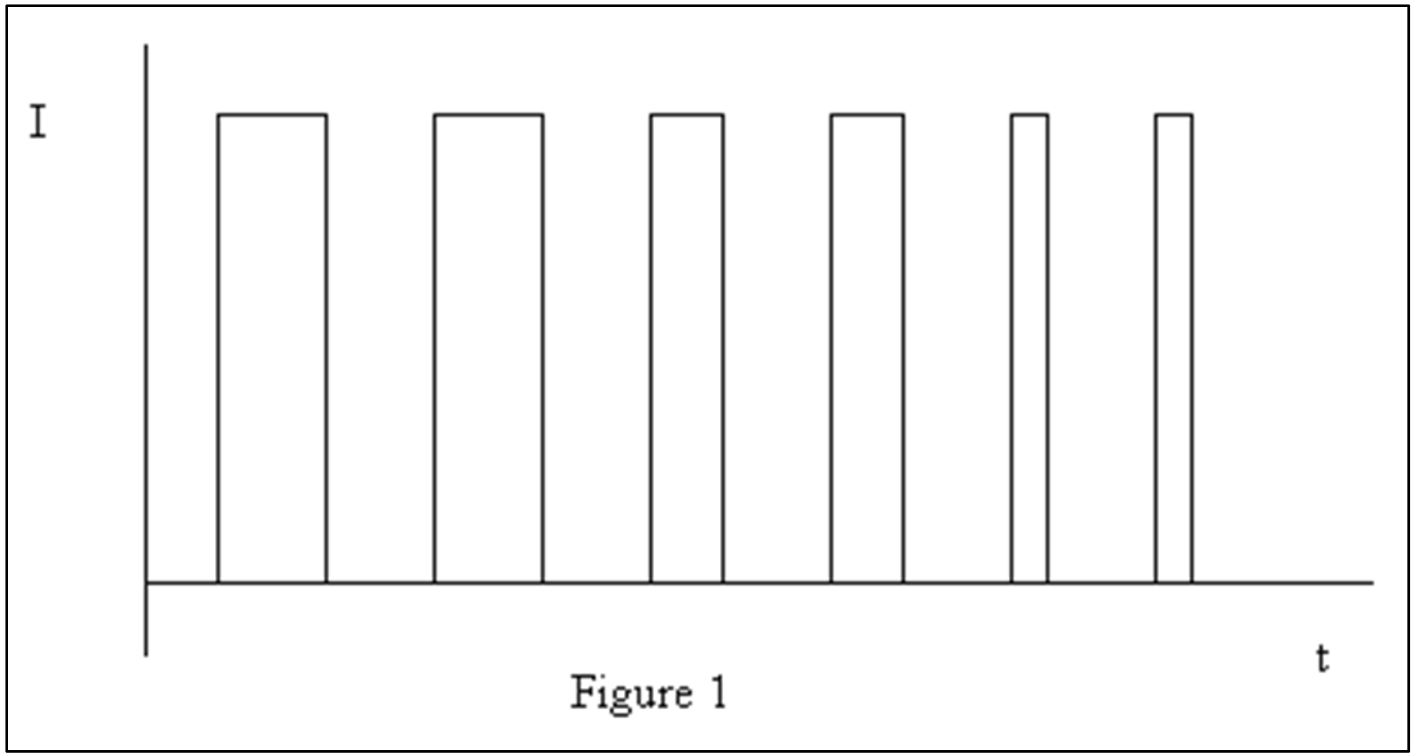

Figure 1

Pulse Rectification

DRPP

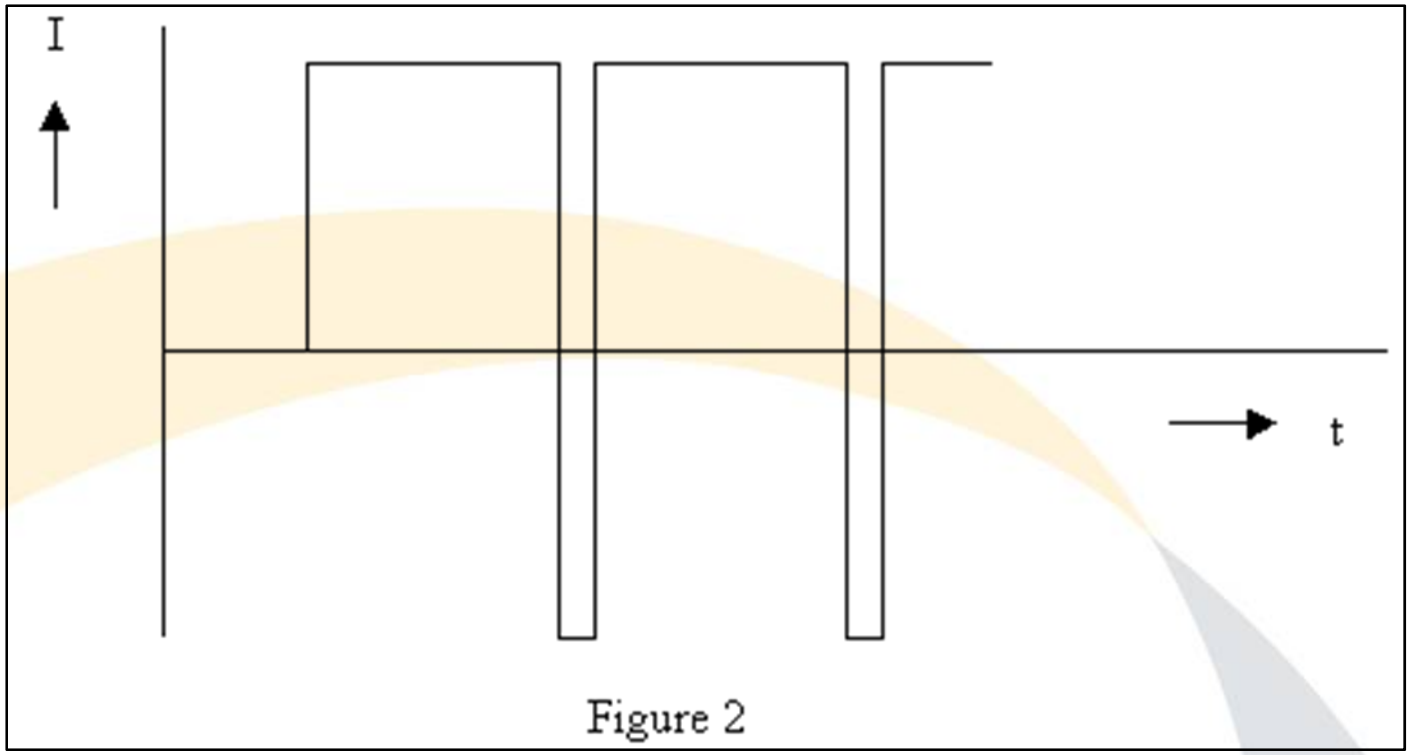

Figure 2

Switch Mode Rectification

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DRPP

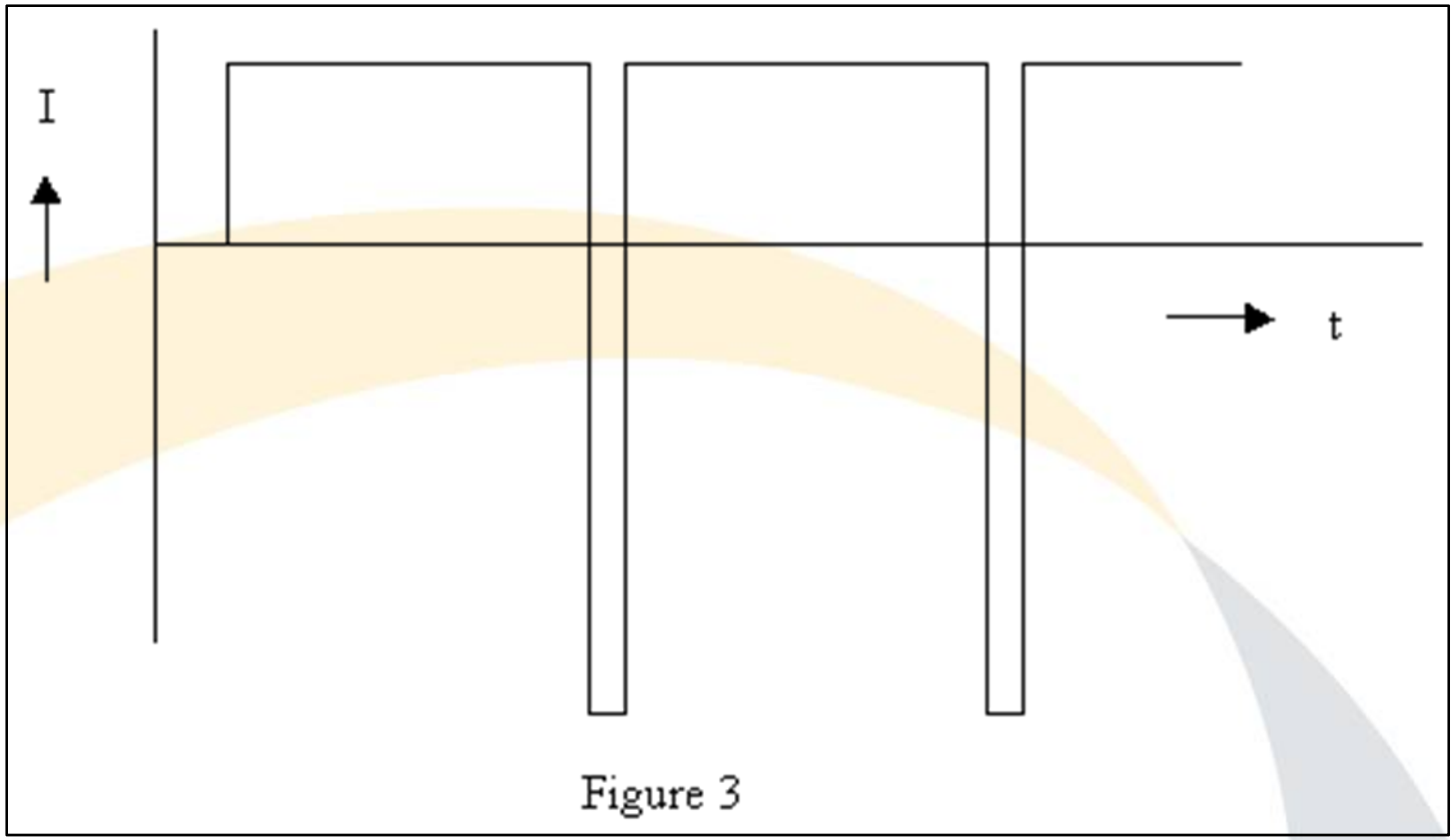

Figure 3

Reverse Pulse Rectification

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IST PWB Reliability Testing

- I.S.T. = Interconnect Stress Test
- Determines overall reliability of PWB
- Tests Copper Interconnection AND Material
- IPC Approved Test Method
- Industry Wide (Customer) Acceptance

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I.S.T. Defined

- Interconnect Stress Test
  - Thermal Cycles by Electrically Heating an IST Test Coupon
  - Continuously measures resistance of the circuits during cycle
  - 10% Increase in Resistance is Failure – Test Stops in Seconds

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I.S.T.

- Primary Objectives
  - Reduce Time to Results
  - Reduce Cost
  - Repeatability and Reliability
  - Automation of Testing and F/A

IST

- Micro-sectioning vs. I.S.T.
  - Low # of holes / high number of holes
    - 1 degree vs. 360 degree
      - Circumference of all connections
  - Go / NoGo vs. quantifying severity
  - Poor vs. Excellent Repeatability
  - Not operator dependent
  - Visual criteria vs. Electrical criteria

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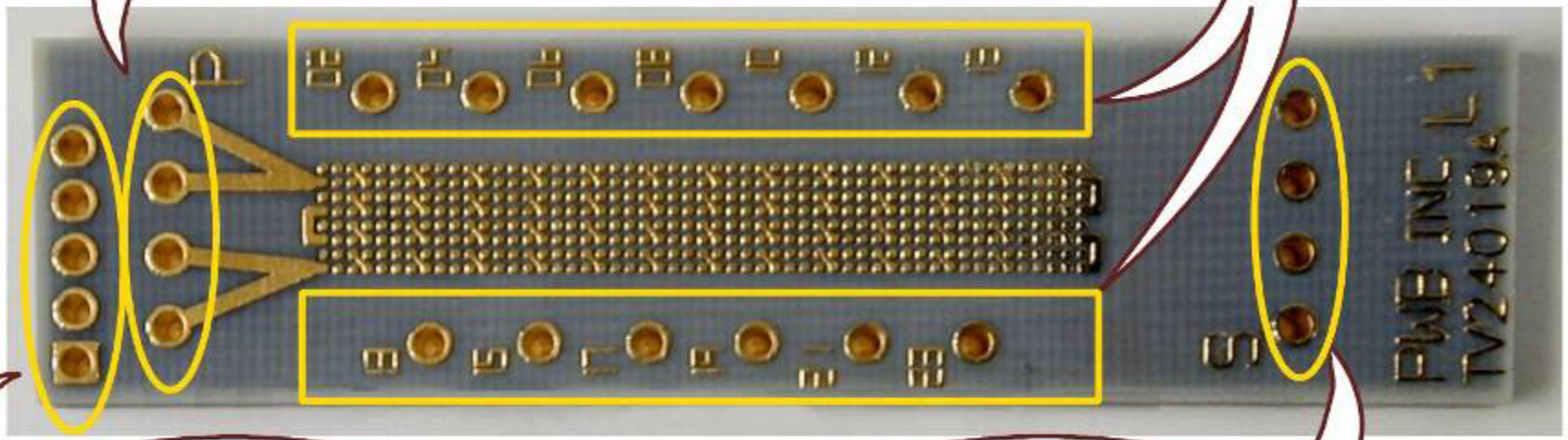
IST Coupon - TV24019



Interconnect Integrity

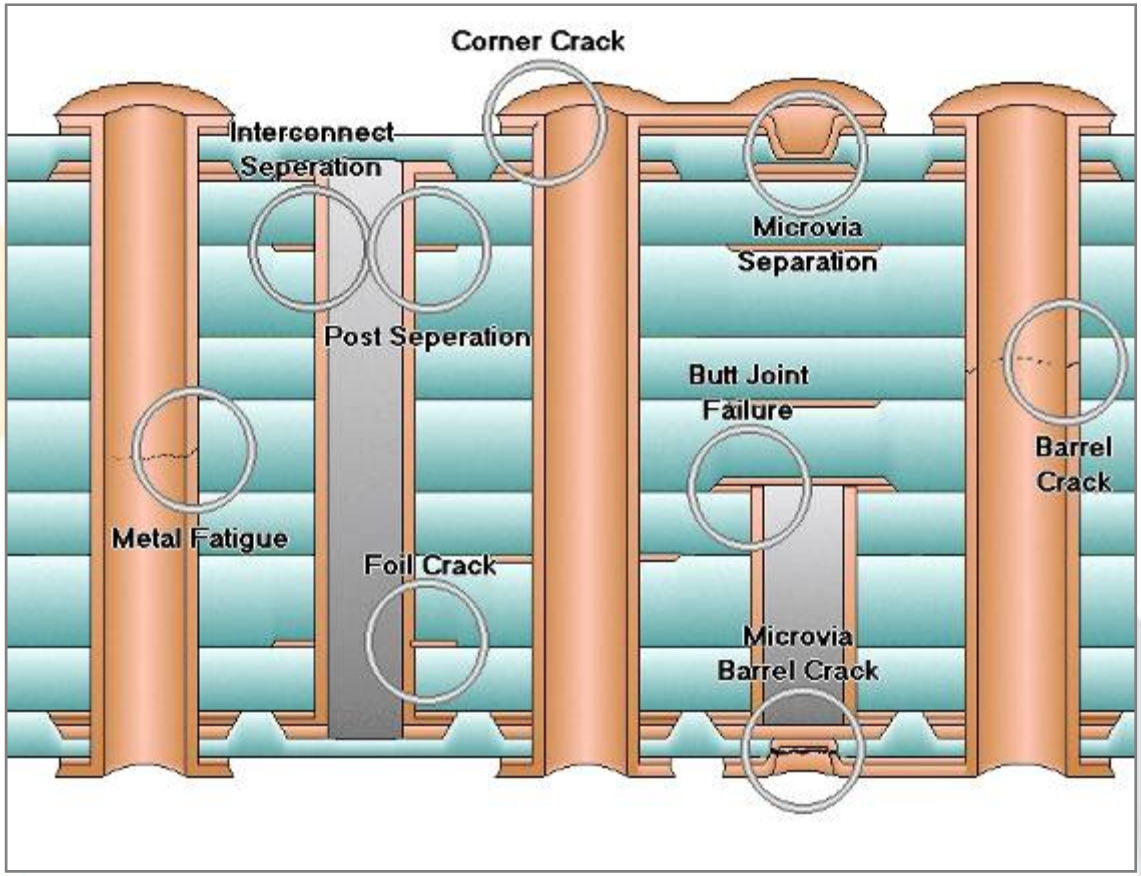
Material Integrity

Registration

PTH Barrel Integrity Cu

24 Layer
.005" PTH
.020" Grid

Traditional Failure Modes



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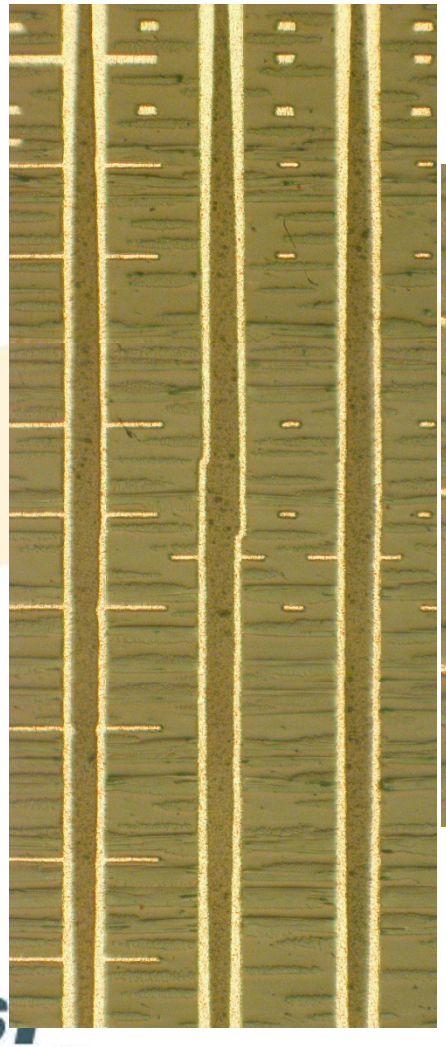
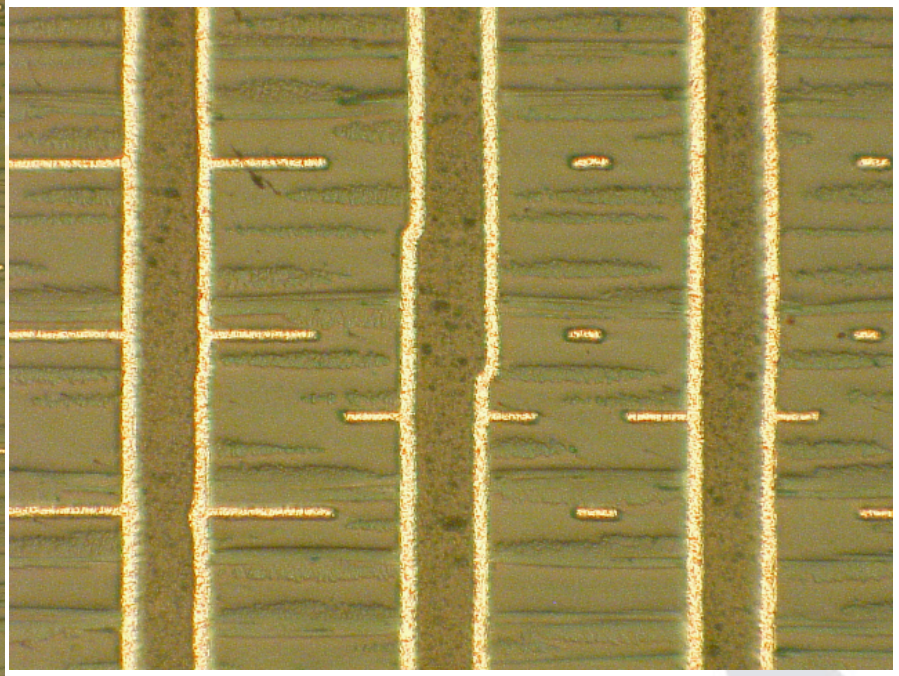
Non-traditional Failure Modes?





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Some Data

IST Data – J07_1898

IST Cycles to Failure – S/N 9 – 2X230˚C

IST Cycles to Failure - S/N 9 - 2X230°C					
COUPON	P1	% P1	S1	% S1	Results
13_9A	1000	0.1	1000	0.2	Accept
13_9B	1000	-0.5	1000	-1	Accept
13_9C	1000	0.4	1000	-0.4	Accept
13_9J	1000	0.4	1000	0.1	Accept
Mean	1000.0	0.1	1000	-0.3	
StDev	0.0	0.4	0.0	0.6	
Min	1000.0	-0.5	1000	-1.0	
Max	1000.0	0.4	1000	0.2	
Range	0.0	0.9	0	1.2	
Coef Var	0%		0%		

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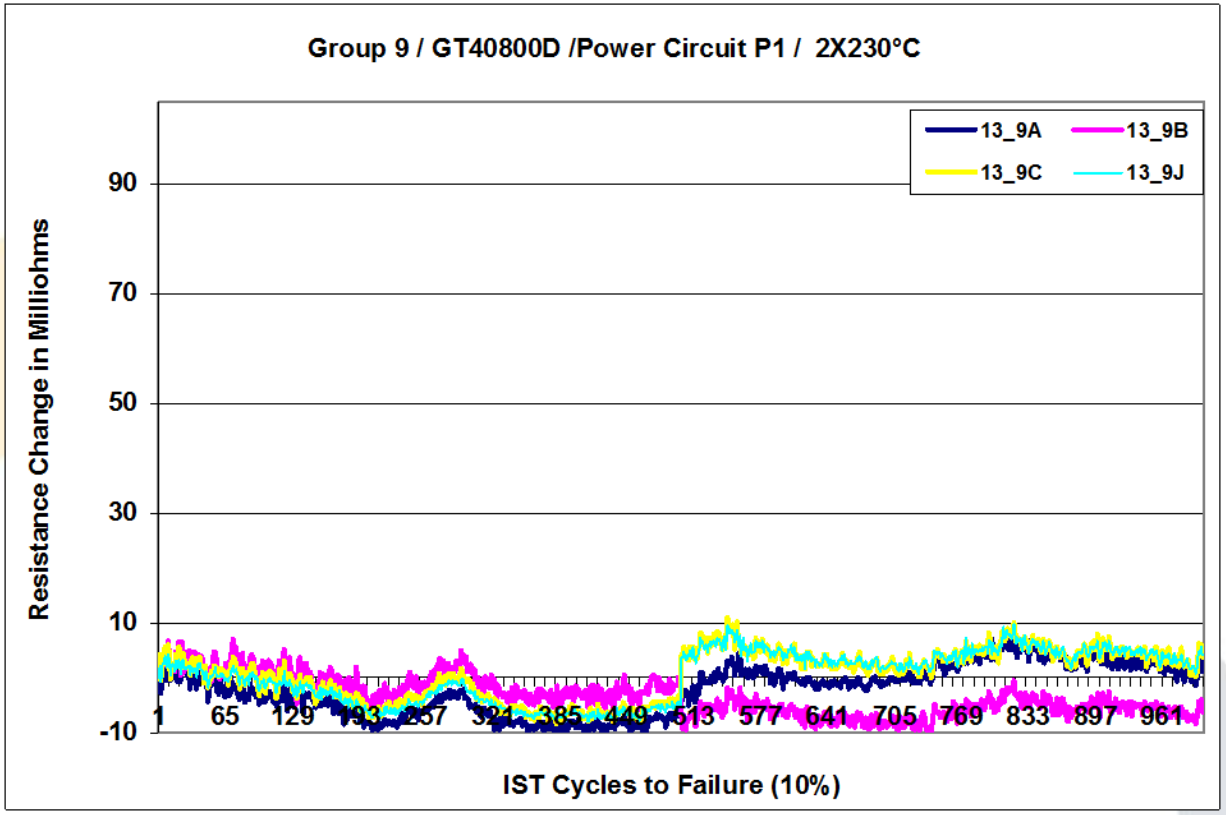
Graphing the Results



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Some more Data

IST Cycles to Failure – S/N 10 – 2X230° C

IST Cycles to Failure - S/N 10 - 2X230°C					
COUPON	P1	% P1	S1	% S1	Results
13_10_A	1000	-0.1	1000	1.8	Accept
13_10_B	1000	0	1000	3.1	Accept
13_10_C	N/A	0.6	669	10	S1
13_10_E	1000	-0.1	1000	2.1	Accept
Mean	1000.0	0.1	917	4.3	
StDev	0.0	0.3	165.5	3.9	
Min	1000.0	-0.1	669	1.8	
Max	1000.0	0.6	1000	10.0	
Range	0.0	0.7	331	8.2	
Coef Var	0%		18%		

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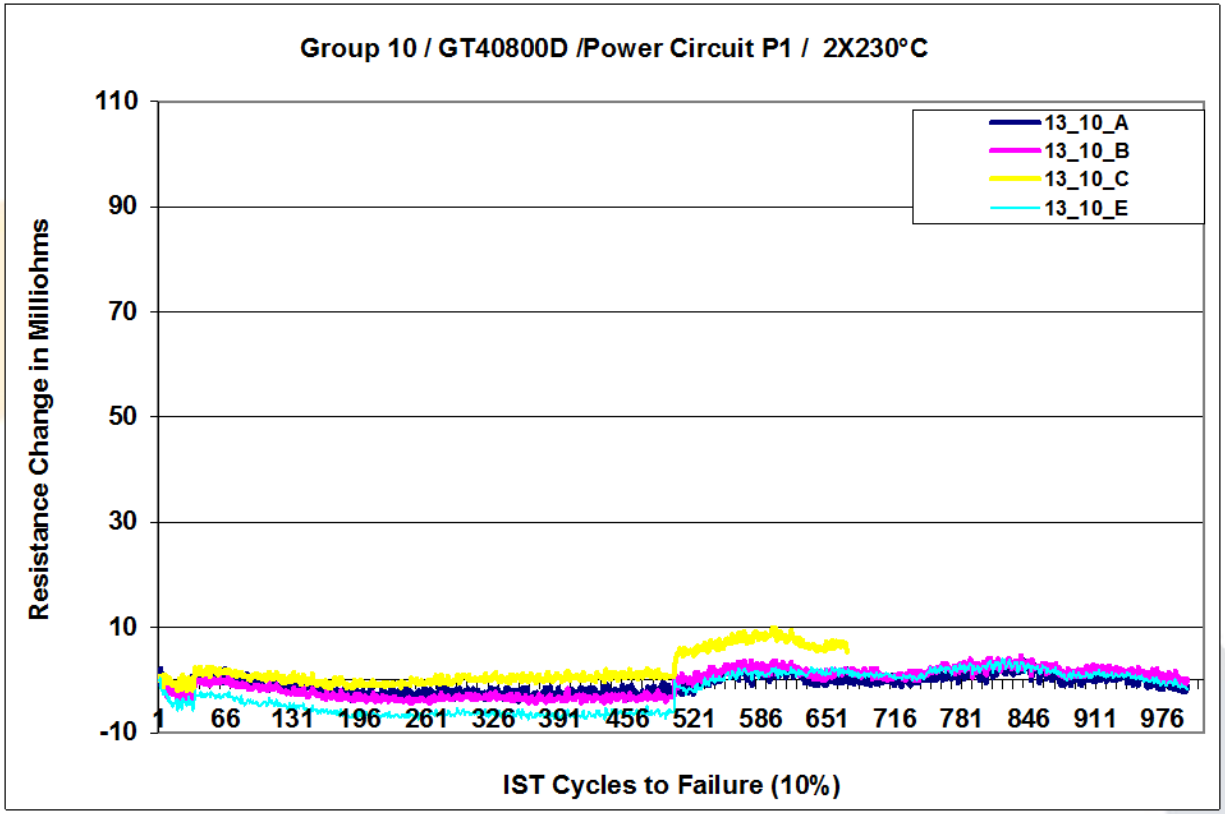
Graphing the Results



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The Cause?

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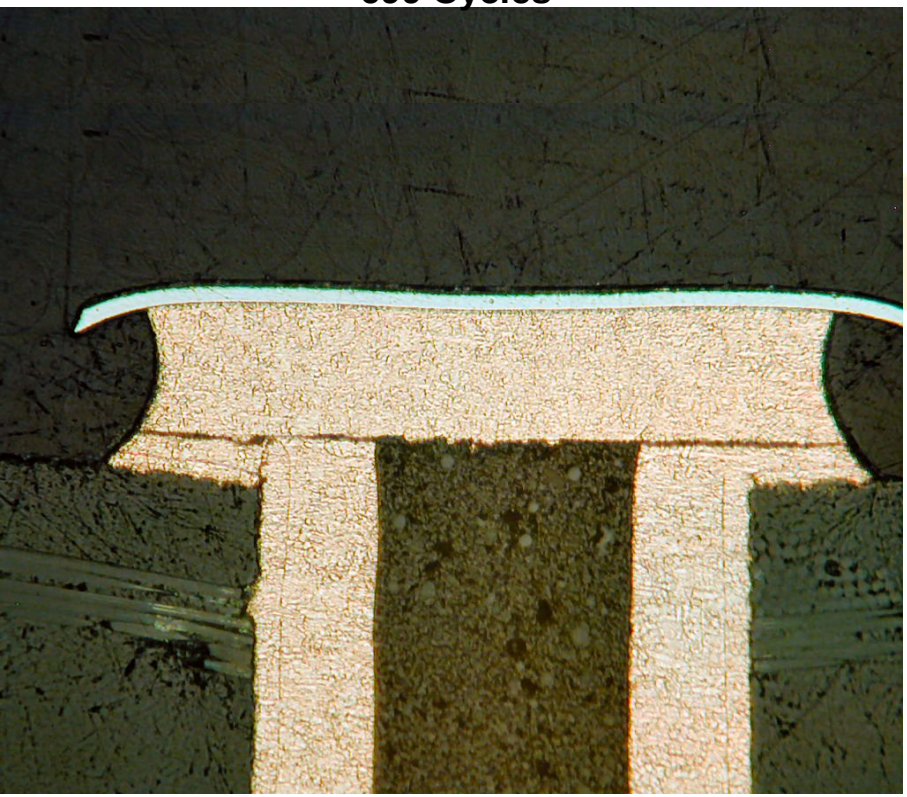
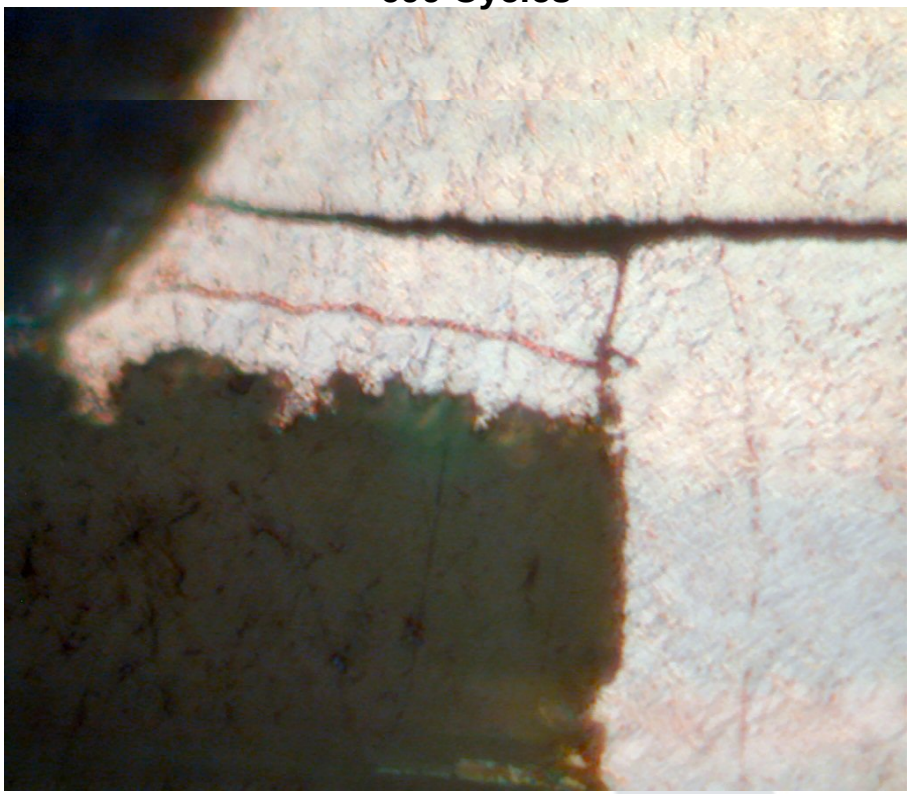
The Real Failure

XS# 3811, Coupon 13-10C - 2X230˚ C - Failed S1, 699 Cycles



XS# 3811, Coupon 13-10C - 2X230˚ C - Failed S1, 699 Cycles



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Summary

- The Semiconductor Test Industry
- The Attributes
- The Processes
- The Verification Method
- The Results

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Acknowledgements

The author wishes to acknowledge the assistance and participation in this presentation by PWB Interconnect Solutions, Inc. Nepean, Ontario Canada

Bill Birch – President, Sales & Marketing

Paul Reid - Program Coordinator