Investigation into the Mass Imaging aspects of 0.3mm Wafer Level Chip Scale Package solder paste deposition.

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Abstract

Due to the ever-aggressive miniaturization program that is rolling through the electronics industry, the next component that is fast approaching this horizon is the 0.3mm CSP. This device represents a major assembly revolution within the Surface mount assembly (SMT) arena. The implementation of this device will require arrays of mass imaged solder paste that only a few years ago where within the hemisphere of semiconductor fabrication. This transition into SMT is a huge step when you consider the typical sub 7 sec cycle times requirements of SMT against relatively slow Semicon ball bumping cycle times, the thin uneven FR4 boards generally used in SMT against the perfectly flat wafers found in Semicon and the standard working environments opposed to the clean room environments found in Semicon.

This paper will research the key elements that influence the deposition process. Process design factors such as solder paste, squeegee construction and stencil design will be fully investigated. In addition the impact of typical fabrication defects associated to the fabrication of stencils will be observed to ensure that an authentic picture is created and not one that belongs in a laboratory.

The deliverables from this paper will be clear and concise implementation solutions for the surface mount engineers who are about to encounter the 0.3mm C.S.P.

Experimental conditions

1) Printing machine

A DEK Galaxy printer was used throughout this study. The machine was calibrated using the manufacturer's defined procedure to verify a post print alignment Cp and Cpk of 2 @ 12.5 microns. To reduce the amount of statistical noise the same machine and squeegee interface was used throughout the experiment, as well as the same batch of substrates.

2) Process Set-up

The process set-up for the experiment can be seen in Table 1. The parameters were adopted from previous work carried out with the solder paste materials.

Parameter	Value & Unit
Print Speed with standard blades	50mm/s
Print Pressure with standard blades	4Kg
Print Speed with Cr-Ni blades	50mm/s
Print Pressure with Cr-Ni	6Kg
Separation Speed	2mm
Separation Distance	5
Squeegee Angle	60 Deg
Tooling	81mm pins
Temp & Humidity	21 Deg C & 40%

Table 1: Process Set-up

A total of 3 boards were printed on a set-up substrate before each production board was assembled. The purposes of the 3 dummy prints ensured an optimized condition for the paste as well as lubrication for the stencil apertures; both these actions ensured that the print process was stabilized before assembly. To further help reduce any statistical noise the print direction for all production boards was set to a forward print stroke.

To help with analysis all production prints were photographed before assembly.

A Universal GSM carried out the placement of the devices and a Soltec XPM2 employed to carry out the duties of reflow. The reflow atmosphere was for the most part was air but one production run (run11) was carried out in Nitrogen (O^2 50PPM), the reflow profile can be seen in Diagram 1.



Diagram 1: Reflow Profile

Materials

The following sections explain the material (Inputs) that was used during this investigation.

1) Solder pastes

The solder paste samples used in this investigation are shown in Table 2. All samples were suspended in a Lead Free no clean flux medium. All samples shown in Table 2 are commercially available.

Table 2: Solder pas	tes investigated.
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Paste label	Alloy type	Metal content (%	Particle size
		weight)	
1	Sn96.5Ag3.0Cu0.5	89	Туре 3
2	Sn96.5Ag3.0Cu0.5	88.75	Type 4

2) Stencils

The stencil set used for this experiment consisted of 4 masks; the configuration can be seen in Table 3

Table 3: Stencils investigated.

Stencil label	Fabrication method	Metal	Metal type	Quality
		Thickness		
А	Laser YAG	50 micron	SS 304	High-quality
В	Laser YAG	75 micron	SS 304	High-quality
С	Laser YAG	75 micron	SS 304	Inferior
D	E-Form	66 micron	Ni	High-quality

The aperture designs associated with the stencils shown in the Table 3 are illustrated below in Table 4; the location references are shown in Diagram 2.

Table 4: Aperture dimensions

Stencil label	Location A	Location B	Location C	Thickness
Stencil A	125	140	155	50 microns
Stencil B	170	180	190	75 microns
Stencil C	190	200	210	75 microns
Stencil D	170	180	190	66 microns



Diagram 2: Design locations

As can be seen from Table 3 and 4 a full array of stencil designs and fabrication methods have been utilized for this investigation. The choice of metal thickness and aperture size has been selected to emulate a wide range of solder paste deposits. In addition to the thickness and aperture size a quality factor was also included into the investigation. Stencil C was intentionally fabricated to cause an inferior aperture finish; this was achieved by ensuring the focal point of the YAG laser was defocused during manufacture.

As can be seen the extensive number of designs has provided a full array of area ratios, these designs will be tracked throughout this experiment.

To complete the details of the stencil design, Table 5 outlines the area ratios associated with each design, for clarity each design has been color-coded relating to the expected capability. It can be noted that the area ratios cover an area that border the recognized rule (≥ 0.66). It is the intention of this investigation to discover the closeness that these rules need to be followed. This is an important fact to discover, as the geometries of the stencil must allow heterogeneous assembly.

Stencil label	Location A Area ratio	Location B Area ratio	Location C Area ratio
Stencil A	0.63	0.7	0.78
Stencil B	0.57	0.6	0.63
Stencil C	0.63	0.66	0.7
Stencil D	0.64	0.68	0.72

Table 5: Area ratios for all stencil designs + expected capability

3) Squeegee

Two squeegee blades were used during this investigation, the standard Dek Stainless Steel and a Cr nitride (Cr-Ni) coated blade. Table 6 shows physical characteristics of both blades.

Table 6: Squeegee configuration

Blade Type	Blade thickness	Blade length	Coating
Α	200 microns	170mm	None
В	250 microns	250mm	Cr-Ni

4) Boards

The board was fabricated from a 4-layer FR4 construction with an overall thickness of 0.9mm. The board design incorporated a daisy chain function for all 15 locations therefore electrical integrity could be carried out during the analyses.

During the set-up it was found that the solder mask was not accurately applied on several locations thus causing the land locations to drift in relationship to the CAD position. Due to time pressure this batch of boards was still utilized but during the analysis process this issue would need to be considered.

The dimensions of both the substrate and device can be seen in Diagram 3 below.



Diagram 3: Dimensions of substrate and device

Analysis

The following sections outline the findings that were observed throughout this investigation.

1) Continuity testing

The following section of this paper is focused on analyzing the devices that failed the continuity testing.

As mentioned in the materials section above, the board and component design included a daisy chain configuration. This greatly facilitated the ability to quickly isolate any defective areas of aboard.

Table 6a and b below represents the number of failed devices with respect to stencil and paste type. The color-coding quickly shows the combinations that produced either defects (red) or no defect (green); the data is shown as a percentage of total defective devices.

Table 6a: Number (%) failed Locations for type 3 solder paste

Paste Type	Stencil	% of Location A fails	% of Location B fails	% of Location C fails
3	A	100.00%	0.00%	0.00%
	B	60.00%	20.00%	0.00%
	с	75.00%	20.00%	40.00%
	D	20.00%	0.00%	0.00%

Table 6b: Number (%) failed Locations for type 4 solder paste

Paste Type	Stencil	% of Location A fails	% of Location B fails	% of Location C fails
4	A	40.00%	0.00%	0.00%
	В	0.00%	0.00%	0.00%
	с	0.00%	20.00%	0.00%
	D	20.00%	0.00%	0.00%

Paste Type 3



Graph showing Fails for type 3 paste

Graph 1: % of location fails Type 3 solder paste

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Graph showing Fails for type 4 paste



Graph 2: % of location fails, Type 4 solder paste

The graphs above graphically show the data presented in table 6a and b, it is clear to see the impact that both the stencil and solder paste type has on the assembly process.

2) Die penetration

To further analyze the failed locations a die penetration technique was utilized to identify the number of failed interconnect per device.

This technique requires a strong dye (Engineers Red) to be soaked into the defective part and then cured, the defective part is then delaminated from its position. All interconnects that had electrical and mechanical integrity would not be stained by the dye due to the inability for the dye to pregnant the joint structure. However any interconnects that was not fully formed would be impregnated with the dye and thus after delaminating, visible marks would be present.

Figure 1 below shows an example of the results from a die penetration test, it can be clearly seen that in this example the low volumes of solder paste detected have resulted in visible marking.



Solder Paste image

Die penetration image

Figure 1: Example of a dye penetration (Board 1site 10)

Table 7 below shows the die penetration results for all failed devices. This data also shows the impact that stencil and solder paste had on the assembly process.

	Sum of Failed Interconnects	Sum of Failed Interconnects
Stencil	Туре 3	Туре 4
Α	33	19
В	26	0
С	64	3
D	3	1

Table 7: Number of failed interconnects

Graph showing the number of failed interconnects versus Stencil and area ratio $Type \ 3$ Solder paste



Graph 3: No of failed interconnects versus stencil type and area ratio, type 3 solder paste



Graph showing the number of failed interconnects versus Stencil and area ratio Type 4 Solder paste

Graph 4: No of failed interconnects versus stencil type and area ratio, type 4 solder paste

The graphs above graphically show the data presented in table 7 together with the area ration associated with the failed aperture designs, it is clear to see the impact that both the area ratio and solder paste type has on the assembly process.

3) Cross section

A number of locations were selected for cross section; the main aim of this activity was to understand the cause and effect of a failed interconnect. Figures 2 below shows a failed interconnect on board 3 site 14. It is clear to see that this interconnect has failed to form and has left an interspaced between pad and device.

Figure 3 shows the corresponding solder paste deposit on board 3 site 14. It can be seen in Figure 3 that the solder paste volume was insufficient therefore the result shown in Figure 2 would be expected.



Figure 2: Photograph of a failed interconnect, Board 3 site 14



Figure 3: Photograph of solder paste deposit, Board 3 site 14

4) Stencil Analysis

If we remember from the materials section (stencils), four different stencils were fabricated for this investigation. Figures 4, 5, 6 and 7 show the aperture appearance, all images are taken from location 1 of the artwork.

Figure 4 shows the smallest aperture used in this investigating (125 microns), a small amount of deformation can be seen on several of these apertures. This was due to the limitations of the laser equipment used.

As can be seen from Figure 5, the 75-micron laser cut stencil is fabricated to a high standard, with respect to size and finish.

Figure 6 a & b shows Stencil C, this stencil was fabricated with a defocused laser and the effects can be seen in Figure 6b. As can be seen the edges of the aperture are extremely irregular, it would also be expected that the aperture walls would also contain micro swarf. This type of defect would be expected to give solder paste release issues due to the stencil clogging.

Figure 7 shows the Electro Formed stencil (Stencil D), it is clear to see the highly defined edge definition.



Figure 4 Stencil A



Figure 5 Stencil B

 Table 8: Stencil Measurements

Stencil	Site No	Top min	Top Max	Bottom min	Bottom max	Target	Delta
А	1	108	110	134	135	125	10
	15	109	110	139	143	125	18
В	1	155	160	180	183	170	13
	15	150	155	180	182	170	12
С	1	176	182	182	185	190	-5
	15	179	182	182	185	190	-5
D	1	162	165	167	167	170	-3
	15	164	166	166	168	170	-2

To complete the stencil analysis the aperture diameters were measured. Table 8 shows the results from this test. It can be seen from Table 8 that Stencils A and B experienced the greatest deviation from target. Stencil C, even with the defocused laser, produced accurately sized apertures. However, it is clear from the top and bottom results that the trapezoidal characteristic, that is associated with laser cut stencils, has disappeared. Stencil D produced not only a precise circumference but also produced the diameter closest to target. Therefore one could assume that this stencil would give the best assembly results.



Figure 6 A Stencil C

Figure 6 B Stencil C



Figure 7 Stencil D

5) X-ray

The final part of the analysis was to investigate the effect that a solder paste bridge would have on the assembly process. During the print cycle for build 10 two solder paste bridges were noted on site 11. This board was assembled and reflowed in the normal manner. After assembly the device was inspected with X-ray to determine if a post reflow solder bridge was present. Figure 8 shoes the wet solder paste deposit and an image created by the X-ray inspection. As can be seen the solder paste bridge did not manifest itself into a post reflow solder bridge.

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Figure 8 Solder Deposit and X-ray of Board 10 Site

Conclusion

As a result of employing several failure mode analysis techniques it has been possible to conclude the following points: -

Stencils

Fabrication method.

The data from Graph 3 shows the impact that stencil fabrication has on the assembly process. It can be seen from Graph 3 that all stencils produced a number of defects but it is clear that stencil C produced the majority. All aperture designs associated with stencil C was kept within the ≥ 0.66 rule therefore it can be concluded that the poor assembly results are due to the induced quality issues.

Release efficiency and process window.

The choice of metal thickness and aperture diameters used throughout this investigation produced a wide range of area ratios shown in Table 5, the color-coding represents the expected capability.

Type 3 Solder paste.

The data shown in Table 6a & b shows the percentage of electrically failed locations (100% represents all 5 locations failed). It can be seen that when we compare the results obtained from the run using Type 3 solder paste (Table 6a), the results closely match the predicted results shown in Table 5.

Thus we have proven that Type 3 can be used in the 0.3mm CSP assembly process but the current area ratio rule of greater than 0.66 needs to be followed to ensure that satisfactory yields are produced. To create a 0.3mm CSP aperture that follows the 0.66 rule we need to select one of the options below

A 50-micron mask thickness and aperture diameters in the ballpark of 180 microns (this figure has been concluded from the results gained from Stencil B) would be required. However the 50-micron mask thickness this would undoubtedly cause insufficient volumes issues with other technology types, thus not complying with heterogeneous assembly requirements.

A thicker material (75 microns) would be required but the aperture diameters would need to be greater than 200 microns. These aperture sizes could possible lead to solder paste bridging due to the inter-space occurring at 100 microns or less.

Both these options are not lending themselves to a high volume assembly.

Type 4 Solder paste.

Table 6b shows the process window that was achieved by changing the print process to Type 4 solder paste, as can be seen the process window is vastly improved. This enhancement can be graphically seen when comparing Graph 1 against Graph 2; it is clear to see that the results obtained from the Type 4 material has reduced the overall number of failed locations. Graph 2 also shows no fails were produced with Stencil B, this suggests that all designs are compatible with the 0.3mm CSP assembly process.

The poor assembly results obtained from Stencil C was also reduced and the location that did fail was limited to the smallest design (Location C - 170 micron). Using Type 4 paste also reduced the impact that the Electro Formed had on the assembly process.

In summary the material set that is best suited towards 0.3mm CSP assembly is.

Type 4 solder paste 75 micron thick stencil High quality Laser cut stencil or Electro Formed Aperture diameters ranging from 170-190 microns

Solder bridging

During this investigation only very small numbers of solder paste bridges were produced. However as can be seen from Figure 8 the solder paste bridges did not cause a post reflow bridging, this could be due to the small volume's of solder paste versus the relatively large surface area of the ball. However comments from the field have alleged that with Ball array packages it is insufficient that are the more common failure mode, for that reason this paper is focused on understanding the stencil design in connection with the lower limit of solder paste

Squeegee Blades

During this investigation a chromium nitride coated squeegee blade was used for run 10. The stencil that was used for this run was Stencil C (poor quality) therefore the results that were expected would be similar to Graph 1 (Stencil C + Standard blades+ Type 3 paste + Air atmosphere). However it was discovered that the results from run 10-showed no failed interconnects, this is in contrast to run 3, which produced 64 failed interconnects.

This delta could be due to the Cr-Ni squeegee coating offering a low resistance, which in turn delivers an improved material flow rate at the squeegee blade tip. An alternative reason for this improvement could be due to the increased rigidity of the squeegee blade which in turn reduces the attach angle. Due to this test occurring at the end of this investigation the number of devices and substrates were limited therefore this phenomenon will need further investigation.

Reflow atmosphere.

During this investigation a nitrogen rich atmosphere was used for Run 11. The results from this test showed that nitrogen reduces the number of failed interconnects when compared with a comparative Air atmosphere set-up but due to limited devices and substrates this phenomenon requires further investigation.

Further work to be conducted on the assembly of 0.3mm CSP

Reflow atmosphere Squeegee coating Reliability testing



0.3mm W.L CSP Assembly

Clive Ashmore



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DG1 Debbie Gomez, 7/18/2005

Abstract

Due to the ever-aggressive miniaturization program that is rolling through the electronics industry, the next component that is fast approaching this horizon is the 0.3mm CSP



Abstract

- This paper will research the key elements that influence the 0.3mm CSP deposition process.
- Process design factors such as solder paste stencil design and substrate will be fully investigated.

 The impact of typical fabrication defects associated to the fabrication of stencils will be observed to ensure that an authentic picture is created and not one that belongs in a laboratory.





Experimental conditions



Experimental conditions

Parameter	Value & Unit
Print Speed with standard blades	50mm/s
Print Pressure with standard blades	4Kg
Separation Speed	2mm
Separation Distance	5mm/s
Squeegee Angle	60 Deg
Tooling	81mm pins
Temp & Humidity	21 Deg C & 40% R.H



Line configuration

- A Dek Galaxy carried out the Solder paste printing
- A Universal GSM carried out the placement of the devices
- A Soltec XPM2 employed to carry out the duties of reflow. The reflow atmosphere was air.



Experimental conditions

- 3 boards were printed on a set-up substrate before each production board was assembled this ensured an optimised condition for the paste as well as lubrication for the stencil apertures
- To further help reduce any statistical noise the print direction for all production boards was set to a forward print stroke.



Reflow - Profile





Materials - Solder pastes

Paste label	Alloy type	Metal content (% weight)	Particle size
Х	Sn96.5Ag3.0Cu0.5	89	Type 3
Y	Sn96.5Ag3.0Cu0.5	88.75	Type 4

All samples were suspended in a Lead Free no clean flux medium, single supplier and are commercially available.



Stencil – Fabrication type

Stencil label	Fabrication method	Metal Thickness	Metal type	Quality
Stencil A	Laser YAG	50 micron	SS 304	High- quality
Stencil B	Laser YAG	75 micron	SS 304	High- quality
Stencil C	Laser YAG	75 micron	SS 304	Inferior
Stencil D	E-Form	66 micron	Ni	High- quality



Stencil- Design Locations



Stencil – Aperture Size

Stencil label	Location A	Location B	Location C	Thickness
Stencil A	125	140	155	50 microns
Stencil B	170	180	190	75 microns
Stencil C	190	200	210	75 microns
Stencil D	170	180	190	66 microns



Stencil – Area Ratio's

Stencil label	Location A	Location B	Location C	Thickness
Stencil A	0.63	0.70	0.78	50 microns
Stencil B	0.57	0.60	0.63	75 microns
Stencil C	0.63	0.67	0.70	75 microns
Stencil D	0.64	0.68	0.72	66 microns

Ref - IPC 7525



Circuit Board



Board construction = FR4,0.9mm thick & Multi-layer





The board design incorporated a daisy chain function for all 15 locations therefore electrical integrity could be carried out during the analyses. The 0.3mm CSP has 264 IO

Issues with substrate fabrication

- Random solder resist mis-registration
- Will this cause assembly issues ?







Analysis



Continuity testing results

Paste Type	Stencil	% of Location A fails	% of Location B fails	% of Location C fails
3	А	100.00%	0.00%	0.00%
	В	60.00%	20.00%	0.00%
	С	75.00%	20.00%	40.00%
	D	20.00%	0.00%	0.00%

Paste Type	Stencil	% of Location A fails	% of Location B fails	% of Location C fails
4	А	40.00%	0.00%	0.00%
	В	0.00%	0.00%	0.00%
	С	0.00%	20.00%	0.00%
	D	20.00%	0.00%	0.00%

100% = All 5 locations failed







Continuity testing - Type 4

Graph showing Fails for type 4 paste



Die penetration – IPC 7095A

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Example of a dye penetration (Board 1site 10)

Die penetration results

	Sum of Failed Interconnects	Sum of Failed Interconnects
Stencil	Туре 3	Туре 4
Α	33	19
В	26	0
С	64	3
D	3	1

No. of failed interconnects Versus Area ratio – Type 3

Graph showing the number of failed interconnects versus Stencil and area ratio Type 3 Solder paste

General Observation – Area ratio of 0.66 still needs to be observed. Stencil C shows poor quality = poor results

No. of failed interconnects Versus Area ratio – Type 4

Graph showing the number of failed interconnects versus Stencil and area ratio Type 4 Solder paste

General Observation – Stencil B shows no Fails Type 4 shows that stencil quality is not as significant **FMEA**

Photograph of a failed interconnect, Stencil C Type 3 site 14 (AR 0.63)

FMEA

Photograph of a failed interconnect, Stencil C Type 3 site 14 (AR 0.63)

Insufficient

Remember the mis - registration?

Mis-registered Solder Mask

Combination of solder mask mis registration and low solder volume, causing failed interconnect

Apertures - Location 1)

Stencil A 125 microns Stencil B 170 microns

Laser cut - Standard

Laser cut - Standard

Stencil C 190 microns

Laser cut - Defocused

E-Formed - MEMS-based fabrication process

X-Ray

Photograph of a failed interconnect, Stencil C Type 3 site 3 (210 micron)

The solder paste bridge did not manifest itself into a post reflow solder bridge

Summary

If you really want to use Type 3

a) 50-micron mask thickness and aperture diameters in the ballpark of 180 microns (this figure has been concluded from the results gained from Stencil B).

However the 50 micron mask thickness this would undoubtedly cause insufficient volumes issues with other technology types, thus not complying with heterogeneous assembly requirements.

b) A thicker material (75 microns) would be required but the aperture diameters would need to be greater than 200 microns. These aperture sizes could possible lead to solder paste bridging and coining in the Laser stencil fabrication process.

Both these options are not lending themselves to a high volume assembly.

Sensible set-up

- Type 4 solder paste
- 75 micron thick stencil
- High quality Laser cut stencil or Electro Formed
- Aperture diameters ranging from 180-210 microns

Proof

Graph showing the number of failed interconnects versus Stencil and area ratio Type 4 Solder paste

Title for slide

End Comment

