



IPC-TM-650 TEST METHODS MANUAL

1 Scope The dielectric withstanding voltage test (also called high-potential, over potential, voltage breakdown, or dielectric strength test) consists of the application of a voltage higher than rated voltage for a specific time between mutually isolated portions of a PCB or between isolated portions and ground. This is used to prove that the PCB can operate safely at its rated voltage and withstand momentary over potentials due to switching, surges, and other similar phenomena. Although this test is often called a voltage breakdown or dielectric strength test, it is not intended that this test cause insulation breakdown or that it be used for detecting corona, rather it serves to determine whether insulating materials and/or conductor spacings are adequate.

2 Applicable Documents None

3 Test Specimen The test specimen shall be comprised of a minimum of two conductor lines per conductive layer, sufficient to allow a voltage to be applied between adjacent conductor patterns both between conductive layers and on the same conductive layer (see 6.1).

4 Apparatus or Material

4.1 A high voltage source capable of supplying the specified voltage with a tolerance of $\pm 5\%$ (see 6.2).

4.2 A voltage measuring device with an accuracy of 5%. If leakage current measuring capability is required, the device shall be capable of detecting the leakage current to within 5% of the requirement.

4.3 Soft bristle brush

4.4 Deionized or distilled water (2 megohm-cm minimum resistivity recommended)

4.5 Isopropyl alcohol

4.6 Drying oven

Number 2.5.7	
Subject Dielectric Withstanding Voltage, PCB	
Date 05/04	Revision D
Originating Task Group Rigid Printed Board Performance Task Group (D-33a)	

5 Procedure

5.1 Specimen Preparation (see 6.3)

5.1.1 Positive, permanent, and noncontaminating identification of test specimen is of paramount importance.

5.1.2 Visually inspect the test specimens for any obvious defects, as described in the applicable performance specification. If there is any doubt about the overall quality of any test specimen, the test specimen should be replaced and this replacement noted.

5.1.3 Solder single stranded (to simulate discrete component axial leads) polytetrafluoroethylene (PTFE) insulated wires in each of the connection points of the test specimens. These wires will be used to connect the test patterns of the test specimens to the high voltage source.

5.1.4 Wet test lead terminals with deionized or distilled water and scrub with a soft bristle brush for a minimum of 30 seconds. During the remainder of the test specimen preparation, handle test specimens by the edges only (see 6.4).

5.1.5 Spray rinse thoroughly with deionized or distilled water. Hold test specimen at an approximate 30° angle and spray from top to bottom.

5.1.6 Wet test lead terminals with clean isopropyl alcohol and agitate for a minimum of 30 seconds. Scrub with a soft bristle brush to remove flux residue.

5.1.7 Rinse cleaned area thoroughly with fresh isopropyl alcohol.

5.1.8 Dry test specimens in a drying oven for a minimum of three hours at an oven temperature of between 49 °C to 60 °C (120 °F to 140 °F).

5.1.9 Allow the test specimens to cool to room temperature. (see 6.5)

IPC-TM-650		
Number 2.5.7	Subject Dielectric Withstanding Voltage, PCB	Date 05/04
Revision D		

5.2 Test (see 6.6)

5.2.1 Raise the test voltage from zero to one of the following specified test condition values (see 6.2) as uniformly as possible, at a rate of approximately 100 volts DC per second. If the test condition is not specified Condition A shall be the default.

- Condition A: 500+15/-0 volts DC
- Condition B: 1000+25/-0 volts DC

5.2.2 Maintain the test voltage at the specified value for a period of 30+3/-0 seconds.

5.2.3 Upon completion of the test, the test voltage shall be gradually reduced to avoid surges.

5.3 Evaluation Examine the test specimens and note any evidence of inadequate insulating materials and/or conductor spacing (i.e., visually inspect for flashover, sparkover or breakdown between conductor patterns or between conductor patterns and mounting hardware).

6 Notes

6.1 Recommended test specimens include "Y" test patterns (also referred to as "E" test coupons) or "comb patterns." Production printed boards may also be used as test specimens.

6.2 Performance specifications should specify the high voltage test condition and any deviations to this test method. If no test condition is specified, use test condition A.

6.3 This test method may be performed on test specimens which have previously been prepared and tested for moisture and insulation resistance.

6.4 Alternative cleaning procedures may be implemented if there is a concern that scrubbing will adversely affect test results, e.g., when the test specimens have very fine spacing and/or are plated with soft metals (tin/lead, gold, etc.).

6.5 Insulating compound (conformal coating) may be applied to the test specimens following soldering and cleaning. Any coating application and cure shall be as specified by the coating supplier.

6.6 The testing process outlined in 5.2 should be used for qualification testing. For in-plant quality conformance testing, the following testing modifications may be chosen:

6.6.1 At the option of the customer, reduced time with a possible correlated higher test voltage may be used.

6.6.2 At the option of the customer, an AC test voltage may be applied.

6.6.3 At the option of the customer, the test voltage may be applied instantaneously.