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3000 Lakeside Drive, Suite 105 N
Bannockburn, Illinois 60015-1249

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IPC-TM-650
TEST METHODS MANUAL

1 SCOPE

This test method describes the procedure for measuring the effects of bias voltages above 300 VDC (currently up to 3000 VDC) on the insulation systems of fabricated printed boards during exposure to elevated temperature and humidity. It will detail the test patterns, conditions and setups required to address the onset of partial discharge and unique issues associated with bias voltages above 300 VDC, e.g., dielectric break down, anodic migration phenomena, electrochemical treeing effects or equipment failures and safety issues. Figure 1-1 illustrates the general inputs necessary and feedback that can be gained from this test method.

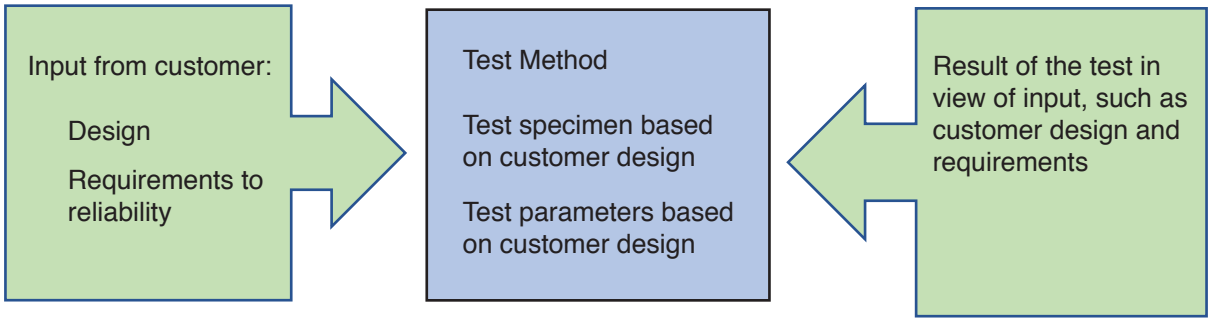

Figure 1-1

2 APPLICABLE DOCUMENTS

2.1 IPC Documents

IPC J-STD-001 Requirements for Soldered Electrical and Electronic Assemblies

IPC J-STD-006 Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications

IPC-2221 Generic Standard on Printed Board Design

IPC-TM-650 Test Methods

2.3.25 Detection and Measurement of Ionizable Surface Contaminants by Resistivity of Solvent Extract

2.6.25 Conductive Anodic Filament (CAF) Resistance Test: X-Y Axis

2.6.27 Thermal Stress, Convection Reflow Assembly Simulation

2.2 International Electrotechnical Commission Documents

IEC 60664-1 Insulation coordination for equipment within low-voltage supply systems - Part 1: Principles, requirements and tests

IEC 60664-3 Insulation Coordination For Equipment Within Low-Voltage Systems - Part 3: Use Of Coating, Potting Or Molding For Protection Against Pollution

2.3 International Organization for Standardization (ISO)

ISO/PAS 19295 Electrically propelled road vehicles — Specification of voltage sub-classes for voltage class B

3 TEST SPECIMENS

For CAF testing, the specimens are described in section 3 of IPC-TM-650, Method 2.6.25 Conductive Anodic Filament (CAF) Resistance Test: X-Y Axis.

For THB (temperature, humidity, bias) testing at high voltage within the printed board, e.g., z-direction between layer-to-layer, or on the printed board outer layer, e.g., influence by flux residues, solder resist robustness, coating robustness, no uniform test specimens are currently available with aligned acceptance by international standardization groups. For the transitional period, until a uniform test specimen will be available, individual custom-made test specimens are to be accepted. This test specimen design should reflect the printed board design in such way, that it represents the printed board design with some safety margin to cover production spread.

For generic recommendations for test specimen design, see 6.

4 EQUIPMENT/APPARATUS OR MATERIAL

4.1 Environmental Test Chamber A clean test chamber capable of producing and recording an environment of 40 ± 2 °C [104 ± 3.6 °F] and 93 ± 3 % rH, 65 ± 2 °C [149 ± 3.6 °F] and 93 ± 3 % rH or 85 ± 2 °C [185 ± 3.6 °F] and 85 + 3 / - 2% relative humidity, and that is equipped with cable access to facilitate measurement cables to be attached to the specimens under test.

4.2 Measuring System

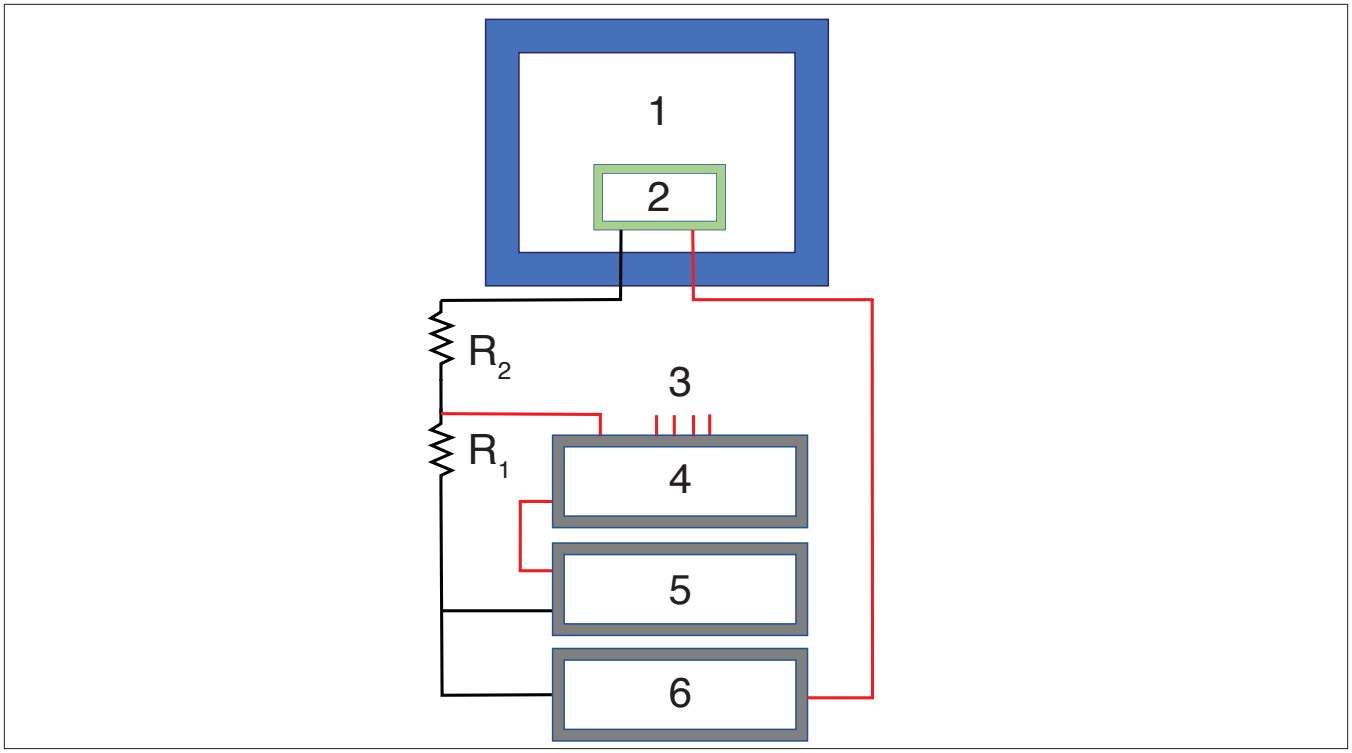

Figure 4-1 Measuring System
1. Environmental Test Chamber
2. Device Under Test (D.U.T.)
3. Additional Test Channels
4. Switching System
5. Voltage Meter
6. Power Supply

R_1. 1 MΩ Precision Resistor
R_2. Additional Current Limiting Resistance

Calculation of D.U.T. (Device Under Test) Resistance: $R_{(D.U.T.)} = (V_1 * R_1 / V_2) - R_1 - R_2$.

V_1. Bias Voltage
V_2. Voltage Drop Across R_1
R_1. 1 MΩ Precision Resistor
R_2. Additional Current Limiting Resistance

Precise measurements of V_1, V_2, R_1 and R_2 are necessary to ensure proper calculation of D.U.T. resistance. Most resistors change value as they heat up and dissipate power so care **shall** be taken to stay well withing the power ratings R_1 and R_2. R_2 should be calculated so the voltage drop across R_1 never exceeds the capability of the switching system or the voltage meter.

Additional D.U.T. test channels can be hooked to the switching system. Commercial systems combining one or more of the test units described are available.

4.2.1 Power Supply A power supply capable of producing a standing DC bias potential of greater than 10% of that required by the test. The DC supply voltage should have a tolerance of ± 2% and current supply capacity at least 10% greater than what would be required if all the test channels attached to it failed during the test, see section and table on current limiting resistors for calculations.

4.2.2 Voltmeter The range of the voltmeter should be at least 20% higher than the highest voltage to be measured. The accuracy of measurement across the measured voltage range should be at least ± 5%.

4.2.3 Current Limiting Resistance The proper selection of the total current limiting resistance value is critical for this test method. Insert the current limiting resistance in series with the terminating leads going to each test pattern. Note that some test equipment has current limiting resistors built into the testing systems that **shall** be accounted for in the calculation of total current limiting resistance.

Maximum power distributed across the sample will be when the resistance of the sample matches that of the current limiting resistance. This is when the most damage from heat can occur within the test sample and the point where 50% of the bias voltage will be dropping across the test sample. The value of the current limiting resistors **shall** be chosen based upon:

- The test voltage used.
- The power available from the power supply.
- The number of channels that are connected to the power supply.
- The maximum power that is intended to be dissipated across the sample.
- The voltage/power rating of the current limiting resistors.

The minimum suggested current limiting resistance is 1 MΩ per 300 VDC of bias voltage. Please see tables below as a reference.

The maximum power dissipation across the current limiting resistors will occur when the test sample resistance has reached a shorted condition. In order to determine the electrical ratings necessary for the current limiting resistance a calculation of total voltage drop and power dissipation **shall** be made to make sure the resistors used are capable of withstanding both the voltage and power that will occur if a sample fails. In many cases the current limiting resistance for test voltages above 300 VDC will need to be comprised of multiple resistors connected in series. This maximum power calculation multiplied by the number of circuits attached to the power supply will dictate the current rating necessary for the power supply.

Table 4-1 Maximum Power Dissipation Across Test Sample

		DC Bias Voltage						
Total Current Limiting Resistance MΩ		**100VDC**	**500VDC**	**1000VDC**	**1250VDC**	**1500VDC**	**2000VDC**	**2500VDC**
	1MΩ	50mW	1250mW	5000mW	7813mW	11250mW	20000mW	31250mW
	2MΩ	25mW	625mW	2500mW	3906mW	5625mW	10000mW	15625mW
	5MΩ	10mW	250mW	1000mW	1563mW	2250mW	4000mW	6250mW
	10MΩ	5mW	125mW	500mW	781mW	1125mW	2000mW	3125mW
	50MΩ	1mW	25mW	100mW	156mW	225mW	400mW	625mW

Note: Power is equal to voltage square divided by resistance divided by two. Maximum power dissipation across the test sample happens when the resistance of test sample equals the total (R1+R2) current limiting resistance.

Table 4-2 Maximum Current Flow Through Test Circuit When Sample Shorted

		DC Bias Voltage						
Total Current Limiting Resistance MΩ		**100VDC**	**500VDC**	**1000VDC**	**1250VDC**	**1500VDC**	**2000VDC**	**2500VDC**
	1MΩ	100µA	500µA	1000µA	1250µA	1500µA	2000µA	2500µA
	2MΩ	50µA	250µA	500µA	625µA	750µA	1000µA	1250µA
	5MΩ	20µA	100µA	200µA	250µA	300µA	400µA	500µA
	10MΩ	10µA	50µA	100µA	125µA	150µA	200µA	250µA
	50MΩ	2µA	10µA	20µA	25µA	30µA	40µA	50µA

Note: Maximum current flow is equal to voltage divided by the current limiting resistance (R1 and R2).

Table 4-3 Maximum Power Dissipation Across Current Limiting Resistors

		DC Bias Voltage						
Total Current Limiting Resistance MΩ		**100VDC**	**500VDC**	**1000VDC**	**1250VDC**	**1500VDC**	**2000VDC**	**2500VDC**
	1MΩ	10mW	250mW	1000mW	1562.5mW	2250mW	4000mW	6250mW
	2MΩ	5mW	125mW	500mW	781.3mW	1125mW	2000mW	3125mW
	5MΩ	2mW	50mW	200mW	312.5mW	450mW	800mW	1250mW
	10MΩ	1mW	25mW	100mW	156.3mW	225mW	400mW	625mW
	50MΩ	0.2mW	5mW	20mW	31.3mW	45mW	80mW	125mW

Note: Power dissipation is voltage squared divided by current limiting resistance (R1 and R2).

4.2.4 Connecting Wire – In-Chamber Use Use PTFE- or PFE-insulated copper wires and solder or screw the copper wire directly to the printed board to connect test points for each test specimen to the measurement system. The insulation material should not outgas during exposure to testing temperature/humidity. The insulating material **shall** be capable of withstanding the rated voltage of the test without electrical breakdown.

4.2.4.1 Degradation of Wire Insulation Properties The insulation of wire can degrade when exposed to high temperature/humidity environments. The insulating properties of reused wire that has been exposed to the environmental conditions of the test should be verified by a dielectric withstanding voltage test periodically. This is especially important at high voltages to prevent partial discharge in the cables.

4.2.5 Connectors and Wire Outside the Test Chamber The Insulating material of both the copper wires and connector systems used for attachment between the measurement system and the PTFE/PFE-insulated wires entering the test chamber **shall** be capable of withstanding the rated voltage of the test without electrical breakdown.

4.3 Prevention of Stray Voltages into Test Setup Outside the Test Chamber At test sample resistances over 10^{10} Ω, stray AC and DC voltages from the environment introduced into the test setup can influence measurement accuracy by increasing or decreasing the measured current flow through the test circuit. As the stainless-steel test chamber is inherently shielded against external interference, care **shall** be taken in the test setup outside the test chamber to reduce the effect radiated voltage can have on the results over 10^{10} Ω.

4.3.1 Grounding of Test Equipment and Chamber All test equipment in the setup and the environmental chamber should be connected to a common earth ground. This is important to prevent partial discharge caused by unreleased elastic charges at high voltage testing.

4.4 Issues Associated with High Voltage Testing Higher voltage almost linearly affects the time to failure, however higher voltage may offset the impact of humidity due to localized heating affecting the test results.

4.5 Automatic Test Systems Automated test systems are commercially available that automate and consolidate the test equipment listed herein. They present advantages in data collection and analysis. Care **shall** be taken to understand the limitations of automated test systems.

4.6 Safety Considerations

4.6.1 Develop Safety Considerations Performing this test can present hazardous conditions to the operator. Local, regional and company specific requirements and safety regulations for equipment installation and operation **shall** be followed. As this testing is being performed using a damp heat chamber above 300 V, there is inherent risk to operating personnel. Advice should be obtained from your local health and safety authority for advice in constructing a suitable test room.

4.6.2 Equipment Consideration As illustrated below, the room should contain:

- The test chamber fitted with a safety interlock, that creates a condition where the user is no longer potentially exposed to the high voltage.
- A bias power supply that will deliver the test voltage to the test specimens should be sited in an isolated and properly grounded cage interconnected to the test chamber.
- Cabling between the bias power supply and the test specimens should run internally from the cage, through the chamber port with no external exposure.
- Any part of the measurement system that is below 300 V can reside outside the cage.

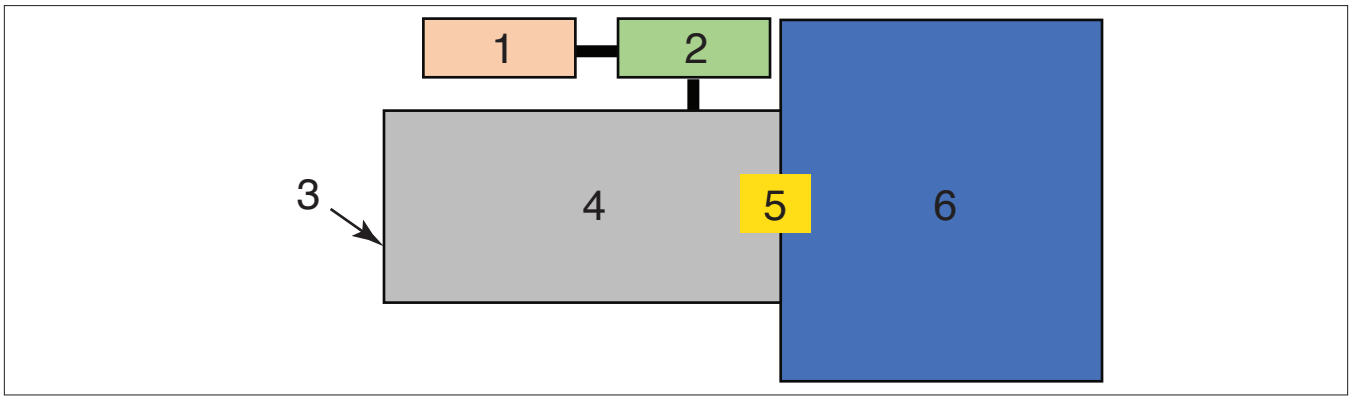

Figure 4-2 Equipment

1. Personal Computer
2. Measurement System
3. Cage Attached to Chamber with Door Interlock
4. High Voltage Power Supply and a Current Limiting Fixture Inside the Cage
5. Access Ports into the Chamber
6. Chamber with Door Interlock

5 PROCEDURE

5.1 Test Specimen Preparation

5.1.1 Sample Identification Use a method for identifying each test specimen that does not cause contamination, such as a scribe, making marks away from the biased area(s) of the specimen. Test specimens **shall** be handled by the edges of the printed board only and the use of noncontaminating gloves is recommended. Each test specimen **shall** be clearly marked to identify the simulated assembly reflow and rework processing and other differentiating parameters, completed prior to resistance testing. The marking **shall not** negatively influence the performance of the material, e.g., outgassing solvent from marking ink.

5.1.2 Prescreen for Opens and Shorts Perform as-received insulation resistance measurements using a multimeter to make connection to each net and check for gross defects. Check for shorts at a 1.0 MΩ setting. No opens are allowed in connected nets.

5.1.3 Simulated Assembly and Rework Test samples **shall** go through representative assembly and rework thermal cycling for the application. Default lead-free simulated assembly and rework is 6X at 260 °C [500 °F]. Default simulated eutectic tin-lead assembly and rework is 6X at 230 °C [446 °F]. For reference see IPC-TM-650, Method 2.6.27 Thermal Stress, Convection Reflow Assembly Simulation.

5.1.4 Cleaning of Samples for Test The process of cleaning test specimens for test by the printed board manufacturer has a purpose, can affect test results and **shall not** change the results of the material test. All cleaning steps **shall** correspond to the series of processes present during printed board manufacturing and **shall** be carried out using the procedures defined for the products the test samples are intended to represent. If no cleaning steps are defined for the product, no cleaning steps **shall** be performed for the test samples. There are exceptions, which are described below.

5.1.4.1 Test of Inner Layer Structures When testing inner layers prior to lamination, both material parameters and the printed board manufacturer's capability to build and clean the inner layers are considered. The cleaning steps at the printed board manufacturer **shall** correspond to the processes present during printed board manufacturing and **shall** be carried out using the procedures defined for the products the test samples are intended to represent. In order to decouple effects from contaminates not cleaned from the outer layer on the test result for the inner layer, an additional cleaning step should be carried out for inner layer tests for laminated printed boards, as listed in IPC-TM-650, Method 2.6.25:

Entirely clean each sample per IPC-TM-650, Method 2.3.25 Conductive Anodic Filament (CAF) Resistance Test: X-Y Axis. Detection and Measurement of Ionizable Surface Contaminants by Resistivity of Solvent Extract by immersion washing until

the level of ionic contamination is reduced to less than 1.0 microgram NaCl equivalent per square centimeter and for a maximum of 20 minutes. Test specimens not achieving this level of cleanliness within 20 minutes **shall** be scrapped for the purposes of this test. See IPC-TM-650, Method 2.6.27 Thermal Stress, Convection Reflow Assembly Simulation.

5.1.4.2 Test of Outer Layers Structures and Assembly and Interconnect Technology The cleaning of outer layers before testing **shall** follow the series of processes present during printed board/printed board assembly manufacturing and **shall** be carried out using the procedures defined for the products the test samples are intended to represent. If no cleaning takes place during the production process, the test specimen **shall not** be cleaned for the HV test either. This applies to printed board manufacturing processes such as the solder mask process or final finishing process, but also to other assembly steps such as SMD solder paste tests or testing of coatings with regards to HV applications.

5.1.4.3 Exception for Connecting Wire Attachment In order to decouple effects from the process of connecting wire attachments to the test samples on the test result of the outer layers, or the assembly technology to be tested, local cleaning of the connecting wire area should be carried out:

Perform appropriate local cleaning and rinsing after the attachment of the connecting wires in order to remove any contaminate added during the attachment process. Isolation resistance between connecting wire attachment sites should remain excellent through 96 hours pre-conditioning.

Note: Each test failure that does occur during subsequent testing should be checked to determine whether the connecting wire attachment area contributed to the test failure. If the connecting wire attachment area rather than the daisy chain area contributes to the failing insulation resistance site, then the test result for that site is no longer valid for data analysis.

5.1.5 Connecting Wire PTFE- or PFE-insulated wires, rated to withstand the test voltage, should be used for connection between the test apparatus and test specimen connection points.

5.1.6 Connection Between the Measurement System and Test Sample The test specimen **shall** be covered with noncontaminating film to prevent flux spattering during the wire attach process. Plated through holes near one edge of the printed board may be used for connecting wire to each test circuit. After stripping back the wire insulation use solder per J-STD-006 with a ROL0 or REL0 flux to attach the wire to the test specimen per J-STD-001, Class 1 or 2. Ensure against damaging printed board laminate material adjacent to the plated holes during soldering by using appropriate time/temperature parameters for the soldering iron.

Alternatively, screw or edge card connector for connection can be used, if correct function was tested and if material degradation at the connector/screw is excluded. The operator **shall** prove the function and safety of the edge card connector/screw beforehand.

5.1.7 Dry Bake sample test specimens for a minimum of 30 minutes in a clean oven at 105 ± 2 °C [221 ± 3.6 °F].

5.1.8 Precondition Preconditioning is the process where the test samples are stabilized to equilibrium at the test conditions. Precondition the test specimen samples in a bias-free state (no electrical potential applied to any test pattern) for 30 minutes minimum at 23 ± 2 °C [73.4 ± 3.6 °F] and 50 ± 5% relative humidity prior to any initial insulation resistance measurements (measuring insulation resistance of each daisy-chain net on each test specimen before starting the first 96 hours ± 30 minutes of bias-free temperature and humidity preconditioning).

5.1.9 Temperature/Humidity/Bias (T/H/B) Chamber Place the specimens in the environmental test chamber in a vertical position such that the air flow is parallel to the direction of all test specimens in the chamber. Allow at least approximately 2.5 cm [1 in] between each test specimen. Place the test specimens, as much as possible, toward the center of the chamber to help ensure optimum air flow and/or prevent drops of condensation falling onto the test specimens. Dress all wiring away from the test patterns, keeping the wires away from the test patterns as they are routed to the outside of the chamber. Also, wire should not impede airflow around the samples.

5.2 Test Procedures

5.2.1 Environmental Test Chamber Controls Tight control of the test chamber temperature and humidity is critical for this test method. A difference of 5% relative humidity can result in a 0.5 to 1.0 decade difference in measured resistance. If condensation occurs on the test specimens within the environmental chamber while the samples are under voltage, other dendritic growth can occur. Water spotting may also be observed in some ovens where the air flow in the chamber is from back to front, when water condensation on a cooler oven window can be blown around the oven as very small droplets that deposit on test specimens. This contributes to dendritic growth.

Note: Altitude can influence the test results. See IPC-2221, Table 6-1 Electrical Conductor Spacing.

5.2.1.1 Test Interrupt In the event that the environmental test chamber deviates from the controlled environment, a drop in relative humidity may be permitted for short periods not to exceed 15 minutes, provided that the chamber air temperature does not exceed test specimen temperature by more than 5 °C [9 °F]. Printed boards or test specimens being added to a chamber **shall** be pre-heated to the temperature of the chamber.

5.2.2 Resistance Measurements The resistance of each test circuit **shall** be calculated using the formula $R_{(D.U.T.)} = (V_1 * R_1 / V_2) - R_1 - R_2$, where V_1 - Bias Voltage of Test, V_2 - Voltage Drop Across R_1, R_1 - 1 MΩ precision resistor, R_2 - additional current limiting resistance and D.U.T. - Device Under Test. The polarity of the bias (conditioning) voltage and the polarity of the test (measurement) voltage **shall** always be the same.

5.2.3 Initial Insulation Resistance Energize the test bias after the samples have been placed into the test chamber but prior to closing the door and starting the environmental exposure. Measure the voltage drop across the 1 MΩ precision resistor of each test circuit and calculate the resistance of the D.U.T. Once all test circuits have been measured, de-energize the test bias.

After initial insulation resistance measurements are taken, close the environmental test chamber and set the test chamber temperature to the specified 40 ± 2 °C [104 ± 3.6 °F], 65 ± 2 °C [149 ± 3.6 °F], or 85 ± 2 °C [185 ± 3.6 °F] without adding humidity and wait until temperature equilibrium is achieved. Once temperature equilibrium has been achieved, increase relative humidity to the specified value with a ramp rate of one hour.

Allow the test specimens to stabilize at the set temperature and humidity for 96 hours ± 30 minutes with no bias applied. After the 96 hour ± 30 minutes preconditioning period, measure the voltage drop across the 1 MW precision resistor of each test circuit and calculate the resistance of the D.U.T.

It is recommended that resistance monitoring measurements be taken at a minimum of every 24 hours for the duration of the test. Sudden drops and recovery of resistance are possible and monitoring channels more often can assist in detecting these conditions. The speed of monitoring will be affected by the capability of the switching and measurement system used in the test setup.

5.2.4 Test Duration Test duration is given in section 6. At the end of the specified test duration, measure the voltage drop across the 1 MΩ precision resistor of each test circuit and calculate the resistance of the D.U.T.'s. Once all test circuits have been measured, de-energize the test bias.

Suspect test failures may be checked to determine whether the connecting wire attach area is the low resistance site rather than the daisy-chain area. This requires cutting the trace near the daisy chain (destructive). After all testing is completed, if the connecting wire attach area rather than the daisy chain area is then found to be the low insulation resistance site, then that test sample is no longer valid for data analysis.

5.3 Data Handling and Analysis Lognormal plots are recommended for plotting percent of samples above an insulation resistance value, versus insulation resistance. Use the log value of the insulation resistance.

Test specimen nets with less than 10 MΩ insulation resistance (high resistance short) after the 96 hours preconditioning **shall** be examined for assignable cause in accordance with section 5.4.1.

The insulation resistance baseline (after humidity preconditioning and before bias conditioning, see 5.2.3) value for a given daisy-chain net (same design spacing) **shall** be the average resistance of those un-shorted daisy-chain nets on all test specimens in the valid sample group as measured after the 96 hours preconditioning period.

The percent failure rate for a given sample group and subsequent test condition is the percent of test specimens that show more than a decade drop in resistance compared with the baseline value for daisy-chain nets with the same design spacing.

For a given sample lot, there may be binomial failure distributions where assignable causes exist along with different levels of capability.

5.4 Visual Examination After completion of the test, the test specimens **shall** be removed from the environmental chamber and examined progressively from 3 diopters up to 100 X magnification for evidence of surface or subsurface insulation resistance abnormality (i.e., discoloration, corrosion, dendrites, anodic migration phenomena), handling or processing defects. Additional use of UV or back light for optical inspection is recommended.

5.4.1 Assignable Cause Where an assignable cause of low insulation resistance can be properly attributed to a handling or processing defect (i.e., contamination on the insulating surface of the test specimen, scratches, cracks, or other obvious damage affecting the insulation resistance between the conductors), then such a value should be excluded.

5.5 Results All standard reporting **shall** be incorporated, including enough information to exactly reproduce the test (equipment, personnel, deviations or options within the method etc.). The report **shall** include the following as a minimum:

- Test specimen description, e.g., P/N, type of assembly, components used.
- Used test conditions like specific environmental conditions (climate), testing time, applied voltage and polarity.
- Details about preconditioning steps like baking or temperature shock-tests.
- Insulation resistance IR test results as Log10(IR) versus time plot.
- Any excluded data points and rationale.
- Any unusual events during processing or testing.

A comprehensive test report should additionally include the following information:

- Substrate information: laminate type, solder mask and final finish (SMOBC/HASL, reflow, OSP, etc.).
- Assembly information (manufacturing process, equipment, materials, pastes/fluxes, cleaning process, manufacturing location).
- Conformal coating materials or other polymer materials and processes, if used.
- Representative photo documentation of test specimen before high voltage insulation resistance test (as reference).
- Photo-documentation of post high voltage insulation resistance test visual inspection, microsection (surface and sub-surface changes like discoloration, corrosion, dendrites, anodic migration phenomena).

6 NOTES

6.1 Failure mechanisms – Documented Knowledge and First Conclusions

In 1976 Bell Laboratories [1] mentioned in a side note, that electrochemical failures by anodic migration in flexible boards or covercoats can occur by high electrical field strength. But it was not described in detail and concluded that the failure is far away from a reasonable use environment.

More details about high voltage induced failure modes on printed boards were provided 2017 by Robert Bosch GmbH [2]. In this publication the need for investigations with high voltage up to 1200 V was emphasized based on recent developments in the field of e-Mobility, e.g., inverter, charger, battery control units. Prolonged exposure of electronic control units to temperature, humidity, bias (THB) loads is reported for the automotive industry. This is caused by an extended use of plastic housings and increased exposition time which was rising from 6000 hours in former times up to 130000 hours operation time nowadays with applied voltage.

In [2] failures in the solder resist were found at 350 V during CAF testing (THB testing), that was growing from the anode to the cathode in the bulk phase of the polymer, see Figure 6-1. Thus, it was not following the CAF failure mechanism along a glass fibre and not following CAF failure life-time models.

More detailed investigations were provided by [3, 4, 5, 6]. A systematic investigation of the failure mode was published by which this occurrence was defined as anodic migration phenomena AMP in polymer materials. A strong driver for this failure mode is on one hand side the material used. It could be shown that the type of fillers, e.g., composition, ionic load, surface properties, the used dispersing agents and the crosslinking polymers are important factor of influence. This applies to both the solder mask and the base material which are used for high voltage applications. The formation of a water path inside the polymer materials is the assumed failure mechanism. Partial discharge and water treeing effects are involved in this high voltage failure mechanism of printed boards. It could be shown, that depending on the material composition the AMP effect can be shifted from the solder resist into the epoxy base material or vice versa. Areas which tend to accumulate a water path along fillers, along interfaces or along inhomogeneities of the polymer material, e.g., voids in the crystal lattice, are more prone to this failure mode, see Figure 6-2.

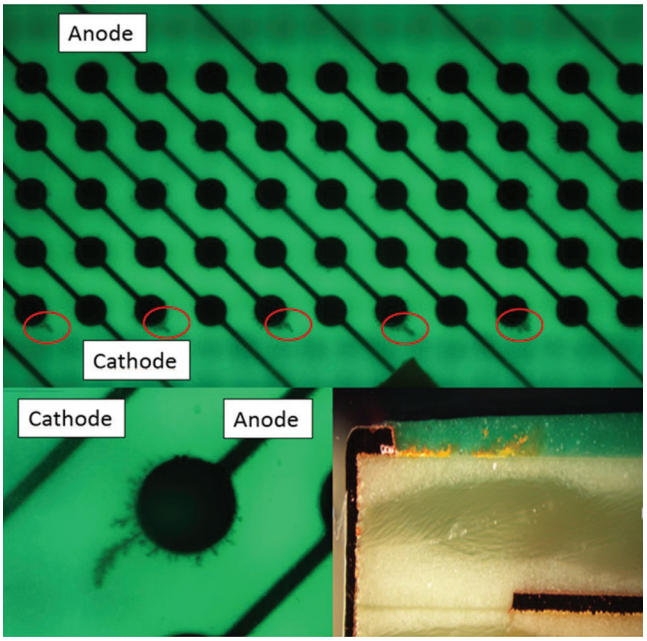

Figure 6-1 THB testing with 350 V at 85 °C, 85% rH; unexpected early failures due to anodic migration in the solder resist; anodic migration in the form of $Cu_2(OH)_3Cl$ or mixtures of Cu_xO identified [2, 3]

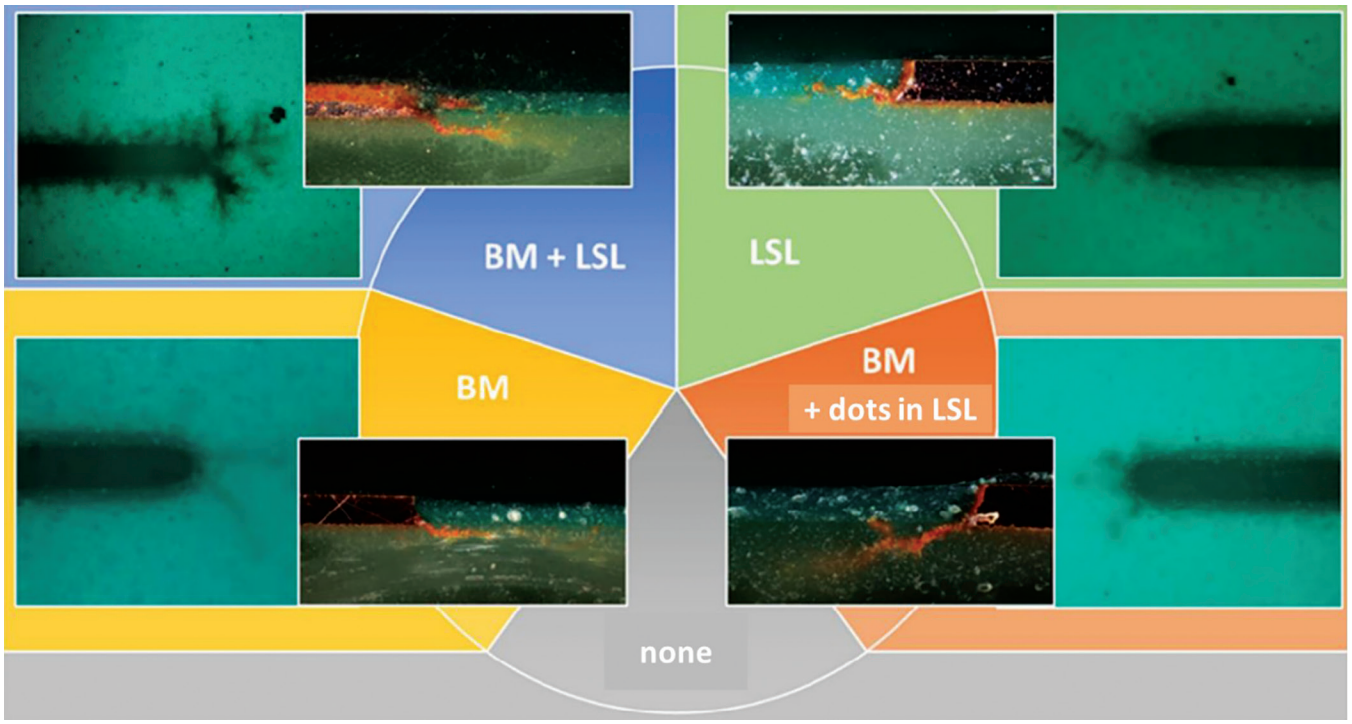

Figure 6-2 Top view in microscope with UV light and corresponding microsection of AMP failures; different propagation pathways are seen depending on solder resist (LSL) and base material (BM) [6]

In addition, hydrolysis reactions **shall** be considered that can lead to undesirable side reaction by time. Due to enhanced exposure to humidity and voltage, electrolysis of water will occur so that a local shift in the pH-value takes place at the anode and cathode. This can trigger further material degradation with subsequent failures. Based on Ohm´s and Faraday´s law, it can be assumed that these reactions are intensified with increased voltage.

On the other hand, the observed failures are also influenced by the test conditions including climate, voltage and test structure. The failure mode is not clearly seen at low voltages even if the electrical field strength is enhanced by use of test structures with a reduced spacing. It could be shown that the failure mode is triggered by a combination of electrical field strength and high voltage, see Figure 6-3. As consequence, THB tests for material characterisation **shall** be carried at the same operation voltage as used for the electronic device and cannot be simulated merely by an electrical field strength approach.

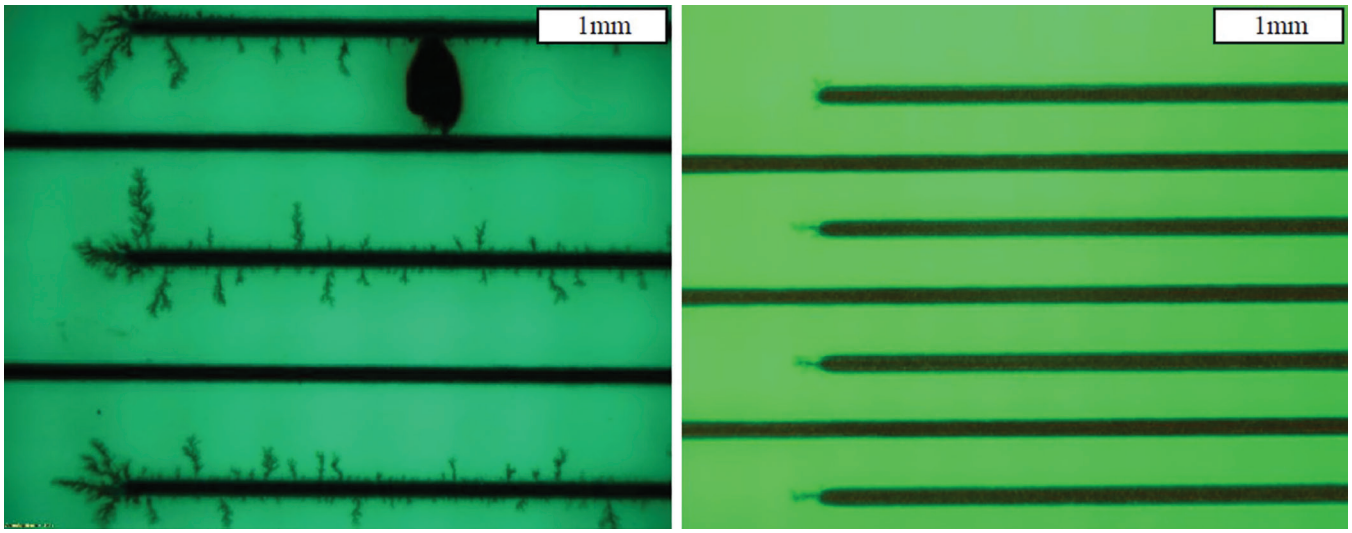

Figure 6-3 Top view on solder mask covered test structures with UV light. Left: 800 µm comb tested with 1000 V test voltage. Right: 400 µm comb tested with 500 V testing voltage. A more distinct AMP failure is found with 1000 V than with 500 V at identical electrical field strength for same materials and application [4]

The published work is also showing that a reduced testing time might not reveal all material failures caused by high voltage. A minimum testing time of 1000 hours seems to be required as test condition. In addition, the knowledge-based decision criteria of Log (SIR/(Ohm)) < 8 as fail or single drop events over two decades seems to be insufficient for high voltage material characterization, Figure 6-4.

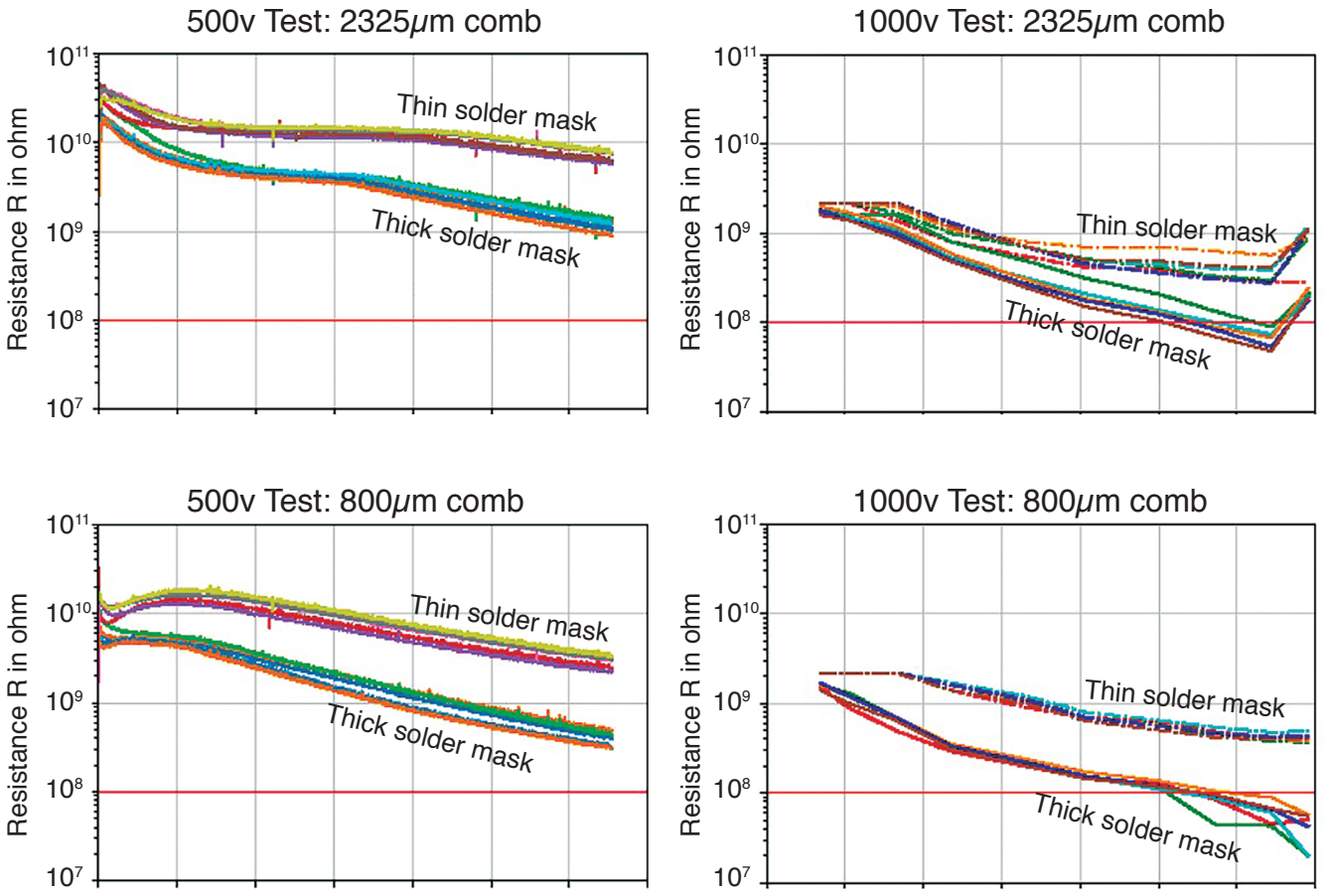

Figure 6-4 Insulation resistance measurement of printed boards with thin and thick applied solder mask tested at 85 °C, 85% rH. Insulation resistance is continuously decreasing without showing a clear drop indicating a failure. The decision criteria Log (SIR/(Ohm)) < 8 as fail does not reflect the defects found by regular optical inspection during the test period [4]

Same conclusions are valid for base material characterization as concluded from [2]. In one example it was shown that testing time > 1000 hours is required for high voltage material characterisation. In addition, layout rules with typical isolation distance of 455 µm in inner layers cannot fulfil high voltage requirements which is only found if tested in this way, see Figure 6-5.

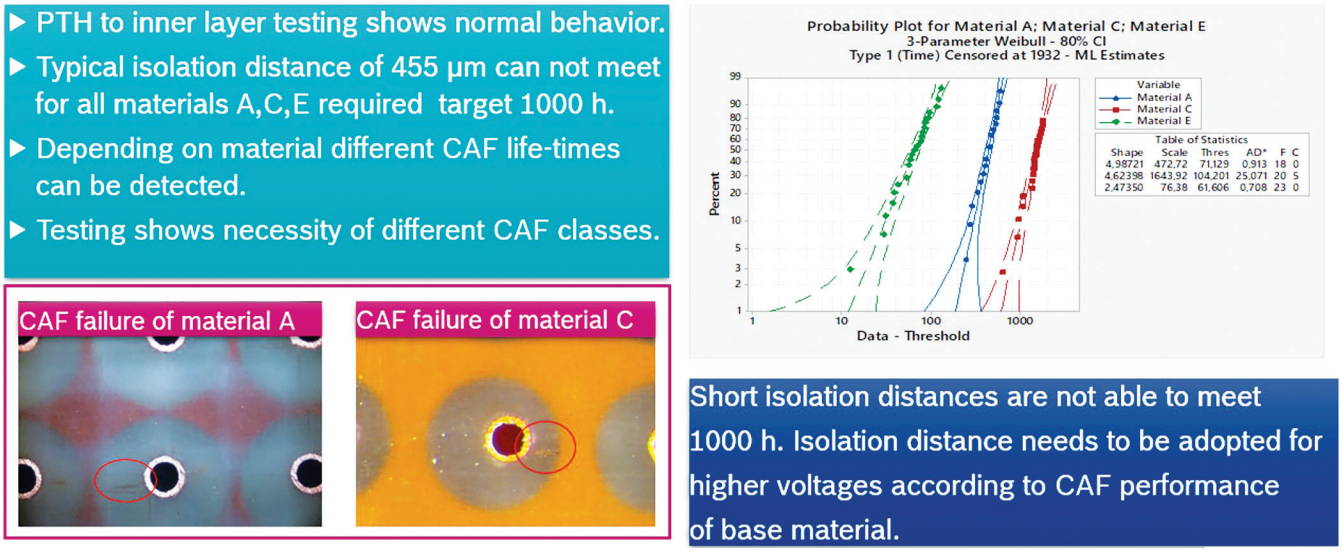

Figure 6-5 CAF testing at 85 °C, 85% rH with 350 V for different base materials with H-IL (hole to inner layer) failures [2]

In addition, the existing test methods are limited to hole-hole failures in CAF tests but **shall** be extended to other defect locations like hole to inner layer (H-IL) and inner layer to inner layer (IL-IL) failures. Printed board manufacturers are reporting in the meantime also about new failure modes found with high voltage testing [7]. In Figure 6-6 the different types of high voltage induced failures in the inner layer of a printed board are shown.

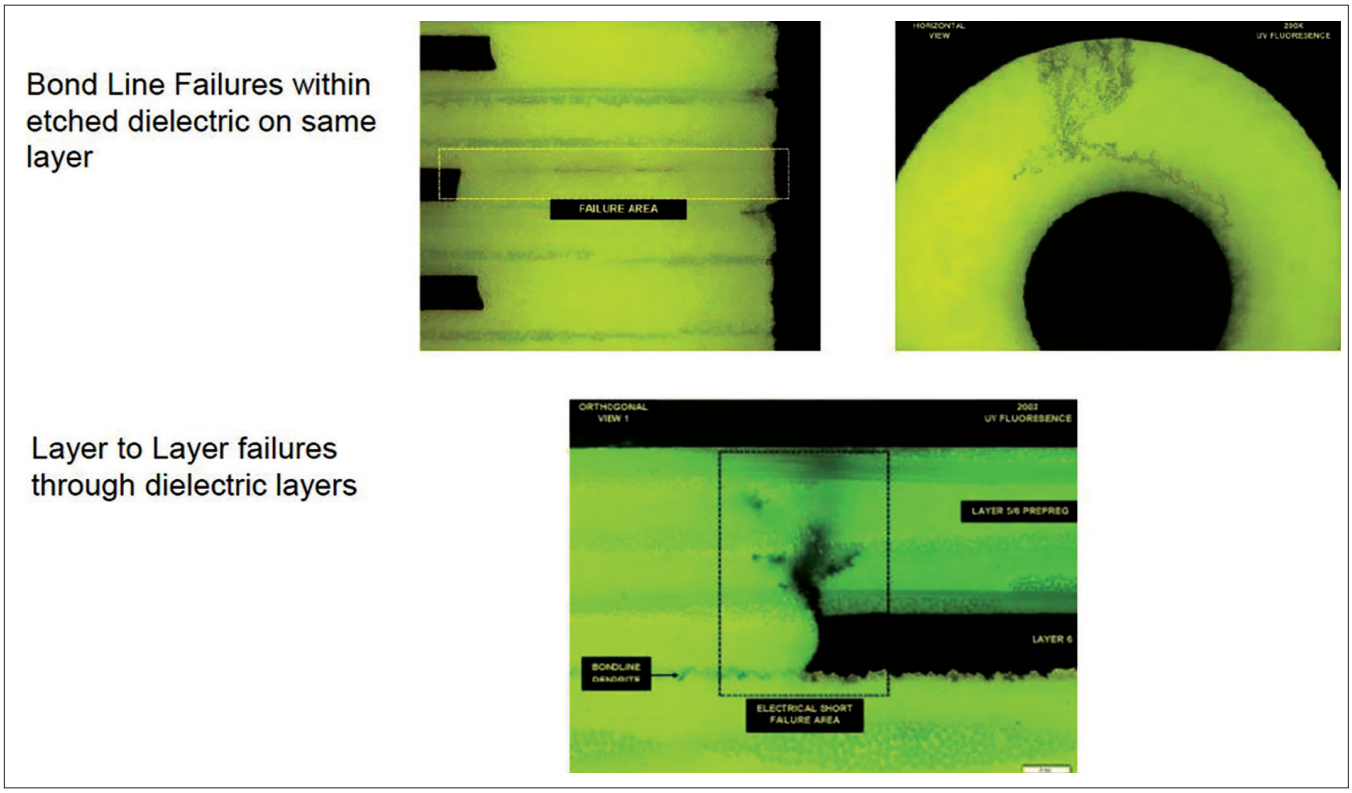

Figure 6-6 THB test with 450 V at 85 °C, 85% rH showing failures in the inner layers of a printed board [7]

For these inner layer defects, it is also unclear whether the valid decision criteria of CAF-tests can be used. Influences by polymers, e.g., composition, fillers, crosslinker, use of adhesion promotors on copper and defects by voids and particles are currently widely discussed. Cleanliness before lamination process, use of two plies of prepregs, use of high resin content prepregs are further factors that are still not aligned for achieving reliable high voltage materials.

6.2 Generic Recommendations for Testing and the Layout of a Test Specimen

High-voltage material tests should be based on real loads that are expected for the use of the product. Guidance can be found by ISO/PAS 19295 that defines the required voltage classes for e-mobility solutions. Most important voltage classes are:

- 470 V class: first generation of electrical vehicles, most widely in operation in 09/2022.
- 850 V class: second generation of electrical vehicles, currently a few realized vehicles in operation.
- 1250 V class: third generation of electrical vehicles that is currently only in planning status.
- 2500 V class: further future.

Material tests with high voltage should follow these class concept as defined by ISO/PAS 19295 to reduce test varieties. Due to country specific safety regulations a limit at 1000 V for THB testing is common. Thus, a 1000 V test condition is also considering the 1250 V class.

The correct climate conditions for THB testing are ongoing topic of discussions. The condition should be a compromise between reasonable response acceleration but without overstressing the system, which would limit material and process options. For testing of degradation mechanisms like CAF in inner layers the climate condition at 85 °C, 85% rH is common and methods for the transfer of data towards the expected end-use environment are known. Thus, for high voltage material investigations concerning inner layers of a printed board, e.g., base materials, the use of the 85 °C, 85% rH condition is still a good starting point.

However, for many polymer-materials degradation and decomposition mechanisms at 85 °C, 85% rH test conditions were observed, that are not seen in the end-use environment of the electronic device. For this reason, a trend to towards realistic humidity loads is observed also for material investigations on outer layers. For the test of materials on outer layers of a printed board like solder resist or coatings, the test condition at 65 °C, 93% rH is a good starting point.

A printed board test specimen for material investigations under high voltage load (THB test) should have a similar design as realized in the product. Not all circuit nets of a product will be operated with high voltage so that critical areas of the circuit **shall** be identified. The layout of the test specimen should not enhance or create THB-induced failures by massive overstress or by triggering changed failure mechanisms that would not occur in the intended end-use environment of the product. As consequence, different test specimens are required for differentiation of failure modes and for simulation of different areas of a printed board design. The differences between inner and outer layers, e.g., distance rules, should always be minded in the creation of a test specimen. In all, the creation of a test specimen will be a compromise between sensitivity to detection of THB induced failure but without overstressing the system, which would limit material and process options.

In general, layout improvement for test pattern and product printed boards is highly recommended for high voltage applications. Avoidance of sharp corners in copper pattern, on pads, and in solder mask clearances are highly recommended. Realization of sinusoidal shape structures for critical lines is suggested. The local field strength at the representative (specific) layout pattern is always decisive for a fault. Two-ply stack-up and separation of high voltage lines with opposite potential on different layers are advisable. Improvement in pattern etching so that sharp edges at the flank of a track are avoided as well as increase in creepage distances by introduction of routed air gaps should be considered.

The required minimum distances of copper lines or pads with critical potential difference in and on a printed board are defined by IPC-2221, IEC 60664-1 respectively IEC 60664-3. Contradicting recommendations will be found between IEC and IPC documents but both documents point in similar direction. However, a consolidation of both documents and an update of distance rules covering modern electronic materials is still missing up to date.

The distance rules depending on the applied voltage should be minded for the creation of an individual high voltage test specimen. IPC-2221 Table 6-1 reflects the range of distances that can be used as starting point.

Table 6-1 Minimum Cu-Cu distances for outer and inner layer structures derived from standards

Voltage, V	IPC-2221	IPC-2221	IEC 60664-3
	Inner Layer, Internal Conductors, mm [in]	Outer Layer, External Conductors or Terminations, Coated or Covered by Permanent Polymer, mm [in]	Outer Layer, External Conductors or Terminations, Coated or Covered by Permanent Polymer, mm [in]
470	0.250 [0.00984]	0.800 [0.0315]	1.210 [0.0476]
850	1.125 [0.0443]	1.868 [0.0735]	2.600 [0.102]
1000	1.500 [0.0591]	2.325 [0.0915]	3.200 [0.126]
2500	5.250 [0.207]	6.900 [0.272]	10.000 [0.394]

Use of these distances is recommended as starting point for the creation of an individual high voltage test specimen.

7 REFERENCES

[1] P.J. Boddy, R.H. Delany, J.N. Lahti, E.F. Landry, R.C. Restrick: Accelerated Life Testing of Flexible Printed Circuits, 1976, Bell Laboratories.

[2] E. Biehl, The necessity of temperature, humidity, bias testing with high voltages ≤ 1000V, Proceedings of SMTA International, Sep. 17 - 21, 2017, Rosemont, IL, USA.

[3] K. Lux, L. Henneken, S. Maass, M. Nowottnick, Humidity induced failure mechanisms of electronic printed circuit boards (PCBs) during high voltage testing, SMTA Europe, Electronics in Harsh Environments Conference, 24.-26.04.2018, Amsterdam, Netherland.

[4] K. Lux, L. Henneken, S. Maass, M. Nowottnick, Influence of voltage, electrical field and material ageing on humidity induced failure mechanisms of electronic printed circuit boards (PCBs) during high voltage load, European Corrosion Congress EuroCorr, 09.-13.09.2018, ICE Krakow, Poland.

[5] K. Lux, L. Henneken, S. Maass, M. Nowottnick, Behavior of solder mask and base material of PCBs under harsh environmental conditions and high voltage load, SMTA Europe, Electronics in Harsh Environments Conference, 02.-04.04.2019, Amsterdam, Netherland.

[6] K. Lux, PhD thesis, Leiterplatten unter 1000V Spannung: Einfluss des Lötstopplacks auf das unter Feuchte und hohen elektrischen Spannungen auftretende anodische Migrationsphänomen in der Leiterplatte, University of Rostock, Germany, 2022 (https://doi.org/10.18453/rosdok_id00003754).

[7] W. Olbrich, High Voltage Failure Mechanisms, TTM webinar, January 2