ECIA/IPC/JEDEC J-STD-075A

Classification of Passive and Solid State Devices for Assembly Processes

A joint standard developed by the Electronic Components Industry Association S-1 Passive Component Committees Steering Committee, IPC Plastic Chip Carrier Cracking Task Group (B-10a) and the JEDEC JC-14.1 Committee on Reliability Test Methods for Packaged Devices

Users of this standard are encouraged to participate in the development of future revisions.

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CLASSIFICATION OF PASSIVE AND SOLID STATE DEVICES FOR ASSEMBLY PROCESSES

1 SCOPE

This industry standard outlines worst case industry solder assembly process conditions for passive and solid state electronic devices (hereafter referred to as "devices). This standard provides evaluation procedures to determine whether a device can be safely subjected to those solder assembly processes and still meet all device specifications and reliability and quality expectations. This standard is not to be used for evaluating sockets and connectors, instead reference EIA-364-56 and EIA-364-61.

The classification requirements of this document are required for passive devices.

Any surface mounted, solid state device that has been classified per J-STD-020 and can withstand the thermal profile stated in J-STD-020 is not required to be classified per this standard for thermal limitations. Similarly, any through hole mounted, solid state device that meets the requirements of JESD22-B106 is not required to be classified per this standard for thermal limitations. However, any solid state device that has a history of thermal limitations or may not be subjected to cleaning or other commonly performed assembly processes is strongly recommended to be classified for those process limitations per this standard. Surface mounted, solid state devices are not to be classified to the wave solder process stated in this standard.

The solder assembly process conditions listed in this document are not recommended conditions for an assembler. An assembler needs to take into account many factors when establishing a safe assembly process for a given printed wiring board (PWB) assembly. This standard outlines a process to classify and label an electronic device's Process Sensitivity Level (PSL) and Moisture Sensitivity Level (MSL) consistent with the semiconductor industry's classification levels.

This specification does not establish re-work simulation conditions. However, this document does highlight some commonly used alternate solder assembly processes used for attaching replacement devices. It is recommended that suppliers be aware of alternate attach processes if they are commonly used on their devices and determine if their devices are sensitive to the temperature values and durations of these alternate processes.

2 PURPOSE

The purpose of this specification is to establish an agreed to set of worst case solder assembly process conditions to which devices are evaluated. The generated PSL rating will convey the conditions to which a device can be safely attached to FR4 type or ceramic laminates using SMT reflow and solder wave/fountain soldering processes. It is important for device manufacturers (hereafter referred to as "suppliers"), users, and (PWB) assemblers to be highly familiar with this standard's information and processes to insure optimal device quality and reliability.

3 DEFINITIONS

Family A grouping of devices by similar/common characteristics (e.g. package; design; materials; technology and or manufacturing process).

MSL Moisture Sensitivity Level – A rating indicating a device's susceptibility to damage due to absorbed moisture when subjected to reflow soldering (see J-STD-020)

PSL Process Sensitivity Level – A rating used to identify a device that is solder process sensitive because the device cannot be used in one or more of the base solder process conditions.

PTH For this document, the acronym PTH is defined as "Pin-Through-Hole". To avoid confusion with the printed wiring board definition of "Plated-Through Hole", this document will only use the phrase "PTH device" or "PTH package".

Supplier The device manufacturer or seller that controls the device specifications and is accountable for the device's performance.

User The individual, organization, company or agency responsible for the procurement of electrical/electronic hardware, and having the authority to define the class of equipment and any variation or restrictions (i.e., the originator/custodian of the contract detailing these requirements).

4 AGREEMENTS

When referenced by a supplier, user, or PWB assembler, this standard becomes part of their requirements/specifications.

5 APPLICABLE DOCUMENTS

The following documents, in their current revision, form a part of this specification to the extent specified herein.

EIA 364-56 *Resistance to Soldering Heat Test Procedure for Electrical Connectors and Sockets*

EIA 364-61 *Resistance to Soldering Heat from Rework Test Procedure for Electrical Connectors and Sockets*

IPC-CH-65 *Guidelines for Cleaning Printed Circuit Boards and Assemblies*

J-STD-004 *Requirements for Soldering Fluxes*

J-STD-020 *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Devices*

J-STD-033 *Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices*

JEDEC JEP140 *Beaded Thermocouple Temperature Measurement of Semiconductor Packages*

6 CLASSIFICATION PROCESS

The process for using this specification is outlined in Figure 6-1.

The process begins with the device supplier evaluating the device (or device family) against each "base" solder process conditions defined in this document. Devices which cannot meet these "base" conditions are defined as being process sensitive and the PSL rating is determined. Once the device's PSL rating is defined, those solder process conditions must be used when determining the devices MSL rating per J-STD-020. This applies to all Surface Mount (SMT) devices and Pin Through Hole (PTH) devices evaluated for SMT (e.g. paste in hole) assembly. Devices supported for SMT assembly **shall** be labeled and packed per J-STD-033 for MSL and this document for PSL (see clause 16).

When a supplier has determined that a device is process sensitive (e.g. the 2nd PSL character is >0), because the device cannot be used in one or more of the base solder process conditions, the supplier **s**hall:

a. Determine the process conditions for which this device (family) may be used using the parameters referenced in this standard.
b. Document to users and PWB assemblers per this document the acceptable process conditions.
c. Use the above determined process conditions to evaluate the device's performance at that process condition and subsequent Moisture Sensitivity analysis, classification, and packaging labeling, as outlined above.

It is recommended that a minimum sample size of 11 units be tested. It is also recommended that a minimum of two nonconsecutive assembly lots be included in the sample with each lot having approximately the same representation. Sample units shall have completed all manufacturing processes required prior to shipment.

The device's (family) ability to meet these process conditions **s**hall be re-evaluated by the supplier for any process change affecting material or device manufacturing process/controls.

The solder process evaluation includes the number of reflows, flux application, thermal profile, PWB assembly wash, vacuum pick-up, and x-ray processes outlined in this document.

Unless otherwise noted, the bake out conditions outlined in J-STD-020 for moisture sensitive devices **s**hall apply. Supplier should be contacted for support if other bake out conditions are required.