ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES®

IPC-D-356B

Bare Substrate Electrical Test Data Format

Developed by the IPC-D-356 Task Group (2-11c) of the Data Generation and Transfer Committee (2-10) of IPC

Supersedes:
IPC-D-356A - January 1998
IPC-D-356 - March 1992

Users of this standard are encouraged to participate in the development of future revisions.

Contact:

IPC
2215 Sanders Road
Northbrook, Illinois
60062-6135
Tel 847 509.9700
Fax 847 509.9798

Table of Contents

Figures

Tables

Bare Substrate Electrical Test Data Format

1 SCOPE AND OBJECTIVE

This standard describes a data format for transmitting bare board electrical test information. The material contained herein is intended to convey requirements, guidelines, and examples necessary to provide the data structures and concepts for bare board electrical test information in digital form, including data suitable for computer aided repair. When used as a netlist input to test data processing, the receiver of IPC-D-356B data will determine test point assignments and positioning.

Being essentially a netlist test format, this standard has been crafted to represent interconnect substrate graphics and test in a balanced way. Although substantial support is given to convey the graphical image of conductor shapes, the standard is not ''graphically correct.'' It is not intended to serve as a means to produce artwork or other board fabrication tools, but rather serve as a useful aid in conducting electrical test, analysis and repair.

1.1 Format Compatibility Although the concepts detailed in this standard may be supplemented by descriptions defined in other companion IPC Standards, it is intended that this standard be suitable for use as a stand alone description of bare board test and repair data for an individual circuit or job. Refer to other standards in the family for other areas of applicability.

IPC-D-356B is not backward compatible to Revision A. The VER parameter allows this version to be distinguished from previous versions.

1.2 Goal of Revision B Despite the widespread acceptance of Revision A, it became clear over time that there were many places where IPC-D-356A format was subject to interpretation and ambiguity. The intent of Revision B is to remove ambiguities, improve graphics representation and reduce file size. Desired graphical improvements consist of better representation of pads and test areas, clear solder mask determination and support for contours or polygon conductor areas. Realization of these goals took into consideration the following requirements;

- Keep it simple, at least as simple as is possible.
- Minimize the difficulty in programming input or output translators.
- Make the file as humanly readable as possible.
- While attempting to improve the graphical capability of the standard, do not attempt to make it ''graphically correct.''
- Support graphical data in commonly occurring forms to prevent the need for CAD or CAM systems from exploding a compact representation of a graphical shape into a verbose statement of the same basic shape.

Every effort has been made to eliminate data redundancy and minimize file size. Extensive use of examples will hopefully make this version even more ''user friendly'' than the previous revision.

1.3 Changes Between Revision A and B

1.3.1 Test Area Revision B contains a paradigm shift in the definition of pads and what is a ''testable pad area.'' Revision A supported round or rectangular pad shapes that may or may not be covered with soldermask. Although this approach was useful for some time, the advent of unusually shaped pads, and SMD pads defined totally or partially by soldermask render this definition imprecise.

To address these problems, two significant changes were made. The traditional ''pad'' has been replaced with two new types of records, ''test area'' and ''non-test area'' records. A test area is literally an area on a pad (often the entire pad), that might be contacted during electrical test. By definition, it is entirely free from soldermask, although it may or may not be a mid-point. By supporting ''test areas'' in simple shapes, the definition of complex underlying ''copper'' can be left to other types of ''graphics only'' records such as trace segments, polygon copper areas or simple non-test areas of copper. This makes the interpretation of where the actual test point should be located within the test area much more straightforward for the receiver of IPC-D-356B data.

1.3.2 Complex Record Changes In addition to changes related to test areas, complex records have been redefined in a more general way to represent all inter-layer connections in nets. In IPC-D-356A, complex records were introduced to support ''via in pad'' constructions while blind vias and buried vias had their own op-code and syntax. Revision B combines all these records into one format that allows the definition of all the elements of a padstack. This definition is more in keeping with the notion that the receiver of a IPC-D-356B netlist should be responsible for assigning the particular test point location within a test area. If it is desired to avoid contacting an integral hole, or perhaps preferentially test a plated hole instead of the pad, the data is there to make that determination.

1.3.3 Polygon Copper Areas Revision A lacked a means to represent contours or polygon areas of copper. To improve the graphical representation of the board, and to minimize the explosion of contours into millions of drawn