

IPC-7352

Generic Guideline for Land Pattern Design

Developed by the 1-13 Land Pattern Subcommittee of the 1-10 Printed Board Design Committee of IPC

Users of this publication are encouraged to participate in the development of future revisions.

Contact:

IPC

Supersedes:

IPC-7352 -June 2010 May 2023 IPC-7352

Table of Contents

1	SCOPE 1	4.2	TH Mounting Techniques That Impact Land
1.4	Producibility Levels		Pattern
1.5	Density Levels	4.2.1	Axial Land Pattern Design19
1.5	Use of "Lead"	4.2.2	Radial Land Pattern Design19
1.7	Terms and Definitions	4.2.3	Solder Side Land Pattern
_	ADDITION DE DOCUMENTO	4.3	Land Pattern Creation
2 2.2	APPLICABLE DOCUMENTS	4.3.1	Courtyard19
2.5	Joint Electron Device Engineering Council	4.4	Through-hole Padstacks
2.3	(JEDEC) ²	4.4.1	Nominal Hole Diameter for Pb vs Pb-free
			Solder Process
3	SURFACE-MOUNT TECHNOLOGY (SMT)	4.4.1.1	Finite Solder Flow
2.1.1	DESIGN REQUIREMENTS	4.4.1.2	Infinite Solder Flow
3.1.1	Component Tolerancing and Dimensioning 4	4.4.3	Thermal Relief21
3.1.2	Solving for Dimension Z	4.4.4	Anti-Pad21
3.1.3	Land Tolerancing	4.5	Press-fit (Compliant) Pin Type21
3.1.4	Dimension and Tolerance Analysis	4.6	Through Hole Padstack – Non-Plated
3.2	Tolerance and Solder Joint Analysis9	4.6.1	Maximum Terminal Dimension21
3.3	Courtyard Determination	4.6.2	Nominal Hole Diameter21
3.4	Land Pattern Naming Convention for	4.6.3	Anti-Pad21
2.4.1	SMD Packages 13	4.7	Land Pattern Naming Convention for PTH
3.4.1	Land Pattern Naming Convention Notes 16		Packages
3.4.2	Naming Convention Special Character Use for Land Patterns	4.7.1	Land Pattern Naming Convention for Unique
3.4.3	Suffix Naming Convention for Land Patterns 16		Packages and Connectors25
3.4.3.1	SON, QFN, SOP and QFP Components That	5	PADSTACK NAMING CONVENTION25
3.4.3.1	Have Different Thermal Pad Sizes	5.1	Basic Land Shape Letters25
3.4.3.2	Gull Wing Components That Have Different	5.2	Padstack Defaults25
5.1.5.2	Lead Tolerances	5.2.1	Examples of the Padstack Naming
3.4.3.3	Use Of Lead Geometry In Land Pattern Name 17		Convention25
3.4.3.4.	•	5.2.2	Padstack Naming Convention Modifiers26
	Reversed Pins	5.2.2.1	Use Of Letter v27
3.4.4	Land Pattern Naming Convention for Unique	5.2.2 .2	Use Of Letter w27
	Packages and Connectors features	5.2.3	Examples Utilizing Modifiers The following
	TURQUOU HOLE MOUNTED DEWOED 19		provide various examples of the padstack
4 4.1	THROUGH-HOLE MOUNTED DEVICES	5 2 Dags	naming convention's usage of modifiers:27
4.1.1	Axial Terminal Components	5.3 Paste	e Mask for Thermal Tabs29
4.1.1	Radial Terminal Components	6	LAND PATTERN QUALITY VALIDATION29
4.1.3	Multiple Pin Terminal Components	7	ZEDO COMPONIENT ODIENTATIONIS 20
	Electrical Connectors	7	ZERO COMPONENT ORIENTATIONS30
4.1.4	Electrical Confilectors		

IPC-7352 May 2023

Append	A xib	(Informative) Test Patterns – Process		Figures	
A.1	Test V	Evaluations	Figure 3-1	Profile Tolerancing Method 4	
			Figure 3-2	Example of 3216 (1206) Capacitor5	
A.2		Patterns -In-Process Validator	Figure 3-3	Profile Dimensioning of Gull wing Leaded	
A.3	Stress	Testing32	C	SOIC6	
Appendix B Polarity Marking Legend34		Polarity Marking Legend34	Figure 3-4	Courtyard Boundary Area Illustration13	
B.1	Botto	m Only Terminal Packages34	Figure 4-1	Horizontally Mounted Radial Leaded	
				Component	
Append	dix C	Component Package Naming	Figure 5-1	Basic Land Shapes25	
C.1	Area	Reference35 Array Components (BGA, FBGA, CGA,	Figure A-1	General Description of Process Validation	
C.1		Chip Array)		Contact Pattern and Interconnect31	
C.2		ponent Lead Packages	Figure A-2	Photo image of IPC Test Board for Primary	
C.3	-	ave Chip Array Packages (RESCAV,		Side	
0.5		CAV, INDCAV, OSCSC, OSCCCC)35	Figure B-1	Popular Polarity Marking Shapes33	
C.4		ex Chip Array Packages (RESCAXE,	Figure B-2	Gull Wing Terminal Legend Polarity	
		CAXS)35		Marking Location	
C.5	Flat C	Chip Array Packages (RESCAF,	Figure B-3	Sample 0.50 mm Pitch SOP Legend and	
	CAPO	CAF, INDCAF		Polarity Marking Rules34	
C.6	IPC-7	359 No-Lead Components (QFN,	Figure B-4	Bottom Only Terminal Packages	
	PQFN	N, SON, PSON, DFN, LCC)36	Figure B-5	Polarized Chip Packages	
C.6.1	Leadl	ess Chip Carrier (LCC)36	Figure C-1	Side Concave Chip Component35	
C.6.2	Quad	Flat No-Lead (QFN)37	Figure C-2	Corner Concave Chip Component35	
C.6.3	Small	Outline No-Lead Package (SON)37	Figure C-3	Convex Chip Component "E Version" 36	
C.6.4	Small	Outline and Quad Flat No-Lead with	Figure C-4	Convex Chip Component "S Version"36	
	Pullba	ack Leads (PQFN, PSON)38	Figure C-5	Flat Chip Component36	
C.6.5	Dual 1	Flat No-Lead (DFN)	Figure C-6	LCC Component	
			Figure C-7	Quad Flat No-Lead (QFN) Construction37	
			Figure C-8	QFN Devices with Multiple Paste Mask 37	
			Figure C-9	Small Outline No-Lead Package (SON)37	
			Figure C-10 PQFN Device with Pullback Leads38		
			Figure C-12 Axial Component Examples39Figure C-13 Radial Terminal Components40Figure C-15 Pin Grid Array (PGA)43		
			Figure C-16 Connectors		

May 2023 IPC-7352

	Tables	Table 3-12	Flat No-Lead with Pullback or Under
Table 3-1	Flat Ribbon L and Gull wing Leads9		Body Leads
Table 3-2	J Leads	Table 3-13 Corner Concave Lead	
Table 3-3	Rectangular or Square-End Components with Lead Widths		Crystal1
Table 3-4	Rectangular or Square-End Components with Pin Widths Smaller than 0.5 mm where Leads		Small Outline Components, Flat Lead13 Land Pattern Convention for SMD Packages
Table 3-5	1	Table 4-1	Finite Solder Flow (Includes Pin-in-Paste and Captive Solder Charge)20
	Leadless Components with Concave/ Castellated Terminations	Table 4-2	Infinite Solder Flow (Includes Wave, Solder Pot, Selective Solder, Hand Solder)20
Table 3-7 Table 3-8	Butt and I Lead	Table 4-3	Terminal to Finished Hole Size Adjustments for Board Thickness
	Flat Lug Leads ²	Table 4-4	Pad Size21
	Surface		Nominal Hole Diameter
Table 5-11	Dan Unio Array Components 17		

May 2023 IPC-7352

IPC-7352 Generic Guideline for Land Pattern Design

1 SCOPE

This document provides generic guidelines on land pattern geometries used for the attachment of electronic components to a printed board, as well as design recommendations for achieving the best possible solder joints to the devices assembled. Adjustments to the information in this guideline may be required to meet company and/or board technology requirements. It is recommended that a company should document the modifications to the IPC-7352 content in corporate command media documentation.

A land pattern is the representation of the area and features on a printed board needed for a component to be placed and attached to the printed board during an assembly process. The land pattern is usually built using ECAD Library tools.

1.1 Purpose The intent of the information presented herein is to provide the appropriate size, shape and tolerance of throughhole and surface mount land patterns to ensure sufficient area for the appropriate solder fillet to meet the requirements of IPC J-STD-001, and to allow for inspection, testing and rework of those solder joints. Designers can use the information contained herein to establish guideline land pattern geometries not only for manual designs but also for computer-aided design systems. Whether parts are mounted on one or both sides of the printed board and are subjected to wave, reflow, or other type of soldering, the land pattern and part dimensions should be optimized to ensure proper solder joint and inspection criteria.

Land patterns become a part of the printed board circuitry and they are subject to the producibility levels and tolerances associated with fabrication and assembly processes. The producibility aspects also pertain to the use of solder mask and the registration required between the solder mask and the conductor patterns.

In addition to the land pattern geometries required for proper solder joint formation, other mounting conditions should be considered, such as solder mask clearance, solder paste stencil aperture sizes, clearance between adjacent components, clearance between the bottom of the component and the printed board surface (if relevant), keep-out areas (if relevant) and adhesive applications. These additional features become part of the overall land pattern guidelines for each component type.

Note 1: The dimensions used for component descriptions have been extracted from the documents listed in 2 Applicable Documents. Designers should refer to the manufacturer's datasheet for specific component package dimensions.

Caution: Users should be aware that individual component datasheets may not meet standardized component outlines (e.g., JEDEC standard component outlines).

- **Note 2:** Elements of the mounting conditions, particularly the courtyard, given in this guideline are related to the reflow soldering process. Adjustments for wave or other soldering processes, if applicable, should be carried out by the user. This may also be relevant when solder alloys other than eutectic SnPb or SnAgCu solders are used.
- **Note 3:** Heat dissipation aspects have not been considered in this guideline.
- **Note 4:** In some cases, the lands shown in this guideline may not apply for a particular application and may need to be altered based on the end-item environmental requirements. For surface mount components, the solder joints provide not only the electrical connection, but the mechanical support as well.
- **Note 5:** Shock and vibration effects are not considered in this guideline.
- **1.2 Classification** This guideline identifies the generic physical design principles involved in the creation of land patterns for surface mount and through-hole components.
- **1.3 Performance Classification** IPC-J-STD-001 recognizes that electrical and electronic products are subject to classifications by intended end-item use. Three general end-product classes have been established to reflect differences in producibility, complexity, functional performance requirements and verification (i.e., inspection or test) frequency:

CLASS 1 General Electronic Products

Includes products suitable for applications where the major requirement is function of the completed assembly.

CLASS 2 Dedicated Service Electronic Products

Includes products where continued performance and extended life is required and for which uninterrupted service is desired but not critical. Typically, the end-use environment would not cause failures.