IPC-7095D-WAM1

Design and Assembly Process Implementation for Ball Grid Arrays (BGAs)

Developed by the Ball Grid Array Task Group (5-21f) of the Assembly & Joining Processes Committee (5-20) of IPC

Supersedes:
IPC-7095D-AM1 - June 2019
IPC-7095D - June 2018
IPC-7095C - January 2013
IPC-7095B - March 2008
IPC-7095A - October 2004
IPC-7095 - August 2000

Users of this publication are encouraged to participate in the development of future revisions.

Contact:

IPC

Table of Contents

1 SCOPE ... 1
1.1 Purpose ... 1
1.1.1 Intent ... 1
1.1.2 Interpretation of “Shall” ... 1
1.1.3 Presentation ... 1
1.1.4 Use of “Lead” ... 1
1.1.5 Abbreviations and Acronyms ... 1

2 APPLICABLE DOCUMENTS ... 1
2.1 IPC ... 1
2.2 Joint Standards ... 2
2.3 JEDEC ... 2
2.4 EIA ... 3

3 SELECTION CRITERIA AND MANAGING BGA IMPLEMENTATION ... 3
3.1 Terms and Definitions ... 3
3.1.1 Solder-Mask-Defined (SMD) BGA Pad ... 3
3.1.2 Non-Solder-Mask Defined (NSMD) BGA Pad ... 3
3.1.3 Nonwet Open (NWO) ... 3
3.1.4 Head-on-Pillow (HoP) ... 3
3.2 Overview ... 3
3.3 Description of Assembly Infrastructure ... 4
3.3.1 Land Patterns and Printed Board Considerations ... 4
3.3.2 Technology Comparison ... 5
3.3.3 Assembly Equipment Impact ... 8
3.3.4 Stencil Requirements ... 8
3.3.5 Inspection Requirements ... 8
3.3.6 Test ... 8
3.4 Time-to-Market Readiness ... 8
3.5 Methodology ... 9
3.6 Process Step Analysis ... 9
3.7 BGA Limitations and Issues ... 9
3.7.1 Visual Inspection ... 9
3.7.2 Moisture Sensitivity ... 10
3.7.3 BGA and Board Coplanarity and Warpage ... 10
3.7.4 Rework ... 11
3.7.5 Cost ... 11
3.7.6 Voids in BGAs ... 11
3.7.7 Pad Cratering ... 11
3.7.8 Head-on-Pillow (Hop) Defect ... 13
3.7.9 Nonwet Open (NWO) Defect ... 14
3.7.10 Reliability Concerns ... 14

4 COMPONENT CONSIDERATIONS ... 15
4.1 Semiconductor Packaging Comparisons and Drivers ... 15
4.1.1 Package Feature Comparisons ... 15
4.1.2 BGA Package Influencers ... 16
4.1.3 Cost Concerns ... 16
4.1.4 Component Handling ... 16
4.1.5 Thermal Performance ... 18
4.1.6 Spatial Constraint ... 18
4.1.7 Electrical Performance ... 18
4.1.8 Mechanical Performance ... 18
4.2 Die Mounting in the BGA Package ... 19
4.2.1 Wire Bonding ... 19
4.2.2 Flip Chip ... 20
4.2.3 Changing BGA Termination Materials ... 20
4.2.4 Options for Nonreballed BGAs ... 21
4.3 Standardization ... 22
4.3.1 Industry Standards for BGAs ... 22
4.3.2 BGA Package Pitch ... 24
4.3.3 BGA Package Outline ... 25
4.3.4 Ball Size Relationships ... 25
4.3.5 Package-on-Package (PoP) BGA ... 26
4.3.6 Coplanarity ... 26
4.4 Component Packaging Style Considerations ... 26
4.4.1 Solder Ball Alloys ... 27
4.4.2 Ball Attach Process ... 30
4.4.3 Ceramic Ball Grid Array (CBGA) ... 30
4.4.4 Ceramic Column Grid Arrays (CCGAs) ... 31
4.4.5 Tape-Based Ball Grid Arrays (TBGAs) ... 35
4.4.6 Multiple-Die Packaging ... 35
4.4.7 System-in-Package (SiP) ... 36
4.4.8 Three-Dimensional (3D) Folded Package Technology ... 36
4.4.9 Ball Stack ... 36
4.4.10 Folded and Stacked Packaging Combination ... 37
4.4.11 Package-on-Package (PoP) ... 37
4.4.12 Benefits of Multiple-Die Packaging ... 37
4.5 BGA Connectors and Sockets ... 38
4.5.1 Material Considerations for BGA Connectors ... 38
4.5.2 Attachment Considerations for BGA Connectors ... 38
4.5.3 BGA Materials and Socket Types ... 39
4.5.4 Attachment Considerations for BGA Sockets ... 39

4.6 BGA Construction Materials 40
4.6.1 Types of BGA Substrate Materials 40
4.6.2 BGA Substrate Materials Properties 41
4.7 BGA Package Design Considerations 42
4.7.1 Power and Ground Planes 42
4.7.2 Signal Integrity 43
4.7.3 Heat Spreader Incorporation Inside the Package 43
4.8 BGA Package Acceptance Criteria and Shipping Format 43
4.8.1 Missing Balls 43
4.8.2 Voids in Solder Balls 44
4.8.3 Solder Ball Attach Integrity 44
4.8.4 Package and Ball Coplanarity 44
4.8.5 Moisture Sensitivity (Baking, Storage, Handling and Rebaking) 45
4.8.6 Shipping Medium (Tape and Reel, Trays, Tubes) 46

5 PRINTED BOARDS AND OTHER MOUNTING STRUCTURES 46
5.1 Substrates 46
5.1.1 Organic Substrates 46
5.1.2 Inorganic Substrates 46
5.1.3 High-Density Interconnect (HDI) Build-Up Layers 46
5.2 Base Materials Considerations 48
5.2.1 Resin Systems 48
5.2.2 Laminate Material Properties 48
5.3 Printed Board Surface Finishes 49
5.3.1 Hot-Air Solder Leveling (HASL) 50
5.3.2 Organic Solderability Preservative (OSP) Coatings 51
5.3.3 Noble Platings/Coatings 51
5.4 Solder Mask 55
5.4.1 Wet- and Dry-Film Solder Masks 55
5.4.2 Jettable Solder Mask 55
5.4.3 Registration of Board-to-Panel Image for Solder Mask 56
5.5 Via Protection 56
5.5.1 Encroached Vias 56
5.5.2 Via Tenting, Plugging and Filling 56

6 PRINTED CIRCUIT ASSEMBLY DESIGN CONSIDERATIONS 58
6.1 Component Placement and Clearances 58
6.1.1 Pick-and-Place Assembly 58
6.1.2 Repair/Rework Requirements 58
6.1.3 Global Placement 59
6.1.4 Alignment Legends (Silkscreened Ink, Cu Features, Pin 1 Identifier) 59
6.2 Attachment Sites (Land Patterns and Vias) 60
6.2.1 Land Diameter Size and Its Impact on Routing 60
6.2.2 Solder-Mask-Defined (SMD) Land and Metal-Defined Land Designs 61
6.2.3 Conductor Width 62
6.2.4 Via Size and Location 62
6.2.5 Parameters Affecting Solder Mask on BGAs 64
6.2.6 Multiple-Grid BGA Land Pattern Array Designs 64
6.3 Escape and Conductor Routing Strategies 65
6.3.1 Escape Strategies 68
6.3.2 Surface Conductor and Space Width 68
6.3.3 Land-to-Via (Dog Bone) Routing Patterns 69
6.3.4 Design for Mechanical Strain Mitigation 70
6.3.5 Uncapped Via-in-Pad and Its Impacts on Reliability 71
6.3.6 Fine-Pitch BGA (FBGA) Microvia-in-Land Strategies 72
6.3.7 Power and Ground Connectivity 72
6.4 Impact of Wave Solder on Top-Side BGAs 73
6.4.1 Top-Side Reflow 73
6.4.2 Impact of Top-Side Reflow 73
6.4.3 Methods for Avoiding Top-Side Reflow 75
6.4.4 Top-Side Reflow for Pb-Free Boards 75
6.5 Testability and Test Point Access 75
6.5.1 Component Testing 75
6.5.2 Solder Ball Damage During Test and Burn-In 76
6.5.3 Printed Board Testing 77
6.5.4 Printed Board Assembly Testing 78
6.6 Other Design for Manufacturability (DfM) Issues 79
6.6.1 Panel/Pallet Design 80
6.6.2 In-Process/End-Product Test Coupons 80
6.7 Thermal Management 82
6.7.1 Conduction 82
6.7.2 Radiation 82
6.7.3 Convection 83
6.7.4 Thermal Interface Materials 83
6.7.5 Heat Sink Attachment Methods for BGAs 84

7 BGA ASSEMBLY 86
7.1 Surface Mount Assembly Processes 86
7.1.1 Solder Paste and Its Application 86
7.1.2 Component Placement Impact 92

7.1.3 Vision Systems for BGA Placement 92
7.1.4 Reflow Soldering and Profiling 94
7.1.5 Effects of Materials on Flux Activation, Component Damage and Solderability 102
7.1.6 Clean vs. No-Clean 102
7.1.7 Package Stand-Off 103
7.2 Processes After Assembly 104
7.2.1 Conformal Coatings 104
7.2.2 Use of Underfills and Adhesives 105
7.2.3 Depaneling of Printed Boards and Modules ... 111
7.3 Inspection Techniques 111
7.3.1 X-Ray Inspection 111
7.3.2 X-Ray Image Acquisition 112
7.3.3 Definition and Discussion of X-Ray System Terminology 113
7.3.4 X-Ray Image Analysis 117
7.3.5 Scanning Acoustic Microscopy (SAM) 119
7.3.6 BGA Stand-Off Measurement 121
7.3.7 Optical Inspection (Endoscopy) 121
7.3.8 Destructive Analysis Methods 122
7.4 Testing and Product Verification 125
7.4.1 Electrical Testing 125
7.4.2 Functional Test (FT) Coverage 125
7.4.3 Burn-In Testing 125
7.4.4 Product Screening Tests 125
7.5 Void Identification 125
7.5.1 Sources of Voids 126
7.5.2 Void Classification 127
7.5.3 Voids in BGA Solder Joints 127
7.6 Void Measurement 128
7.6.1 X-Ray Detection and Measurement Cautions 128
7.6.2 Impacts of Voids 128
7.6.3 Void Protocol Development 129
7.6.4 Sampling Plans for Void Evaluation 130
7.7 Process Control for Void Reduction 131
7.7.1 Process Parameter Impact on Void Formation 131
7.7.2 Process Control Criteria for Voids in Solder Balls 134
7.7.3 Process Control Criteria 135
7.8 Solder Defects 136
7.8.1 Solder Bridging 136
7.8.2 Cold Solder 136
7.8.3 Opens 136
7.8.4 Insufficient/Uneven Heating 136
7.8.5 Head-on-Pillow (HoP) 137
7.8.6 Nonwet Open (NWO) / Hanging Ball 139
7.8.7 Component Defects 139
7.9 Repair Processes 140
7.9.1 Rework and Repair Philosophy 140
7.9.2 Removal of BGAs 140
7.9.3 Replacement 141

8 RELIABILITY 143
8.1 Reliability Factors for BGA Assemblies 144
8.1.1 Cyclic Strain 144
8.1.2 Fatigue 144
8.1.3 Creep 145
8.1.4 Creep and Fatigue Interaction 146
8.1.5 Reliability Under Mechanical Loads 146
8.2 Damage Mechanisms and Failure of Solder Attachments 147
8.2.1 Comparison of Thermal Fatigue Crack Growth Mechanism in SnAgCu (SAC) vs. SnPb BGA Solder Joints 148
8.2.2 Mixed-Alloy Soldering 149
8.3 Solder Joints and Attachment Types 150
8.3.1 Global Expansion Mismatch 151
8.3.2 Local Expansion Mismatch 151
8.3.3 Internal Expansion Mismatch 151
8.4 Solder Attachment Failure 151
8.4.1 Solder Attachment Failure Classification 151
8.5 Critical Factors Impacting Reliability 156
8.5.1 Package Technology 156
8.5.2 Stand-Off Height 157
8.5.3 Printed Board Design Considerations 158
8.5.4 Reliability of Solder Attachments of Ceramic Grid Arrays (CGAs) 158
8.5.5 Pb-Free Soldering of BGAs 159
8.6 Design for Reliability (DfR) Process 165
8.7 Validation and Qualification Tests 165
8.8 Screening Procedures 166
8.8.1 Solder Joint Defects 166
8.8.2 Screening Recommendations 166
8.9 Accelerated Reliability Testing 166

9 PROCESS TROUBLESHOOTING 166
9.1 Solder Mask-Defined (SMD) BGA Conditions 166
9.1.1 Solder-Mask-Defined (SMD) and Non-Solder-Mask-Defined (NSMD) Lands 167
9.1.2 Solder-Mask-Defined (SMD) Land on Product Printed Board 167
9.1.3 Solder-Mask-Defined (SMD) BGA Failures 168

9.2 Over-Collapse BGA Solder Ball Conditions 168
9.2.1 BGA Ball Shape Without Heat Slug 500-µm Stand-Off Height 168
9.2.2 BGA Ball Shape with Heat Slug 375-µm Stand-Off Height 169
9.2.3 BGA Ball Shape with Heat Slug 300-µm Stand-Off Height 169
9.2.4 Critical Solder Paste Conditions 169
9.2.5 Void Determination Through X-Ray and Cross-Section 169
9.2.6 Voids and Uneven Solder Balls 170
9.2.7 Eggshell Void 170
9.3 BGA Warpage 170
9.3.1 BGA Warpage 171
9.3.2 Solder Joint Opens Due to Interposer Warpage 171
9.4 Solder Joint Conditions 172
9.4.1 Target Solder Condition 172
9.4.2 Solder Balls with Excessive Oxide 172
9.4.3 Dewetting 173
9.4.4 Nonwetting 173
9.4.5 Incomplete Joining Due to Land Contamination 174
9.4.6 Deformed Solder Ball 174
9.4.7 Deformed Solder Ball – Dynamic Warping 175
9.4.8 Insufficient Solder and Flux for Proper Joint Formation 175
9.4.9 Reduced Termination Contact Area 176
9.4.10 Solder Bridging 176
9.4.11 Incomplete Solder Reflow 177
9.4.12 Missing Solder 177
9.4.13 Nonwet Open (NWO) 178
9.4.14 Head-on-Pillow (HoP) Solder Joint 178

APPENDIX A **Process Control Characterization to Reduce the Occurrence of Voids** 179

APPENDIX B **Glossary of Acronyms and Abbreviations** 185

Figures

Figure 3-1 BGA Package Manufacturing Process 4
Figure 3-2 Multichip Module (MCM) Type 2S-L-WB 5
Figure 3-3 Conductor Width-to-Pitch Relationship 7
Figure 3-4 Wire-Bonded Ball Grid Array (BGA) 7
Figure 3-5 Flip Chip Bonded Ball Grid Array (BGA) 8
Figure 3-6 BGA Warpage 10
Figure 3-7 Examples of Pad Cratering 12
Figure 3-8 Various Possible Failure Modes for a BGA Solder Joint 12
Figure 3-9 Corner View (Left) and Cross-Section View (right) of a Head-on-Pillow (HoP) Solder Joint Defect 13
Figure 3-10 Cross-Section View of a Head-on-Pillow (HoP) Open Defect 13
Figure 3-11 Examples of Nonwet Open (NWO) Defects in Side View and Cross-Section View 14
Figure 4-1 Termination Types for Area Array Packages 17
Figure 4-2 Board-on-Chip (BOC) BGA Construction 19
Figure 4-3 Top of Molded Board-on-Chip (BOC) BGA 20
Figure 4-4 Flip Chip (Bumped Die) on a BGA Substrate 20
Figure 4-5 BGA Solder Joints Using SnPb – (A) and Mixed-Metallurgy (B) (Pb-Free Alloy in a SnPb Process) With Partially Mixed SnPb in a SAC Ball 22
Figure 4-6 JEDEC Standard Format for Package-on-Package Components 26
Figure 4-7 Dynamic Warpage Plot with Temperature for a Flip Chip BGA Package 28
Figure 4-8 Low-Temperature Alloys with Liquidus Temperatures Between 100 °C and 200 °C and Which Do Not Contain Pb, Cd or Au 28
Figure 4-9 SnBi Phase Diagram 29
Figure 4-10 Typical Microstructure of SnBi Solder Alloy 29
Figure 4-11 Plastic Ball Grid Array (PBGA) Package 30
Figure 4-12 Cross-Section of a Thermally Enhanced Ceramic Ball Grid Array (CBGA) Package 30
Figure 4-13 Ceramic Ball Grid Array (CBGA) Package with Molded Polymer Encapsulation 31
Figure 4-14 Typical Ceramic Column Grid Array (CCGA) With Cu Ribbon Wrap 31
Figure 4-15 Plastic BGA (PBGA) with Variety of Columns 32
Figure 4-16 Typical Solder Column with Cu Ribbon Wrap 32
Figure 4-17 Section View of PbSn10 Solder Column with Electroplated Cu Covered with SnPb40 Outer Layer 32
Figure 4-18 SnPb-Plated Microcoil (Left) and Au-Plated Microcoil (Right) 33
Figure 4-19 Au-Plated Microcoil Spring on Column Grid Array (CGA1152) Ceramic IC Package 33
Figure 4-20 Microcoil Spring with SAC305 Fillet on Column Grid Array (CGA) Package 33
Figure 4-21 Microcoil Spring (Electroplated SnPb40) Column Grid Array (CGA1152) With SnPb37 Fillet 33
Figure 4-22 Polyimide Film-Based Lead-Bond µBGA Package Substrate 35
Figure 4-23 Comparison of In-Package Circuit Routing of Single- and Two-Metal Layer Tape Substrates 35
Figure 4-24 Single-Package Die-Stack BGA 36
Figure 4-25 Custom Eight Die (Flip Chip and Wire Bond) SiP Assembly 36
Figure 4-26 Folded Multiple-Die BGA Package 36

Figure 4-27 Eight-Layer Ball Stack Package 36
Figure 4-28 Single-Sided Small Outline Dual In-Line Memory Module (SO-DIMM) Memory Card Assembly 37
Figure 4-29 Folded and Stacked Multiple-Die BGA 37
Figure 4-30 Package-on-Package (PoP) Assembly 37
Figure 4-31 BGA Connector 38
Figure 4-32 BGA Connector with Vacuum Cap 38
Figure 4-33 Pin Grid Array (PGA) Socket Pins 39
Figure 4-34 Pin Grid Array (PGA) Socket with and Without Pick-and-Place Cover 39
Figure 4-35 Land Grid Array (LGA) Contact Pin 39
Figure 4-36 Land Grid Array (LGA) Socket with and Without Pick-and-Place Cover 39
Figure 4-37 Example of Missing Balls on a BGA 43
Figure 4-38 Example of Voids in Eutectic Solder Balls at Incoming Inspection 44
Figure 4-39 Examples of Solder Ball and Land Surface Conditions 44
Figure 4-40 Establishing BGA Coplanarity Requirement ... 45
Figure 4-41 Ball Contact Positional Tolerance 45
Figure 5-1 Possible HDI Build-Ups Using Laser-Via Generation 47
Figure 5-2 Possible HDI Build-Ups Using Etching and Mechanical Processes 47
Figure 5-3 Expansion Rate Above T_g 48
Figure 5-4 Hot Air Solder Level (HASL) Surface Topology Comparison 51
Figure 5-5 Illustration of Electroless Ni/Immersion Au (ENIG) Structure 52
Figure 5-6 Black Pad Fracture Showing a Crack Between Ni and Ni-Sn Intermetallic Layer 52
Figure 5-7 Typical Mud Crack Appearance of Black Pad Surface 52
Figure 5-8 Large Region of Severe Black Pad with Corrosion Spikes Protruding into Ni-Rich Layer Through P-Rich Layer Underneath Immersion Au Surface 53
Figure 5-9 Au Embrittlement 53
Figure 5-10 Illustration of Electroless Ni/Electroless Pd/ Immersion Au (ENEPIG) Structure 53
Figure 5-11 Graphic Depiction of Directed Immersion Au (DIG) 54
Figure 5-12 Examples of Microvoids 55
Figure 5-13 Via Plugging Methods 57
Figure 6-1 BGA Alignment Marks 59
Figure 6-2 Solder Lands for BGA Components 61
Figure 6-3 Metal-Defined Land Attachment Profile 62
Figure 6-4 Solder Mask Stress Concentration 62
Figure 6-5 Solder Joint Geometry Contrast 62
Figure 6-6 Good and Bad Solder Mask Designs 63
Figure 6-7 Examples of Metal-Defined Lands 63
Figure 6-8 Bad Solder Mask Registration 64
Figure 6-9 Good Solder Mask Registration 64
Figure 6-10 Balls Anywhere Land Pattern Design for a Balls Anywhere BGA Component 65
Figure 6-11 Uniform-Grid BGA Land Pattern 65
Figure 6-12 Quadrant BGA Pattern 66
Figure 6-13 Square Array 66
Figure 6-14 Rectangular Array 66
Figure 6-15 Depopulated Array 66
Figure 6-16 Square Array with Missing Balls 67
Figure 6-17 Interspersed Array 67
Figure 6-18 Conductor Routing Strategy 68
Figure 6-19 Conductor and Space Widths for Different Array Pitches 69
Figure 6-20 One- and Two-Track Conductor Routing 69
Figure 6-21 Typical Land-to-Via (Dog Bone) Layout 69
Figure 6-22 Land-to-Via (Dog Bone) Routing Options 69
Figure 6-23 BGA Land-to-Via (Dog Bone) Land Pattern Preferred Direction for Conductor Routing 70
Figure 6-24 Preferred Screw and Support Placement 70
Figure 6-25 Connector Screw Support Placement 70
Figure 6-26 Cross-Section of 0.75-mm Ball with Via-in-Pad Structure 71
Figure 6-27 Cross-Section Illustration of Via-in-Pad Design Showing Via Cap and Solder Ball 71
Figure 6-28 Via-in-Pad Process Descriptions (BGAs on Top) 72
Figure 6-29 Microvia Example (Cross-Section) 72
Figure 6-30 Void in Microvia 72
Figure 6-31 Ground or Power BGA Connection 73
Figure 6-32 Example of Ball Deformation and Dewetting of Top-Side Reflow Joints 73
Figure 6-33 Top-Side Mixed-Component Board Assembly Wave Soldering Temperature Profile 74
Figure 6-34 Heat Pathways to BGA Solder Joint During Wave Soldering 74
Figure 6-35 Methods of Avoiding Top-Side BGA Solder Joint Reflow During Wave Soldering 75
Figure 6-36 Example of a Side Contact Made with Tweezers-Type Contact 76
Figure 6-37 Pogo-Pin-Type Electrical Contact Impressions on the Bottom of a Solder Ball 76
Figure 6-38 Area Array Land Pattern Testing 77
Figure 6-39 Board Panelization 81
Figure 6-40 Comb Pattern Examples 81
Figure 6-41 Heat Sink Attached to a BGA Using Adhesive 84
Figure 6-42 Heat Sink Attached to a BGA Using a Clip 85
Figure 6-43 Heat Sink Attached to a BGA Using a Clip That Hooks into Printed Board Holes 85
Figure 6-44 Heat Sink Attached to a BGA Using a Clip That Hooks onto a Stake Soldered to the Printed Board 85

Figure 6-45 Heat Sink Attached to a BGA by Wave Soldering Its Pins in Through-Holes 86
Figure 7-1 Stencil Aperture Labels for Aspect Ratio, Area Ratio Calculations (Solder Stencil Feature Dimensions) 88
Figure 7-2 BGA Balls After Paste Dipping 90
Figure 7-3 Cavity Board and 3D Stencil 90
Figure 7-4 3D Stencil with Two Cavity Pockets 90
Figure 7-5 Slit-Metal Squeegee 91
Figure 7-6 Cavity Keep-Out Zone 91
Figure 7-7 High-Pb and Eutectic Solder Ball and Joint Comparison 91
Figure 7-8 Balls Anywhere Image Captures for Offline Teaching 93
Figure 7-9 Examples of Peak Reflow Temperatures at Various Locations at or Near a BGA 94
Figure 7-10 Schematic of Reflow Profile for SnPb Assemblies 96
Figure 7-11 Schematic of Reflow Profile for Pb-Free Assemblies 96
Figure 7-12 Locations of Thermocouples on a Printed Board Assembly with Large and Small Components 97
Figure 7-13 Recommended Locations of Thermocouples on a BGA 97
Figure 7-14 Proper Thermocouple Location on a BGA Connector 97
Figure 7-15 Comparison of Assembly Processes for a SAC BGA Component Using SAC Solder Paste (Top), BiSn Baseline or Ductile Metallurgy Solder Paste (Middle) and Resin-Containing Joint-Reinforcement Paste (JRP) (Bottom) 98
Figure 7-16 Comparison of the Reflow Temperature Profiles for SAC, BiSnAg and Low-Temperature JRP Solder Pastes 99
Figure 7-17 Mixed-Alloy BGA Solder Joint Formed with SAC Ball Soldered with Ductile Metallurgy BiSn Solder Paste 100
Figure 7-18 Mixed-Alloy BGA Solder Joint Formed with SAC Ball Soldered with BiSn Joint-Reinforcement Paste (JRP) 100
Figure 7-19 Effect of Paste Volume on the Area of Bi-Mixed Regions with Mixed-Alloy SAC-BiSn BGA Solder Joints 101
Figure 7-20 Solder Joint Shapes and Microstructures for Three Combinations of Solder Balls and Solder Pastes for a Paddle-Contact BGA Socket 101
Figure 7-21 Effect of Solder Mask Relief Around BGA Lands of a Printed Board 104
Figure 7-22 Impact of Improper Usage of Conformal Coating 105
Figure 7-23 Map of Underfill Adhesive Usage for BGAs and Other Packages 106
Figure 7-24 BGA Package with Incomplete Underfill Coverage 107
Figure 7-25 Flow of Underfill Between Two Parallel Surfaces 107
Figure 7-26 Examples of Air Bubbles in Underfill 108
Figure 7-27 Example of Partial Underfill 108
Figure 7-28 Microsection of BGA With Corner-Applied Adhesive 109
Figure 7-29 Top View of BGA With Corner-Applied Adhesive 109
Figure 7-30 Critical Dimension for Application of Corner-Applied Adhesive Prior to Reflow 109
Figure 7-31 Typical Corner-Applied Adhesive Failure Mode 109
Figure 7-32 Examples of Four Strategies for Polymeric Reinforcement of BGA Solder Joints 110
Figure 7-33 Solder Joint Encapsulation Material (SJEM) 110
Figure 7-34 Fundamentals of X-Ray Technology 112
Figure 7-35 X-Ray Example of Head-on-Pillow (HoP) Solder Joints 112
Figure 7-36 Three X-Ray Examples of Voiding in Solder Ball Contacts 112
Figure 7-37 Two Examples of Manual X-Ray System Image Quality 113
Figure 7-38 Example of X-Ray Pin Cushion Distortion and Voltage Blooming 113
Figure 7-39 Transmission Image (2D) 114
Figure 7-40 Tomosynthesis Image (3D) 114
Figure 7-41 Laminography 3D Automated X-Ray Inspection (AXI) Section Image 114
Figure 7-42 High-Quality 2D Transmission X-Ray Image Example 115
Figure 7-43 Oblique Viewing Printed Board Tilt 115
Figure 7-44 Oblique Viewing Detector Tilt 115
Figure 7-45 Top-Down View of FBGA Solder Joints 116
Figure 7-46 Oblique View of FBGA Solder Joints 116
Figure 7-47 Large Board Computed Tomography (CT) / Partial CT Principle 116
Figure 7-48 Large-Board Computed Tomography (CT) Scan (Left) and 3D Rendering (Right) Showing Head-on-Pillow (HoP) 117
Figure 7-49 Large-Board Computed Tomography (CT) ... 117
Figure 7-50 Tomosynthesis 117
Figure 7-51 Scanned Beam X-Ray Laminography 118
Figure 7-52 Voiding Creation Dynamics Within a QFN Device Observed Using Heated Stage 119
Figure 7-53 Typical Acoustic Microscopy Configuration .. 120
Figure 7-54 C-Scan Image (left) and T-Scan Image (right) of the Same BGA 120
Figure 7-55 Endoscope Example 1 121
Figure 7-56 Endoscope Example 2 121
Figure 7-57 Endoscope Example 3 121
Figure 7-58 Engineering Crack Evaluation Technique 122
Figure 7-59 Solder Balls Cross-Sectioned Through Voids in the Solder Balls 122

Figure 7-60 Cross-Section of a Crack Initiation Near the Ball/Pad Interface 123

Figure 7-61 Dye and Pull (Pry) Showing No Dye Indications on the BGA Pad or Printed Board Surfaces 123

Figure 7-62 Dye and Pull (Pry) Showing Dye Indications on Both the Printed Board and BGA Pads 124

Figure 7-63 Dye and Pull (Pry) Showing Laminate Fractures (Pad Cratering) With Dye Indications on BGA Side and Printed Board Side 124

Figure 7-64 Small Voids Clustered in Mass at the Ball-to-Land Interface 126

Figure 7-65 Typical Size and Location of Various Types of Voids in a BGA Solder Joint 127

Figure 7-66 X-Ray Image of Solder Balls with Voids 128

Figure 7-67 Comparison Between Standard Reflow Soldering (Top) and Vacuum-Assisted Reflow Soldering (Bottom) for BGA Solder Joints 133

Figure 7-68 Vacuum-Assisted Convection Reflow Oven 133

Figure 7-69 Vacuum-Assisted Vapor Phase Reflow Oven 134

Figure 7-70 Time vs. Pressure Plot Showing the Difference Between Vacuum-Assisted and High-Pressure Soldering Processes 134

Figure 7-71 Example of Voided Area at Land and Printed Board Interface 135

Figure 7-72 X-Ray Image Showing Uneven Heating 136

Figure 7-73 X-Ray Image at 45° Showing Insufficient Heating in One Corner of the BGA 136

Figure 7-74 Example of Head-on-Pillow (HoP) Showing Ball and Solder Paste That Have Not Coalesced 137

Figure 7-75 Head-on-Pillow (HoP) Occurrence Process Sequence 137

Figure 7-76 Head-on-Pillow (HoP) Due to High Package Warpage 138

Figure 7-77 Example of Liquidus Time Delay (LTD) 138

Figure 7-78 Solder Particles on a Printed Board Noncoalesced After Reflow 138

Figure 7-79 Examples of Hanging Ball Defects 139

Figure 7-80 X-Ray Image of Popcorning 139

Figure 7-81 X-Ray Image Showing Warpage in a BGA .. 140

Figure 7-82 BGA/Assembly Shielding Examples 141

Figure 8-1 Example of Solder Joint Crack Due to Thermomechanical Fatigue 148

Figure 8-2 BGAs Following Thermal Cycling Showing Coarsening with a Fatigue Crack (A) and Coarsening (B) 148

Figure 8-3 Thermal Fatigue Crack Propagation in Eutectic SnPb Solder Joints in a Ceramic Ball Grid Array (CBGA) Module 149

Figure 8-4 Thermal Fatigue Crack Propagation in SnAg3.8Cu0.7 Joints in a Ceramic Ball Grid Array (CBGA) Module 149

Figure 8-5 Incomplete Solder Joint Formation for 1 % Ag Ball Alloy Assembled at Low End of Typical Process Window 150

Figure 8-6 Solder Joint Failure Due to Silicon and Printed Board Coefficient of Thermal Expansion (CTE) Mismatch 151

Figure 8-7 Cold Solder Joint with Grainy Appearance .. 152

Figure 8-8 Land Contamination (Solder Mask Residue) 152

Figure 8-9 Solder Ball Drop 152

Figure 8-10 Missing Solder Ball 153

Figure 8-11 Dynamic Warpage of Flip Chip BGAs and Printed Boards 153

Figure 8-12 Solder Joint Defects Caused by Severely Warped BGA and Printed Board After Reflow 154

Figure 8-13 Examples of Acceptable Convex Solder Joints 154

Figure 8-14 Example of an Acceptable Columnar Solder Joint 155

Figure 8-15 Two Examples of Pad Cratering (Located at Corner of BGA) 155

Figure 8-16 Pad Crater Under 1-mm-Pitch Pb-Free Solder Ball 155

Figure 8-17 Cross-Sections Illustrating Insufficient Melting of Solder Joints During Reflow 156

Figure 8-18 Solder Mask Influence 158

Figure 8-19 Reliability Test Failure Due to Very Large Void 158

Figure 8-20 Endoscope Photo of SnAgCu (SAC) BGA Solder Ball 161

Figure 8-21 Comparison of Reflow Soldering Profiles for SnPb, Backward-Compatibility and Pb-Free Printed Board Assemblies 162

Figure 8-22 Micrographs of a Cross-Section of a BGA SAC Solder Ball Assembled onto a Printed Board with SnPb Solder Paste Using Standard SnPb Reflow Soldering Profile 162

Figure 8-23 Micrograph of a Cross-Section of a BGA SAC Solder Ball Assembled onto a Printed Board with SnPb Solder Paste Using Backward-Compatibility Reflow Soldering Profile 163

Figure 8-24 Mixed-Metallurgy (SAC/SnPb) BGA Solder Joint Alternatives 164

Figure 9-1 Cracks Caused by Solder-Mask-Defined (SMD) Land 167

Figure 9-2 Solder Mask Encroaching Too Far on Land 167

Figure 9-3 Solder Mask-Defined (SMD) BGA Solder Joint Failure 168

Figure 9-4 BGA Ball Shape Without Heat Slug 500-µm Stand-Off Height 168

Figure 9-5 BGA Ball Shape with Heat Slug 375-µm Stand-Off Height 169

Figure 9-6 BGA Ball Shape with Heat Slug 300-µm Stand-Off Height 169

Figure 9-7 Uneven and Missing Solder Balls 170
Figure 9-8 Eggshell Void 170
Figure 9-9 Convex (Frowning) BGA With Bridging at Corners 171
Figure 9-10 Solder Joint Opens Due to Interposer Warpage 171
Figure 9-11 Target Solder Condition 172
Figure 9-12 Solder Balls with Excessive Oxide 172
Figure 9-13 Dewetting of Solder at Interface 173
Figure 9-14 Nonwetting 173
Figure 9-15 Incomplete Joining Due to Land Contamination 174
Figure 9-16 Solder Ball Deformation 174
Figure 9-17 Column-Shaped Ball Deformation 175
Figure 9-18 Suspended Solder Ball 175
Figure 9-19 Extended and Proper Solder Connections on the Same BGA 176
Figure 9-20 Solder Bridging 176
Figure 9-21 Incomplete Solder Reflow 177
Figure 9-22 Missing Solder Paste Deposit 177
Figure 9-23 Nonwet Open (NWO) 178
Figure 9-24 Head-on-Pillow (HoP) 178
Figure A-1 Typical Flow Diagram for Void Assessment 179
Figure A-2 Voids in BGAs With Crack Started at Corner Lead 183
Figure A-3 Void Diameter Related to Land Size 184

Tables

Table 3-1 Multichip Module (MCM) Definitions 5
Table 3-2 Number of Conductors vs. Array Size on Two Layers of Circuitry 6
Table 3-3 List of IPC Standards Related to Pad Cratering 13
Table 4-1 JEDEC Standard JEP95-1/5 Allowable Ball Diameter Variations for FBGA 23
Table 4-2 Ball Diameter Sizes for Plastic BGAs (PBGAs) 24
Table 4-3 Ball Diameter Sizes for Die-Size BGAs (DSBGAs) 24
Table 4-4 Land Pattern Design 24
Table 4-5 Land-to-Ball Calculations for BGA Packages (mm) 25
Table 4-6 Examples of JEDEC-Registered BGA Outlines 26
Table 4-7 Pb-Free Alloy Variations 27
Table 4-8 Column Grid Array (CGA) Land Size Approximation 34
Table 4-9 Column Grid Array (CGA) Alloy and Construction Styles 34
Table 4-10 IPC-4101 FR-4 Property Summaries – Illustrations of Specification Sheets of Materials Projected to Better Withstand Pb-free Assembly 41
Table 4-11 Typical Properties of Common Dielectric Materials for BGA Package Substrates 42
Table 4-12 Controlled Coplanarity Per Ball Size 45
Table 4-13 Moisture Classification Level and Floor Life 46
Table 5-1 Key Attributes for Various Printed Board Surface Finishes 50
Table 5-2 Evaluation Via Filling/Encroachment Based on Surface Finish Process 56
Table 5-3 Via Fill Options 58
Table 6-1 Number of Conductors Between Solder Lands – 1.27-mm-Pitch BGA (0.75-mm Ball Diameter) 60
Table 6-2 Number of Conductors Between Solder Lands – 1-mm-Pitch BGA (0.60-mm Ball Diameter) 60
Table 6-3 Number of Conductors Between Solder Lands – 0.80-mm-Pitch BGA (0.50-mm Ball Diameter) 60
Table 6-4 Number of Conductors Between Solder Lands – 0.65-mm-Pitch BGA (0.40-mm Ball Diameter) 60
Table 6-5 Number of Conductors Between Solder Lands – 0.50-mm-Pitch BGA (0.30-mm Ball Diameter) 61
Table 6-6 Maximum Solder Land to Pitch Relationship (mm) 61
Table 6-7 Escape Strategies for Full Arrays 68
Table 6-8 Conductor and Space Width for Different Array Pitches 68
Table 6-9 Effects of Material Type on Conduction 82
Table 6-10 Emissivity Ratings for Certain Materials 83
Table 7-1 Solder Ball Size Distribution by Type and Mesh 87
Table 7-2 Recommendations for Solder Powder Type for Different Pitches to Achieve Good Solder Paste Release (S/P Ratio > 4.2) 87
Table 7-3 Stencil Thicknesses Per BGA Pitch 87
Table 7-4 Pros and Cons of Common Stencil Technologies and Options 89
Table 7-5 Fine-Pitch BGA (FBGA) Printing Options 90
Table 7-6 Example of Solder Paste Volume Requirements for Ceramic Array Packages 92
Table 7-7 Profile Comparison Between SnPb and SAC Alloys 95
Table 7-8 Inspection Usage Application Recommendations 111
Table 7-9 Field of View for Inspection 118
Table 7-10 Void Classification 127
Table 7-11 Examples of Suggested Void Protocols 129
Table 7-12 Ball-to-Void Size Image – Comparisons for Various Ball Diameters 130
Table 7-13 Repair Process Temperature Profiles for SnPb Assembly 143
Table 7-14 Repair Process Temperature Profiles for Pb-Free Assemblies 143

Table 8-1 Typical Stand-Off Heights for BGAs 157

Table 8-2 Melting Points, Advantages and Disadvantages of Common Solder Alloys 159

Table 8-3 Types of Pb-free Assemblies 161

Table A-1 Corrective Action Indicator for Lands Used With 1-mm, 1.27-mm and 1.5-mm Pitch 181

Table A-2 Corrective Action Indicator for Lands Used With 0.5-mm, 0.65-mm or 0.8-mm Pitch 182

Table A-3 Corrective Action Indicator for Microvia-in-Pad Lands Used With 0.3-mm, 0.4-mm or 0.5-mm Pitch 183

Design and Assembly Process Implementation for Ball Grid Arrays (BGAs)

1 SCOPE

This standard describes design and assembly implementation for ball grid array (BGA) and fine-pitch BGA (FBGA) technology, focusing on inspection, repair and reliability issues associated with design and assembly of printed boards using these packages.

1.1 Purpose The purpose of this standard is to provide useful and practical information to those who use or are considering using BGAs. The target audiences for this document are managers, designers and process engineers who are responsible for design, assembly, inspection and repair processes of printed boards and printed board assemblies.

1.1.1 Intent This document describes how to successfully implement robust design and assembly processes for printed board assemblies using BGAs as well as ways to troubleshoot some common anomalies which can occur during BGA assembly. For accept/reject criteria and requirements for BGA assemblies, see J-STD-001 and IPC-A-610.

1.1.2 Interpretation of ''Shall'' The imperative form of the verb ''**shall**'' is used throughout this standard whenever a requirement is intended to express a provision that is mandatory. Deviation from a ''**shall**'' requirement may be considered if sufficient data are supplied to justify the exception. To assist the reader, the word ''**shall**'' is presented in bold characters.

The words ''should'' and ''may'' are used whenever it is necessary to express nonmandatory provisions. ''Will'' is used to express a declaration of purpose.

1.1.3 Presentation All dimensions and tolerances in this specification are expressed in hard SI (metric) units and bracketed soft imperial [inch] units. Users of this specification are expected to use metric dimensions. All dimensions ≥ 1 mm [0.0394 in] will be expressed in millimeters and inches. All dimensions < 1 mm [0.0394 in] will be expressed in micrometers and microinches.

1.1.4 Use of ''Lead'' For readability and translation, this document uses the word lead only to describe leads of a component (sometimes referred to as terminations).

1.1.5 Abbreviations and Acronyms Periodic table elements are abbreviated in this standard. See Appendix B for full spellings of abbreviations (including elements) and acronyms used in this standard.

2 APPLICABLE DOCUMENTS

2.1 IPC[1]

IPC-T-50 Terms and Definitions for Printed Boards and Printed Board Assemblies

IPC-D-279 Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies

IPC-A-610 Acceptability of Electronic Assemblies

IPC-TM-650 Test Methods Manual[2]

2.4.42 Torsional Strength of Chip Adhesives

IPC-SM-785 Guidelines for Accelerated Reliability Testing of Surface Mount Attachments

IPC-SM-817 General Requirements for Dielectric Surface Mounting Adhesives

IPC-CC-830 Qualification and Performance of Electrical Insulating Compound for Printed Wiring Assemblies

IPC-HDBK-830 Guidelines for Design, Selection and Application of Conformal Coatings

IPC-1401 Corporate Social Responsibility and Sustainability Protocols for Electronic Manufacturing Industry

IPC-1601 Printed Board Handling and Storage Guidelines

IPC-1751 Generic Requirements for Declaration Process Management

1. www.ipc.org
2. Current and revised IPC Test Methods are available on the IPC Web site (www.ipc.org/test-methods.aspx)